PORTATONE

PSR-1000/PSR-2000

SERVICE MANUAL

PSR-1000

PSR-2000

■ **CONTENTS**

PK **001666**

YAMAHA

HAMAMATSU, JAPAN

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■ LSI PIN DESCRIPTION

● **HD63266F** (XI939A00) **FDC** (Floppy Disk Controller)

DM: IC300

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	8"//5"	I	Data transmission speed	33	/TRKO	I	Track 00 signal
2	XTALSET	I	Clock select	34	/INDEX	I	Index signal
3	/RESET	I	Rest	35	/RDATA	I	Read data input from FDD
4	E//RD	I	Enable/Read	36	XTAL2		Clock
5	RW//WR	I	Read/write/Write	37	EXTAL2		
6	/CS	I	Chip select	38	NC		
7	/DACK	I	DMA acknowledge	39	XTAL1		Clock
8	RS0	I	Register select	40	EXTAL1		
9	RS1	I		41	VSS4		Ground
10	VSS1		Ground	42	VSS5		
11	VSS2			43	NC		
12	D0	I/O	Data bus	44	VCC2		Power supply
13	D1	I/O		45	VCC3		
14	D2	I/O		46	VCC4		
15	D3	I/O		47	/WGATE	O	Write control
16	D4	I/O		48	/WDATA	O	Writ data to FDD
17	D5	I/O		49	VSS6		Ground
18	D6	I/O		50	/STEP	O	Step signal to control head of FDD
19	D7	I/O		51	/HDIR	O	Direction
20	/DREQ	O	DMA request	52	/HLOAD	O	Head load
21	/IRQ	O	Interrupt request	53	/HSEL	O	Head select
22	/DEND	I	Data end	54	VSS7		Ground
23	VSS3		Ground	55	/DS0	O	Drive select
24	1/2 EX1			56	/DS1	O	
25	VCC1		Power supply	57	/DS2	O	
26	NUM1	I		58	/DS3	O	
27	NUM3	I		59	VSS8		Ground
28	IFS	I	Host interface select	60	/MON0	O	Motor on
29	SFORM	I	Format data	61	/MON1	O	
30	/INP	I	Index pulse	62	/MON2	O	
31	/READY	I	Ready from FDD	63	/MON3	O	
32	/WPRT	I	Write control signal	64	VSS9		Ground

● **AK5351-VF-E2** (XV510A00) **ADC** (Analog to Digital Converter)

DM: IC800 (PSR-2000)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	AINR+	I	Analog signal input (R channel +)	13	DGND	-	Digital ground
2	AINR-	I	Analog signal input (R channel -)	14	TST4	I/O	Test mode setting 4
3	VREF	O	Reference voltage	15	AMODE2		Interface clock select 2
4	VA	-	Analog power supply	16	/PD	I	Power-down mode
5	AGND	-	Analog ground	17	MCLK	I	Master clock input
6	AINL+	I	Analog signal input (L channel +)	18	SCLK	I/O	Serial data clock
7	AINL-	I	Analog signal input (L channel -)	19	LRCK	I	Input/Output channel clock
8	TST1	I/O	Test mode setting 1	20	FSYNC	I/O	Frame synch. clock
9	HPFE		HPF on/off	21	SDATA	O	Serial data output
10	TST2	I/O	Test mode setting 2	22	CMODE	I	Master clock select
11	TST3	I/O	Test mode setting 3	23	SMODE1	I	Interface clock select 1
12	VD	-	Digital power supply	24	VB	-	Digital power supply

● HD6417709F80B (XV250B00) CPU

DM: IC100

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	MD1	I	System clock	105	CKE/PTK[5]	I/O	CK enable (SDRAM)/ I/O port K
2	MD2	I		106	RAS3L/PTJ[0]	I/O	RAS/ I/O port J
3	Vcc (RTC)	-	Power supply (3.3 V)	107	RAS2L/PTJ[1]	I/O	RAS/ I/O port J
4	XTAL2	I	Clock	108	CASLL/CAS/PTJ[2]	I/O	CAS (DRAM)/CAS (SDRAM)/ I/O port J
5	EXTAL2	O	Clock	109	Vss	-	Ground (0 V)
6	Vss (RTC)	-	Ground (0 V)	110	CASLH/PTJ[3]	I/O	CAS (DRAM)/ I/O port J
7	NMI	I	Interrupt request	111	Vcc	-	Power supply (3.3 V)
8	IRQ0/IRL0/PTH[0]	I	Interrupt request	112	CASHL/PTJ[4]	I/O	CAS (DRAM)/ I/O port J
9	IRQ1/IRL1/PTH[1]	I		113	CASHH/PTJ[5]	I/O	CAS (DRAM)/ I/O port J
10	IRQ2/IRL2/PTH[2]	I		114	DACK0/PTD[5]	I/O	DMAC/ I/O port D
11	IRQ3/IRL3/PTH[3]	I		115	DACK1/PTD[7]	I/O	DMAC/ I/O port D
12	IRQ4/PTH[4]	I		116	CAS2L/PTE[6]	I/O	CAS (DRAM)/ I/O port E
13	D31/PTB[7]	I/O	Data bus/ I/O port B	117	CAS2H/PTE[3]	I/O	CAS (DRAM)/ I/O port E
14	D30/PTB[6]	I/O		118	RAS3U/PTE[2]	I/O	RAS/ I/O port E
15	D29/PTB[5]	I/O		119	RAS2U/PTE[1]	I/O	RAS/ I/O port E
16	D28/PTB[4]	I/O		120	PTE[0]	I/O	I/O port E
17	D27/PTB[3]	I/O		121	BACK	O	System clock
18	D26/PTB[2]	I/O		122	BREQ	I	System clock
19	Vss	-	Ground (0 V)	123	WAIT	I	Bus control
20	D25/PTB[1]	I/O	Interrupt request	124	RESETM	I	Reset
21	Vcc	-	Power supply (3.3 V)	125	PTH[5]/ADTRG	I	I/O port H/Analog
22	D24/PTB[0]	I/O	Data bus/ I/O port B	126	IOIS16/PTG[7]	I	Right protect/Input port G
23	D23/PTA[7]	I/O	Data bus/ I/O port A	127	PTG[6]	I	I/O port G
24	D22/PTA[6]	I/O		128	PTG[5]	I	
25	D21/PTA[5]	I/O		129	PTG[4]	I	
26	D20/PTA[4]	I/O		130	PTG[3]	I	
27	Vss	-	Ground (0 V)	131	PTG[2]	I	
28	D19/PTA[3]	I/O	Data bus/ I/O port A	132	Vss	-	Ground (0 V)
29	Vcc	-	Power supply (3.3 V)	133	PTG[1]	I	I/O port G
30	D18/PTA[2]	I/O	Data bus/ I/O port A	134	Vcc	-	Power supply (3.3 V)
31	D17/PTA[1]	I/O		135	PTG[0]	I	I/O port G
32	D16/PTA[0]	I/O		136	PTF[7]/PINT[15]	I	I/O port F/Port Interrupt request
33	Vss	-	Ground (0 V)	137	PTF[6]/PINT[14]	I	
34	D15	I/O	Data bus	138	PTF[5]/PINT[13]	I	
35	Vcc	-	Power supply (3.3 V)	139	PTF[4]/PINT[12]	I	
36	D14	I/O	Data bus	140	PTF[3]/PINT[11]	I	
37	D13	I/O		141	PTF[2]/PINT[10]	I	
38	D12	I/O		142	PTF[1]/PINT[9]	I	
39	D11	I/O		143	PTF[0]/PINT[8]	I	
40	D10	I/O		144	MD0	I	System clock
41	D9	I/O		145	Vcc (PLL1)	-	Power supply (3.3 V)
42	D8	I/O		146	CAP1	-	Clock
43	D7	I/O		147	Vss (PLL1)	-	Ground (0 V)
44	D6	I/O		148	Vss (PLL2)	-	Ground (0 V)
45	Vss	-	Ground (0 V)	149	CAP2	-	Clock
46	D5	I/O	Data bus	150	Vcc (PLL2)	-	Power supply (3.3 V)
47	Vcc	-	Power supply (3.3 V)	151	PTH[6]	I	I/O port H
48	D4	I/O	Data bus	152	Vss	-	Ground (0 V)
49	D3	I/O		153	Vss	-	Ground (0 V)
50	D2	I/O		154	Vcc	-	Power supply (3.3 V)
51	D1	I/O		155	XTAL	O	Clock
52	D0	I/O		156	EXTAL	I	Clock
53	A0	O	Address bus	157	STATUS[0]/PTJ[6]	I/O	System clock
54	A1	O		158	STATUS[1]/PTJ[7]	I/O	
55	A2	O		159	TCLK/PTH[7]	I/O	Timer
56	A3	O		160	IRQOUT	O	Interrupt request
57	Vss	-	Ground (0 V)	161	Vss	-	Ground (0 V)
58	A4	O	Address bus	162	CKIO	I/O	Clock
59	Vcc	-	Power supply (3.3 V)	163	Vcc	-	Power supply (3.3 V)
60	A5	O	Address bus	164	TxD0/SCPT[0]		
61	A6	O		165	SCK0/SCPT[1]		
62	A7	O		166	TxD1/SCPT[2]	O	Forward data/Output port for SCI
63	A8	O		167	SCK1/SCPT[3]	I/O	Serial clock/ I/O port for SCI
64	A9	O		168	TxD2/SCPT[4]	O	Forward data/Output port for SCI
65	A10	O		169	SCK2/SCPT[5]	I/O	Serial clock/ I/O port for SCI
66	A11	O		170	RTS2/SCPT[6]	I/O	Transmit request/ I/O port for SCI
67	A12	O		171	RxD0/SCPT[0]		
68	A13	O		172	RxD1/SCPT[2]	I	Reception data/Input port for SCI
69	Vss	-	Ground (0 V)	173	Vss	-	Ground (0 V)
70	A14	O	Address bus	174	RxD2/SCPT[4]	I	Reception data/Input port for SCI
71	Vcc	-	Power supply (3.3 V)	175	Vcc	-	Power supply (3.3 V)
72	A15	O	Address bus	176	CTS2/IRQ5/SCPT[7]	I	Transmit clear/Interrupt request/Input port for SCI
73	A16	O		177	PTC[7]/PINT[7]	I/O	I/O port C/Interrupt request
74	A17	O		178	PTC[6]/PINT[6]	I/O	
75	A18	O		179	PTC[5]/PINT[5]	I/O	
76	A19	O		180	PTC[4]/PINT[4]	I/O	
77	A20	O		181	Vss	-	Ground (0 V)
78	A21	O		182	WAKEUP/PTD[3]	I/O	Interrupt request/ I/O port D
79	Vss	-	Ground (0 V)	183	Vcc	-	Power supply (3.3 V)
80	A22	O	Address bus	184	PTD[2]/RESETOUT	I/O	I/O port D/Reset
81	Vcc	-	Power supply (3.3 V)	185	PTC[3]/PINT[3]	I/O	I/O port C/Interrupt request
82	A23	O	Address bus	186	PTC[2]/PINT[2]	I/O	
83	Vss	-	Ground (0 V)	187	PTC[1]/PINT[1]	I/O	
84	A24	O	Address bus	188	PTC[0]/PINT[0]	I/O	
85	Vcc	-	Power supply (3.3 V)	189	DRAK0/PTD[1]	I/O	DMA request/ I/O port D
86	A25	O	Address bus	190	DRAK1/PTD[0]	I/O	DMA request/ I/O port D
87	BS/PTK[4]	I/O	Bus control/ I/O port K	191	DREQ0/PTD[4]	I	DMA request/ I/O port D
88	RD	O	Read strobe	192	DREQ1/PTD[6]	I	DMA request/ I/O port D
89	WE0/DQMLL	O	Select signal/DQM (SDRAM)	193	RESETP	I	System clock
90	WE1/DQMLU/WE	O	Select signal/DQM (SDRAM)/PCMCIA WE	194	CA	I	System clock
91	WE2/DQMUL/ICIORD/PTK[6]	I/O	Select signal/DQM (SDRAM)/PCMCIA I/O read/ I/O port K	195	MD3	I	System clock
92	WE3/DQMUU/ICIOWR/PTK[7]	I/O	Select signal/DQM (SDRAM)/PCMCIA I/O write/ I/O port K	196	MD4	I	System clock
93	RD/WR	O	Read/Write signal	197	MD5	I	System clock
94	PTE[7]	I/O	I/O port E	198	AVss	-	Analog ground (0 V)
95	Vss	-	Ground (0 V)	199	AN[0]/PTL[0]	I	A/D change input/Input port L
96	CS0	O	Chip select	200	AN[1]/PTL[1]	I	
97	Vcc	-	Power supply (3.3 V)	201	AN[2]/PTL[2]	I	
98	CS2/PTK[0]	I/O	Chip select/ I/O port K	202	AN[3]/PTL[3]	I	
99	CS3/PTK[1]	I/O	Chip select/ I/O port K	203	AN[4]/PTL[4]	I	
100	CS4/PTK[2]	I/O	Chip select/ I/O port K	204	AN[5]/PTL[5]	I	
101	CS5/CE1A/PTK[3]	I/O	Chip select/CE1/ I/O port K	205	AVcc	-	Analog power supply (3.3 V)
102	CS6/CE1B	O	Chip select/CE1	206	AN[6]/DA[1]/PTL[6]	I/O	A/D change input/D/A change output/Input port L
103	CE2A/PTE[4]	I/O	Chip enable/ I/O port E	207	AN[7]/DA[0]/PTL[7]	I/O	
104	CE2B/PTE[5]	I/O	Chip enable/ I/O port E	208	AVss	-	Analog ground (0 V)

● **TC203C760HF-002** (XS725A00) **SWP30B** (AWM Tone Generator coped with MEG) Standard Wave Processor

DM: IC400 (PSR-2000 only)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss		(Ground)	121	VSS		(Ground)
2	CA0	I	Address bus of internal register	122	HMD0	I/O	Wave memory data bus (Upper data memory)
3	CA1	I		123	HMD1	I/O	
4	CA2	I		124	HMD2	I/O	
5	CA3	I		125	HMD3	I/O	
6	CA4	I		126	HMD4	I/O	
7	CA5	I		127	HMD5	I/O	
8	CA6	I		128	HMD6	I/O	
9	CA7	I		129	HMD7	I/O	
10	CA8	I		130	HMD8	I/O	
11	CA9	I		131	HMD9	I/O	
12	CA10	I		132	HMD10	I/O	
13	CA11	I		133	HMD11	I/O	
14	VSS		(Ground)	134	HMD12	I/O	
15	CD0	I/O	Data bus of internal register	135	HMD13	I/O	
16	CD1	I/O		136	HMD14	I/O	
17	CD2	I/O		137	HMD15	I/O	
18	CD3	I/O		138	VSS		(Ground)
19	CD4	I/O		139	HMA0	O	Wave memory address bus (Upper 16 bits)
20	CD5	I/O		140	HMA1	O	
21	CD6	I/O		141	HMA2	O	
22	CD7	I/O		142	HMA3	O	
23	CD8	I/O		143	HMA4	O	
24	CD9	I/O		144	HMA5	O	
25	CD10	I/O		145	HMA6	O	
26	CD11	I/O		146	HMA7	O	
27	CD12	I/O		147	HMA8	O	
28	CD13	I/O		148	HMA9	O	
29	CD14	I/O		149	HMA10	O	
30	VDD		(Power supply)	150	VSS		(Ground)
31	VSS		(Ground)	151	VDD		(Power supply)
32	CD15	I/O		152	HMA11	O	
33	CSN	I	Chip select	153	HMA12	O	
34	WRN	I	Write strobe	154	HMA13	O	
35	RDN	I	Read strobe	155	HMA14	O	
36	VDD		(Power supply)	156	HMA15	O	
37	SYSH0	O	NSYS/LNSYS upper 16 bits	157	HMA16	O	
38	SYSH1	O		158	HMA17	O	
39	SYSH2	O		159	HMA18	O	
40	SYSH3	O		160	HMA19	O	
41	SYSH4	O		161	HMA20	O	
42	SYSH5	O		162	HMA21	O	
43	SYSH6	O		163	HMA22	O	
44	SYSH7	O		164	HMA23	O	
45	KONO0	O	Key on data	165	HMA24	O	
46	KONO1	O		166	VSS		(Ground)
47	KONO2	O		167	MRASN	O	RAS when DRAM(s) is connected to wave memory
48	KONO3	O		168	MCASN	O	CAS when DRAM(s) is connected to wave memory
49	VSS		(Ground)	169	MOEN	O	Wave memory output enable
50	SYSL0	I/O	NSYS input/LNSYS output lower 8 bits	170	MWEN	O	Wave memory write enable
51	SYSL1	I/O		171	VSS		(Ground)
52	SYSL2	I/O		172	LMD0	I/O	Wave memory data bus (Lower data memory)
53	SYSL3	I/O		173	LMD1	I/O	
54	SYSL4	I/O		174	LMD2	I/O	
55	SYSL5	I/O		175	LMD3	I/O	
56	SYSL6	I/O		176	LMD4	I/O	
57	SYSL7	I/O		177	LMD5	I/O	
58	KONI0	I	Key on data input (Power supply) (Ground)	178	LMD6	I/O	
59	KONI1	I		179	LMD7	I/O	
60	VDD	I		180	VDD		(Power supply)
61	VSS			181	VSS		(Ground)
62	KONI2	I		182	LMD8	I/O	
63	KONI3	I		183	LMD9	I/O	
64	DAC0	O	DAC output	184	LMD10	I/O	
65	DAC1	O		185	LMD11	I/O	
66	WCLK	O	DAC0/DAC1 word clock	186	LMD12	I/O	
67	MELO0	O	MEL wave data output	187	LMD13	I/O	
68	MELO1	O		188	LMD14	I/O	
69	MELO2	O		189	LMD15	I/O	
70	MELO3	O		190	VSS		(Ground)
71	MELO4	O		191	LMA0	O	Wave memory address bus (Lower data memory)
72	MELO5	O		192	LMA1	O	
73	MELO6	O		193	LMA2	O	
74	MELO7	O		194	LMA3	O	
75	VDD		(Power supply)	195	LMA4	O	
76	ADLR	O	ADC word clock	196	LMA5	O	
77	MELI0	I	MEL wave data input	197	LMA6	O	
78	MELI1	I		198	LMA7	O	
79	MELI2	I		199	LMA8	O	
80	MELI3	I		200	LMA9	O	
81	MELI4	I		201	LMA10	O	
82	MELI5	I		202	LMA11	O	
83	MELI6	I		203	VSS		(Ground)
84	MELI7	I		204	LMA12	O	
85	VSS		(Ground)	205	LMA13	O	
86	RCASN	O	DRAM column address strobe	206	LMA14	O	
87	RA8	O	DRAM address bus	207	LMA15	O	
88	RA7	O		208	LMA16	O	
89	RA6	O		209	LMA17	O	
90	VDD		(Power supply)	210	VDD		(Power supply)
91	VSS		(Ground)	211	VSS		(Ground)
92	RA5	O		212	LMA18	O	
93	RA4	O		213	LMA19	O	
94	RA3	O		214	LMA20	O	
95	RA2	O		215	LMA21	O	
96	RA1	O		216	LMA22	O	
97	RA0	O		217	LMA23	O	
98	RRASN	O	DRAM row address strobe	218	LMA24	O	
99	RWEN	O	DARM write enable	219	VSS		(Ground)
100	VSS		(Ground)	220	SYO	O	Sync. signal for master clock
101	RD7	I/O	DRAM data bus	221	SYOD	O	Sync. signal for HCLK/QCLK
102	RD6	I/O		222	QCLK	O	1/12 master clock (64 Fs)
103	RD5	I/O		223	HCLK	O	1/6 master clock (128 Fs)
104	RD4	I/O		224	CK256	O	1/3 master clock (256 Fs)
105	RD3	I/O		225	SYSCLK	O	1/2 master clock (384 Fs)
106	RD2	I/O		226	VDD		(Power supply)
107	RD1	I/O		227	SYI	I	Sync. clock
108	RD0	I/O		228	MCLKI	I	Master clock input
109	VSS		(Ground)	229	MCLKO	O	Master clock output
110	RD17	I/O		230	VDD		(Power supply)
111	RD16	I/O		231	XIN	I	Crystal osc. input
112	RD15	I/O		232	XOUT	O	Crystal osc. output
113	RD14	I/O		233	VSS		(Ground)
114	RD13	I/O		234	ICN	I	Initial clear
115	RD12	I/O		235	CHIP2	I	2 chips mode enable
116	RD11	I/O		236	SLAVE	I	Master/Slave select when 2 chips mode
117	RD10	I/O		237	TESTON	I	Test pin
118	RD9	I/O		238	ACIN	I	
119	RD8	I/O		239	DCTEST	I	
120	VDD		(Power supply)	240	VDD		(Power supply)

● **HG73C205AFD** (XU947C00) **SWX00B** (Tone Generator)

DM: IC801 (PSR-1000)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	ICN	I	Initial clear	85	CMA3	O	Program address bus
2	RFCLKI	I	PLL Clock	86	CMA8	O	Program address bus
3	TM2	I	PLL Control	87	CMA2	O	Program address bus
4	AVDD_PLL		Power supply	88	CRD	O	read signal
5	AVSS_PLL		Ground	89	CMA1	O	Program address bus
6	MODE0	I	SWX dual mode	90	CUB	O	high byte effective signal
7	VCC7		Power supply	91	VCC91		Power supply
8	GND8		Ground	92	GHND92		Ground
9	XIN	I	crystal oscillator	93	CS1	O	CS signal
10	XOUT	O	crystal oscillator	94	CMA0	O	Program address bus
11	MODE1	I	SWX separate mode	95	CLB	O	low byte effective signal
12	TEST0	I	TEST pin	96	CMA12	O	Program address bus
13	TESTON	I	TEST pin	97	CMA11	O	Program address bus
14	AN0-P40	I	A/D converter	98	CMA10	O	Program address bus
15	AN1-P41	I	A/D converter	99	CMA9	O	Program address bus
16	AN2-P42	I	A/D converter	100	GND100		Ground
17	AN3-P43	I	A/D converter	101	CWE	O	write signal
18	AVDD_AN		Power supply	102	CMA16	O	Program address bus
19	AVSS_AN		Ground	103	CMA15	O	Program address bus
20	TXD0	O	for MIDI or TO-HOST	104	CMA14	O	Program address bus
21	TXD1	O	for MIDI	105	CMA13	O	Program address bus
22	EXCLK	I	Crystal oscillator	106	CMD8	I/O	Program memory Data bus
23	SMD11	I/O	Wave memory data bus	107	CMD7	I/O	Program memory Data bus
24	SMD4	I/O	Wave memory data bus	108	CMD9	I/O	Program memory Data bus
25	SMD3	I/O	Wave memory data bus	109	CMD6	I/O	Program memory Data bus
26	SMD12	I/O	Wave memory data bus	110	CMD10	I/O	Program memory Data bus
27	SMD10	I/O	Wave memory data bus	111	CMD5	I/O	Program memory Data bus
28	SMD5	I/O	Wave memory data bus	112	CMD11	I/O	Program memory Data bus
29	SMD2	I/O	Wave memory data bus	113	CMD4	I/O	Program memory Data bus
30	SMD13	I/O	Wave memory data bus	114	CMD12	I/O	Program memory Data bus
31	SMD9	I/O	Wave memory data bus	115	CMD3	I/O	Program memory Data bus
32	SMD6	I/O	Wave memory data bus	116	CMD13	I/O	Program memory Data bus
33	SMD1	I/O	Wave memory data bus	117	CMD2	I/O	Program memory Data bus
34	SMD14	I/O	Wave memory data bus	118	CMD14	I/O	Program memory Data bus
35	VCC35		Power supply	119	VCC119		Power supply
36	GND36		Ground	120	GND115		Ground
37	SMD8	I/O	Wave memory data bus	121	CMD1	I/O	Program memory Data bus
38	SMD7	I/O	Wave memory data bus	122	CMD15	I/O	Program memory Data bus
39	SMD0	I/O	Wave memory data bus	123	CMD0	I/O	Program memory Data bus
40	SMD15	I/O	Wave memory data bus	124	CMA21	O	Program address bus
41	SOE	O	read signal	125	PDT15	I/O	SWX access data bus
42	SWE	O	write signal	126	PDT14	I/O	SWX access data bus
43	SRAS	O	RAS signal	127	PDT13	I/O	SWX access data bus
44	SCAS	O	CAS signal	128	PDT12	I/O	SWX access data bus
45	REFRESH	O	REFRESH signal	129	PDT11	I/O	SWX access data bus
46	CS0	O	CS signal	130	PDT10	I/O	SWX access data bus
47	SMA0	O	Memory address bus	131	PDT9	I/O	SWX access data bus
48	SMA16	O	Memory address bus	132	PDT8	I/O	SWX access data bus
49	VCC49		Power supply	133	VCC133		Power supply
50	GND50		Ground	134	GND134		Ground
51	SMA1	O	Memory address bus	135	PDT7	I/O	SWX access data bus
52	SMA15	O	Memory address bus	136	PDT6	I/O	SWX access data bus
53	SMA2	O	Memory address bus	137	PDT5	I/O	SWX access data bus
54	SMA14	O	Memory address bus	138	PDT4	I/O	SWX access data bus
55	SMA3	O	Memory address bus	139	PDT3	I/O	SWX access data bus
56	SMA13	O	Memory address bus	140	PDT2	I/O	SWX access data bus
57	SMA4	O	Memory address bus	141	PDT1	I/O	SWX access data bus
58	SMA12	O	Memory address bus	142	PDT0	I/O	SWX access data bus
59	SMA5	O	Memory address bus	143	VCA143		Power supply
60	GND60		Ground	144	GND144		Ground
61	VCC61		Power supply	145	PAD2	I	SWX access address bus
62	SMA11	O	Memory address bus	146	PAD1	I	SWX access address bus
63	SMA6	O	Memory address bus	147	PAD0	I	SWX access address bus
64	SMA10	O	Memory address bus	148	VCC148		Power supply
65	SMA7	O	Memory address bus	149	GND149		Ground
66	SMA9	O	Memory address bus	150	PCS	I	Chip select
67	SMA17	O	Memory address bus	151	PWR	I	write enable
68	SMA8	O	Memory address bus	152	PRD	I	read enable
69	SMA18	O	Memory address bus	153	RXD0	I	for Midi or TO-HOST
70	SMA19	O	Memory address bus	154	RXD1	I	for Midi or Key scan
71	SMA20	O	Memory address bus	155	SCLKI	I	EXT Clock
72	SMA21	O	Memory address bus	156	ADIN	I	A/D converter
73	SMA22	O	Memory address bus	157	ADLR	O	A/D converter LR clock
74	SMA23	O	Memory address bus	158	DO0	O	DAC
75	CMA20	O	Program address bus	159	DO1	O	DAC
76	CMA19	O	Program address bus	160	SYSCLK	O	1/2 clock
77	VCC77		Power supply	161	VCC161		Power supply
78	GND78	O	Ground	162	GND162		Ground
79	CMA18	O	Program address bus	163	WCLK	O	for DAC LR clock
80	CMA17	O	Program address bus	164	QCLK	O	1/12 clock
81	CMA5	O	Program address bus	165	BCLK	O	IIS-DAC clock
82	CMA6	O	Program address bus	166	SYI	I	Synch signal
83	CMA4	O	Program address bus	167	IRQ0	I	Interrupt request
84	CMA7	O	Program address bus	168	NMI	I	Interrupt request

● **YSS236-F** (XT013A00) **VOP3**

DM: IC401 (PSR-2000 only)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	VSS		Power supply	81	SO7	O	
2	WA17	O		82	SO6	O	Serial output
3	WA16	O		83	SO5	O	
4	WA15	O		84	VDD		Ground
5	WA14	O		85	VSS		Power supply
6	WA13	O	External memory address bus	86	SO4	O	
7	WA12	O		87	SO3	O	
8	WA11	O		88	SO2	O	Serial output
9	WA10			89	SO1	O	
10	VDD		Ground	90	SO0	O	
11	VSS		Power supply	91	WDCK	O	Data enable for DAC
12	WA09	O		92	SWPKON	O	SWP00 format key on output
13	WA08	O		93	IRQN	O	EG interrupt
14	WA07	O		94	VDD		Ground
15	WA06	O		95	VSS		Power supply
16	WA05	O	External memory address bus	96	XTAL_I	I	Quartz crystal terminal
17	WA04	O		97	XTAL_O	O	Quartz crystal terminal
18	WA03	O		98	MCLK	O	Oscillate clock output
19	WA02	O		99	VDD		Ground
20	VDD		Ground	100	VSS		Power supply
21	VSS		Power supply	101	MICN	I	Initial clear
22	WA01	O	External memory address bus	102	CLKIN	I	Master clock input
23	WA00	O		103	SYWIN	I	Sync.signal input
24	WEN	O	External memory control (WEN)	104	SYW	O	Sync.signal output
25	OEN	O	External memory control (OEN)	105	SYWD	O	Sync.signal output
26	RASN	O	External memory control (RASN)	106	VDD		Ground
27	CASN	O	External memory control (CASN)	107	VSS		Power supply
28	CEN	O	External memory control (CEN)	108	CLKO	O	For test (512 fs output)
29	VDD		Ground	109	WCLK	O	2 times sync.clock output (256 fs)
30	VSS		Power supply	110	HCLK	O	4 times sync.clock output (128 fs)
31	WD19	I/O		111	QCLK	O	8 times sync.clock output (64 fs)
32	WD18	I/O		112	TSTCI	I	PLL test input
33	WD17	I/O	External memory data bus	113	VDD		Ground
34	WD16	I/O		114	VSS		Power supply
35	WD15	I/O		115	(NC)		
36	WD14	I/O		116	VDD(PLL)		
37	VDD		Ground	117	CPO	O	PLL control output
38	VSS		Power supply	118	CPIN	I	PLL control input
39	WD13	I/O		119	REF	I	PLL control input
40	WD12	I/O		120	VSS(PLL)		
41	WD11	I/O		121	(NC)		
42	WD10	I/O	External memory data bus	122	VDD		Ground
43	WD09	I/O		123	VSS		Power supply
44	WD08	I/O		124	TSTCS	I	PLL test input
45	WD07	I/O		125	CA6	I	
46	VDD		Ground	126	CA5	I	CPU address bus
47	VSS		Power supply	127	CA4	I	
48	WD06	I/O		128	CA3	I	
49	WD05	I/O		129	CA2	I	
50	WD04	I/O		130	VDD		Ground
51	WD03	I/O	External memory data bus	131	VSS		Power supply
52	WD02	I/O		132	CA1	I	CPU address bus
53	WD01	I/O		133	CA0	I	Lo/Hi select in 8 bits write
54	WD00	I/O		134	CSN	I	Chip select
55	VDD		Ground	135	RDN	I	Register read
56	VSS		Power supply	136	WRN	I	Register write
57	TST2	O		137	BTYP		Data bus type select
58	TST1	O	Test output	138	VDD		Ground
59	TST0	O		139	VSS		Power supply
60	MS	I	Memory select	140	CD15	I/O	
61	LRCLK	O	LR clock for ADC	141	CD14	I/O	
62	SI7	I	Serial input	142	CD13	I/O	CPU data bus
63	SI6	I		143	CD12	I/O	
64	VDD		Ground	144	CD11	I/O	
65	VSS		Power supply	145	VDD		Ground
66	SI5	I		146	VSS		Power supply
67	SI4	I		147	CD10	I/O	
68	SI3	I	Serial input	148	CD09	I/O	
69	SI2	I		149	CD08	I/O	CPU data bus
70	SI1	I		150	CD07	I/O	
71	SI0	I		151	CD06	I/O	
72	DB1	I	Output bit type select for DAC	152	CD05	I/O	
73	DB0	I		153	VDD		Ground
74	VDD		Ground	154	VSS		Power supply
75	VSS		Power supply	155	CD04	I/O	
76	ODFM	I	Output mode select for DAC	156	CD03	I/O	
77	OFS3	I		157	CD02	I/O	CPU data bus
78	OFS2	I	Serial output format select	158	CD01	I/O	
79	OFS1	I		159	CD00	I/O	
80	OFS0	I		160	VDD		Ground

● **µPD789022GB-A15-8E** (XZ560100) **CPU**

MKS5F: IC1

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	P12	I/O	Port 1	23	P32/INTP2/CPT2	I/O	Port 3/External interrupt input/Capture edge input
2	P11	I/O		24	P31/INTP1	I/O	Port 3/External interrupt input
3	P10	I/O		25	P30/INTP0	I/O	
4	P47/KR7	I/O	Port 4/Key return signal detection input	26	P22/RXD/SI0	I/O	Port 2/Asynchronous serial interface serial data input/Serial interface serial data input
5	P46/KR6	I/O		27	P21/TXD/SO0	I/O	Port 2/Asynchronous serial interface serial data output/Serial interface serial data output
6	P45/KR5	I/O		28	P20/ASCK//SCK0	I/O	Port 2/Asynchronous serial interface serial clock input/Serial interface serial clock
7	P44/KR4	I/O		29	P07	I/O	Port 0
8	P43/KR3	I/O		30	P06	I/O	
9	P42/KR2	I/O		31	P05	I/O	
10	P41/KR1	I/O		32	P04	I/O	
11	P40/KR0	I/O		33	P03	I/O	
12	NC			34	P02	I/O	
13	IC		Internally connected (N.C.)	35	P01	I/O	
14	X2		Clock	36	P00	I/O	
15	X1	I		37	NC		
16	VSS0		Ground	38	VDD1		Power supply
17	VDD0		Power supply	39	VSS1		Ground
18	/RESET	I	System reset	40	P17	I/O	Port 1
19	P53	I/O	Port 5	41	P16	I/O	
20	P52	I/O		42	P15	I/O	
21	P51/TO2	I/O	Port 5/16-bit timer output	43	P14	I/O	
22	P50/TI0/TO0	I/O	Port 5/External count clock input to 8-bit timer/8-bit timer output	44	P13	I/O	

● **S1D13305F00B100** (XQ595A00) **LCDC** (LCD Controller)

DM: IC500

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	VA5	O	VRAM address bus	31	XD2	O	Data bus output for 4 bit dot
2	VA4	O		32	XD1	O	
3	VA3	O		33	XD0	O	
4	VA2	O		34	XECL	O	S driver enable, chain clock
5	VA1	O		35	XSCL	O	Data bus shift clock
6	VA0	O		36	Vss	-	Ground
7	/VWR	O	VRAM read/write	37	LP	O	X driver latch pulse
8	/VCE	O	Memory control	38	WF	O	Frame signal for X/Y driver
9	/VRD	-	Not used	39	YDIS	O	Power down signal for displaying off mode
10	/RES	I	Initial clear	40	YD	O	Scan start signal
11	NC	-	Not used	41	YSCL	O	Scan shift clock
12	NC	-	Not used	42	VD7	I/O	VRAM data bus
13	/RD	I	Read strobe	43	VD6	I/O	
14	/WR	I	Write strobe	44	VD5	I/O	
15	SEL2	I	Bus select	45	VD4	I/O	
16	SEL1	I	Bus select	46	VD3	I/O	
17	OSC1	I	Clock	47	VD2	I/O	
18	OSC2	O	Clock	48	VD1	I/O	
19	/CS	I	Chip select	49	VD0	I/O	
20	A0	I	Data mode select	50	VA15	O	VRAM address bus
21	Vdd	-	Power supply	51	VA14	O	
22	D0	I/O	Data bus	52	VA13	O	
23	D1	I/O		53	VA12	O	
24	D2	I/O		54	VA11	O	
25	D3	I/O		55	VA10	O	
26	D4	I/O		56	VA9	O	
27	D5	I/O		57	VA8	O	
28	D6	I/O		58	VA7	O	
29	D7	I/O		59	VA6	O	
30	XD3	O	Data bus output for 4 bit dot	60	NC	-	Not used

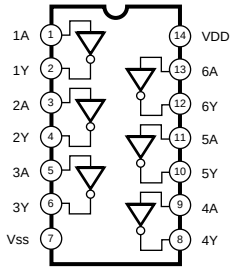
● **AD1854JRSRL** (XY782A00) **DAC** (Digital to Analog Converter)

DM: IC700

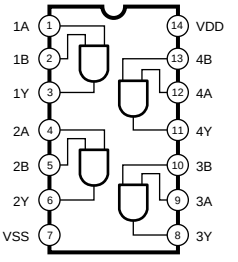
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	DGND	I	Digital Ground	15	AGND	I	Analog Ground
2	MCLK	I	Master Clock Input. Connect to an external clock source at either 256, 384 or 512 Fs.	16	OUTL-	O	Left Channel Negative line level analog output.
3	CLATCH	I	Latch input for control data. This input is rising-edge sensitive.	17	OUTL+	O	Left Channel Positive line level analog output.
4	CCLK	I	Control clock input for control data. Control input data must be valid on the rising edge of CCLK. CCLK may be continuous or gated.	18	AVDD	I	Analog Power Supply. Connect to analog 5 V supply.
				19	FILTB	O	Filter Capacitor connection, connect 10 µF capacitor to AGND.
5	CDATA	I	Serial control input, MSB first, containing 16 bits of unsigned data per channel. Used for specifying channel-specific attenuation and mute.	20	IDPM1	I	Input serial data port mode control one. With IDPM0, defines one of four serial modes.
6	384//256	I	Selects the master clock mode as either 384 times the intended sample frequency (HI) or 256 times the intended sample frequency (LO). The state of this input should be hardwired to logic HI or logic LO, or may be changed while the AD1854 is in power-down/reset. It must not be changed while the AD1854 is operational.	21	IDPM0	I	Input serial data port mode control zero. With IDPM1, defines one of four serial modes.
				22	ZEROL	O	Left Channel Zero Flag Output. This pin goes HI when Left Channel has no signal input for more than 1024 LR Clock Cycles.
7	X2MCLK	I	Selects internal clock doubler (LO) or internal clock = MCLK (HI).	23	MUTE	I	Mute. Assert HI to mute both stereo analog outputs. Deassert LO for normal operation.
8	ZEROR	O	Right Channel Zero Flag Output. This pin goes HI when Right Channel has no signal input for more than 1024 LR Clock Cycles.	24	/PD//RST	I	/Power-Down//Reset. The AD1854 is placed in a low power consumption mode when this pin is held LO. The AD1854 is reset on the rising edge of this signal. The serial control port registers are reset to the default values. Connect HI for normal operation.
9	DEEMP	I	De-Emphasis. Digital de-emphasis is enabled when this input signal is HI. This is used to impose a 50 µs/15 µs response characteristic on the output audio spectrum at an assumed 44.1 kHz sample rate.	25	L//RCLK	I	Left//Right clock input for input data. Must run continuously.
10	96//48	I	Selects 48 kHz (LO) or 96 kHz Sample Frequency Control.	26	BCLK	I	Bit clock input for input data. Need not run continuously; may be gated or used in a burst fashion.
11	AGND	I	Analog Ground				
12	OUTR+	O	Right Channel Positive line level analog output.				
13	OUTR-	O	Right Channel Negative line level analog output.	27	SDATA	I	Serial input, MSB first, containing two channels of 16, 18, 20, and 24 bits of twos complement data per channel.
14	FILTR	O	Voltage Reference Filter Capacitor Connection. Bypass and decouple the voltage reference with parallel 10 µF and 0.1 µF capacitors to the AGND.	28	DVDD	I	Digital Power Supply Connect to digital 5 V supply.

■ IC BLOCK DIAGRAM

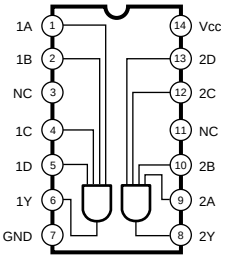
● **SN74HCU04NSR** (XW842A00)
SN74HCU04N (IG142250)
Hex Inverter
DM: IC510, 511
AM: IC301



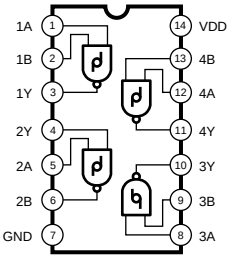
● **HD74LV08AFPEL** (IS000800)
Quad 2 Input AND
DM: IC101



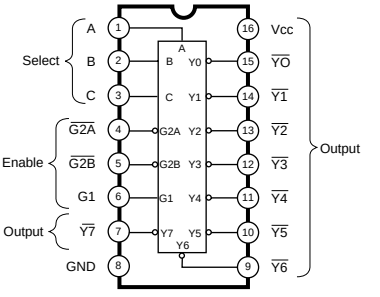
● **HD74LV21ATELL** (X0010A00)
Dual 4 Input AND
DM: IC310



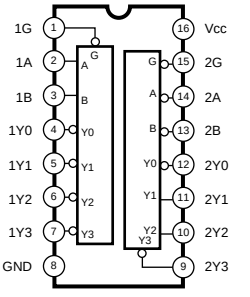
● **SN74HC132NSR** (XW792A00)
MM74HC132SJX (XY352A00)
Quad 2 Input NAND
DM: IC914



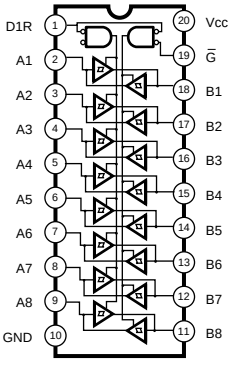
● **SN74HCT138NSR** (XY865A00)
3 to 8 Demultiplexer
DM: IC600



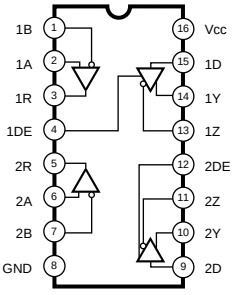
● **HD74LVC139FPEL** (XS048A00)
Dual 2 to 4 Demultiplexer
DM: IC308



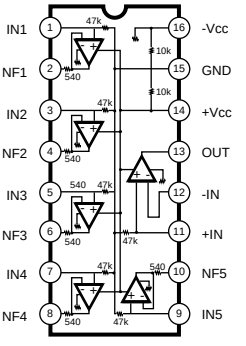
● **HD74LV245ATELL** (XW744A00)
74LVC245APW (XZ286A00)
TC74VHCT245AFT (XT744A00)
Octal 3-State Bus Transceiver
DM: IC103, 104, 301-303, 304-306, 911



● **SN75C1168N** (XU463A00)
Line Driver/Receiver
AM: IC307



● **M5227P** (XF751A00)
5-Band Graphic Equalizer
AM: IC104, 105

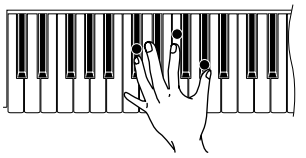


■ TEST PROGRAM

1. Preparation

1) PA-300 (AC adaptor) is used.
2) The volume is usually moved to the use position when no volume change is required.
3) Measuring instruments: frequency counter, level meter (with JIS-C filter)
   Note: Connect a stereo plug to the [PHONES] jack at 33 ohms.
4) Jigs: foot switch (FC-4), foot volume (FC-7), MIDI cable, floppy disk (2HD & 2DD), microphone (PSR-2000 only)

2. How to enter the Test Program



While pressing the [C#2], [F2] and [G#2] keys, turn the [STANDBY/ON] switch on.

3. Proceeding through the Teat Program

When the test program is activated, the sign “TEST” is indicated on the LCD display.
Automatically performs RAM BACKUP check when entering test mode.
Select the test program item to be executed by pressing the [TEMPO-] or [TEMPO+] button.
Press the [START/STOP] button to execute testing. When the test result is OK, press the [START/STOP] button to return to the test item name on display. Proceed to the next test by pressing the [TEMPO-] or [TEMPO+] button. When the test result is OK, an asterisk (*) is added in front of its item name on display.
When the test result is NG, press the [DEMO] button or the lowest (leftmost) white key on the keyboard to return to the test item name on display and then turn off the [STANDBY/ON] switch to end the test program.

4. Test program list

No.	LCD (initial)	Test Function and Judgment criteria
1	001: Version	Displays each ROM version. ROM versions are displayed alternately on the LCD.
2	002: ROM Check1	Checks the ROMs that are connected to the CPU bus. The test results appear on the LCD. Check the LCD “ROM Check1 OK”
3	003: RAM Check1	Checks the RAMs that are connected to the CPU bus. The test results appear on the LCD. Check the LCD “RAM Check1 OK”
4	004:Flash Check1	Checks the Flash Memories that are connected to the CPU bus. The test results appear on the LCD. Check the LCD “Flash Check1 OK”
5	005: Wave ROM Check1	Checks the Wave ROMs. The test results appear on the LCD. Check the LCD “XG Wave ROM Check OK”
6	006: Wave RAM Check1	Checks the Wave RAMs. The test results appear on the LCD. Check the LCD “XG Wave RAM Check OK”
7	007: FDD Check	Checks the floppy disk drive unit. Insert the floppy disks one bye one (2HD or 2DD). The test will be executed immediately if an FD is inserted in the drive. After completing the test for one FD, replace it with another to continue the test. Displays “FDD Check OK” if the test result is OK. Displays “NO FD” and stands by for FD insertion if an FD is drawn out before completion of the test. Displays “PROTECT FD” if the write-protect switch of FD is on. Displays “UNFORMAT FD” if non-formatted FD is inserted.
9	009: Effect 2 RAM Check (PSR-2000 only)	Checks the VOP3 RAM. Outputs the sine wave (C3) MAX at the send level and MIN at the drive level. Check the sound by hearing that there is not noise or abnormal sound.
10	010: Effect 3 RAM Check	Checks the XG1 RAM. Outputs the sine wave (C3) MAX at the send level and MIN at the drive level. Check the sound by hearing that there is not noise or abnormal sound.
12	012: TG1 Check	Sequentially outputs the sine wave starting from the low keys (from C2 to G4) by switching the channel of the sound source. Check the sound by hearing that there is not noise or abnormal sound.
15	015: Pitch Check	Pitch check: Connect the frequency counter to the [PHONES] jack (33 ohm load). Outputs the sine wave at 440.0 Hz +/- 0.22 Hz. (PAN = Center) Decline quantity check of the volume: Connect the level meter (with JIS-C filter) to the [PHONES] jack. Set the [MASTER VOLUME] at MIN and check the output level. **PHONES L, R:** less than -80.0 dBm

No.	LCD (initial)	Test Function and Judgment criteria
16	016: Output R Check	Connect the level meter (with a JIS-C filter) to each terminal (PHONES, OUTPUT L/L+R, R, AUX OUT L, R). Set the [MASTER VOLUME] at MAX and check the R channel output level. (1 kHz sine wave, PAN=R) (PHONES L, R: 33 ohm load OUTPUT L/L+R, R: 10 kohm load AUX OUT L, R: 10 kohm load) **PHONES L:** less than -30.0 dBm **PHONES R:** +3.5 dBm +/-2 dB **OUTPUT L/L+R:** less than -50.0 dBm **OUTPUT R:** +13.5 dBm +/- 2 dBm (PSR-1000), +11.6 dBm +/-2 dBm (PSR-2000) **AUX OUT L:** less than -60.0 dBm **AUX OUT R:** +9.1 dBm +/- 2 dB (PSR-1000), +5.5 dBm +/- 2 dB (PSR-2000)
17	017: Output L Check	Connect the level meter (with a JIS-C filter) to each terminal (PHONES, OUTPUT L/L+R, R, AUX OUT L, R). Set the [MASTER VOLUME] at MAX and check the L channel output level. (1 kHz sine wave, PAN=L) (PHONES L, R: 33 ohm load OUTPUT L/L+R, R: 10 kohm load AUX OUT L, R: 10 kohm load) **PHONES L:** +3.5 dBm +/- 2 dB **PHONES R:** less than -30.0 dBm **OUTPUT L/L+R:** +13.5 dBm +/- 2 dBm (PSR-1000), +11.6 dBm +/- 2 dBm (PSR-2000) **OUTPUT R:** less than -50.0 dBm **AUX OUT L:** +9.1 dBm +/- 2 dB (PSR-1000), +5.5 dBm +/- 2 dB (PSR-2000) **AUX OUT R:** less than -60.0 dBm
18	018: EQ Low Check	Check the sine wave output of EQ-Low frequency at about 65.4 Hz (C1). (PAN=Center)
19	019: EQ Mid Check	Check the sine wave output of EQ-Mid frequency at about 523 Hz (C4). (PAN=Center)
20	020: EQ High Check	Check the sine wave output EQ-High frequency at about 4186 Hz (C7). (PAN=Center)
22	022: D/A Noise Check	Checks D/A converter noise. Connect the level meter (with a JIS-C filter) to each terminal (PHONES, OUTPUT L/L+R, R, AUX OUT L, R) . Set the [MASTER VOLUME] at MAX and check the noise level. **PHONES L, R:** less than -75.0 dBm **OUTPUT L/L+R, R:** less than -70.0 dBm **AUX OUT L, R:** less than -70.0 dBm
23	023: SW, LED Check	Check the switches on the panel and LED. Press the switches on the LCD as instructed. A pre-assigned note is output when the switch is pressed. (See table 1). When the switch with LED is pressed, that LED will light up. As the check result appears on the LCD when all the switches are pressed as instructed. Check that OK is displayed. For the dial check, confirm that the turning the data dial clockwise will increase the numerical value from 50 to 100 and turning it counterclockwise will reduce it from 100 to 0.
24	024: All Panel LED On Check	Check that all panel LEDs are on. (Except for the [MIC. OVER] and [MIC. SIGNAL] LEDs of PSR-2000) The 2-colors LED light up in orange.
25	025: Red LED On Check	Check that all red LEDs are on. (Except for the [MIC. OVER] LED of PSR-2000) The 2-colors LED light up in red.
26	026: Green LED On Check	Check that all green LEDs are on. (Except for the [MIC. SIGNAL] LED of PSR-2000) The 2-colors LED light up in green.
28	028: All LCD On Check	Check that all LCD dots are on.
29	029: All LCD Off Check	Check that all LCD dots are off.
31	031: LCD Brightness Check	Press the [1] to [4] switches of [ONE TOUCH SETTING] in order. The brightness of the LCD grows lighter every time a switch is pressed.
36	036: Pedal 1 Check	Connect the foot switch (FC-4) to the [FOOT PEDAL 1] jack. Check that the C3 note is output when pressing the pedal, and that the C4 note is output when releasing the pedal .
37	037: Pedal 2 Check	Connect the foot volume (FC-7) to the [FOOT PEDAL 2] jack. Check that the C3 note is output when fully pressing the pedal to the back (to maximum), and that the C4 note is output when fully pressing the pedal to the front (to minimum).
38	038: Pitch Bend Wheel Check	Checks the pitch bend wheel. First, it is checked that the [PITCH BEND] wheel is a center position. Check that the C3 note is output when rotating the [PITCH BEND] wheel to minimum from center, and that the C4 note is output when rotating it to maximum.
39	039: Modulation Wheel Check (PSR-2000 only)	Checks the modulation wheel. First, it is checked that the [MODULATION] wheel is a center position. Check that the C3 note is output when rotating the [MODULATION] wheel to minimum from center, and that the C4 note is output when rotating it to maximum.
40	040: MIDI Check	After connecting the [MIDI IN] jack and [MIDI OUT] jack with a MIDI cable, execute the test. Set the [HOST SELECT]switch to “MIDI”. Check that the C4 note is output and that the LCD displays “OK”. If there is no input after one second since signal output, it is judged NG.
41	041: TO HOST Check	Connect pin 3 to pin 5 and pin 6 to pin 8 of the [TO HOST] terminal, and execute the test. Check that the following note sounds when changing the [HOST SELECT] switch position according to the LCD indication; the LCD will display “OK”. (PC1: note C3; PC2: note C4; MAC: note C5) If there is no input after one second since signal output, it is judged NG.
42	042: MIC Check (PSR-2000 only)	Connect a microphone to the [MIC./LINE IN] jack and speak to it. Set the [MIC./LINE] select switch to [MIC.] and set the [INPUT VOLUME] at maximum. Check the voice sound by hearing that there is not unusual noise or abnormal sound.

No.	LCD (initial)	Test Function and Judgment criteria
43	043: ROM Check2	Checks the ROMs that are connected to the CPU bus. Check the LCD “ROM Check2 OK”
44	044: RAM Check2	Checks the RAMs that are connected to the CPU bus. Check the LCD “RAM Check2 OK”
45	045: Flash Check2	Checks the Flash Memories that are connected to the CPU bus. Check the LCD “Flash Check2 OK”
46	046: Wave ROM Check2	Checks the Wave ROMs. Check the LCD “XG Wave ROM Check OK”
47	047: Wave RAM Check2	Checks the Wave RAMs. Check the LCD “XG Wave RAM Check OK”
55	055: Factory Set	All the RAMs are initialized and set to the factory preset data when executing this test.
56	056: Test Exit	Exit from the test program after executing this test.

Note: 0 dBm=0.775 V

Time is required to complete the checks performed by test No. 43–47.

• Power On Reset

All the RAMs are initialized and set to the factory preset data when the [STANDBY/ON] switch is turned on while pressing the highest (rightmost) white key on the keyboard.

• TABLE 1

ORDER	SWITCH	NOTE (PSR-1000)	NOTE (PSR-2000)
1	EXTRA TRACKS	C2	C2
2	TRACK2	C#2	C#2
3	TRACK1	D2	D2
4	REPEAT	D#2	D#2
5	METRONOME	E2	E2
6	REC	F2	F2
7	TOP	F#2	F#2
8	START/STOP (SONG)	G2	G2
9	RW	G#2	G#2
10	FF	A2	A2
11	8BEAT	A#2	A#2
12	16BEAT	B2	B2
13	SWING & JAZZ	C3	C3
14	R & B	C#3	C#3
15	DANCE	D3	D3
16	LATIN	D#3	D#3
17	MARCH &WALTZ	E3	E3
18	USER STYLE	F3	F3
19	TRANSPOSE -	F#3	F#3
20	TRANSPOSE +	G3	G3
21	TEMPO -	G#3	G#3
22	TEMPO +	A3	A3
23	TAP TEMPO	A#3	A#3
24	PAD STOP	B3	B3
25	FADE IN/OUT	C4	C4
26	PAD1	C#4	C#4
27	PAD2	D4	D4
28	PAD3	D#4	D#4
29	PAD4	E4	E4
30	ACCOMP. ON/OFF	F4	F4
31	BREAK	F#4	F#4
32	INTRO	G4	G4
33	MAIN A	G#4	G#4
34	MAIN B	A4	A4
35	MAIN C	A#4	A#4
36	MAIN D	B4	B4
37	ENDING	C5	C5
38	AUTO FILL	C#5	C#5
39	OTS LINK	D5	D5
40	SYNC STOP	D#5	D#5

ORDER	SWITCH	NOTE (PSR-1000)	NOTE (PSR-2000)
41	SYNC START	E5	E5
42	START/STOP (STYLE)	F5	F5
43	SOUND CREATER	F#5	F#5
44	DIGITAL RECORDING	G5	G5
45	MIXING CONSOLE	G#5	G#5
46	DEMO	A5	A5
47	HELP	A#5	A#5
48	FUNCTION	B5	B5
49	A	C6	C6
50	B	C2	C2
51	C	C#2	C#2
52	D	D2	D2
53	E	D#2	D#2
54	DIRECT ACCESS	E2	E2
55	BALANCE	F2	F2
56	PART ON/OFF	F#2	F#2
57	1-U	G2	G2
58	1-L	G#2	G#2
59	2-U	A2	A2
60	2-L	A#2	A#2
61	3-U	B2	B2
62	3-L	C3	C3
63	4-U	C#3	C#3
64	4-L	D3	D3
65	5-U	D#3	D#3
66	5-L	E3	E3
67	6-U	F3	F3
68	6-L	F#3	F#3
69	7-U	G3	G3
70	7-L	G#3	G#3
71	8-U	A3	A3
72	8-L	A#3	A#3
73	EXIT	B3	B3
74	F	C4	C4
75	G	C#4	C#4
76	H	D4	D4
77	I	D#4	D#4
78	J	E4	E4
79	BACK	F4	F4
80	NEXT	F#4	F#4

ORDER	SWITCH	NOTE (PSR-1000)	NOTE (PSR-2000)
81	MAIN	G4	G4
82	LAYER	G#4	G#4
83	LEFT	A4	A4
84	MUSIC FINDER	A#4	A#4
85	LEFT HOLD	B4	B4
86	TOUCH	C5	C5
87	SUSTAIN	C#5	C#5
88	HARMONY ECHO	D5	D5
89	POLY/MONO	D#5	D#5
90	DSP	E5	E5
91	FAST/SLOW	F5	F5
92	PIANO &HARPSI	F#5	F#5
93	E.PIANO	G5	G5
94	ORGAN & ACCORDION	G#5	G#5
95	PERCCUSION	A5	A5
96	GUITAR	A#5	A#5
97	BASS	B5	B5
98	BRASS	C6	C6
99	W.WIND	C2	C2
100	STRING	C#2	C#2
101	CHOIR & PAD	D2	D2
102	SYNTH	D#2	D#2
103	XG	E2	E2
104	USER	F2	F2

ORDER	SWITCH	NOTE (PSR-1000)	NOTE (PSR-2000)
105	ORGAN FLUTES (PSR-2000 only)	–	F#2
106	OCTAVE -	F#2	G2
107	OCTAVE +	G2	G#2
108	VOCAL HARMONY (PSR-2000 only)	–	A2
109	TALK (PSR-2000 only)	–	A#2
110	EFFECT (PSR-2000 only)	–	B2
111	VH TYPE SELECT (PSR-2000 only)	–	C3
112	MC. SETUP (PSR-2000 only)	–	C#3
113	ENTER	G#2	D3
114	OTS1	A2	D#3
115	OTS2	A#2	E3
116	OTS3	B2	F3
117	OTS4	C3	F#3
118	FREEZE	C#3	G3
119	REGIST1	D3	G#3
120	REGIST2	D#3	A3
121	REGIST3	E3	A#3
122	REGIST4	F3	B3
123	REGIST5	F#3	C4
124	REGIST6	G3	C#4
125	REGIST7	G#3	D4
126	REGIST8	A3	D#4
127	MEMORY	A#3	E4

■ SYSTEM RESET

This operation lets you restore the PSR-1000/2000 to its original factory settings. These settings include System Setup, MIDI Setup, User Effect, Music Finder, and Files & Folders.

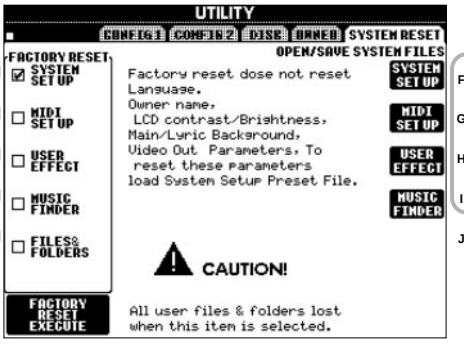
Restores the System Setup parameters to the original factory settings. You can also restore only the System Setup settings by simultaneously holding down the highest key on the keyboard (C6) and turning on the power.

Restores the MIDI templates to the original factory settings.

Restores the User Effects to the original factory settings.

Restores the Music Finder data to the original factory settings.

Deletes all files and folders stored in the User page.



Executes the Factory Reset operation for all items checkmarked above.

These call up the corresponding Open/ Save displays. These let you store the corresponding data as files to disk, for future recall. Pressing each of these buttons calls up the corresponding Open/Save display, from which you can select the corresponding PRESET page. From this PRESET page, you can save the relevant data.

NOTE

The functions and settings below do not apply to the Factory Reset operation. However, you can restore these to their original settings by calling up the preset System Setup files, using the Open/Save System Files function.
Language
Owner Name
LCD Brightness

NOTE

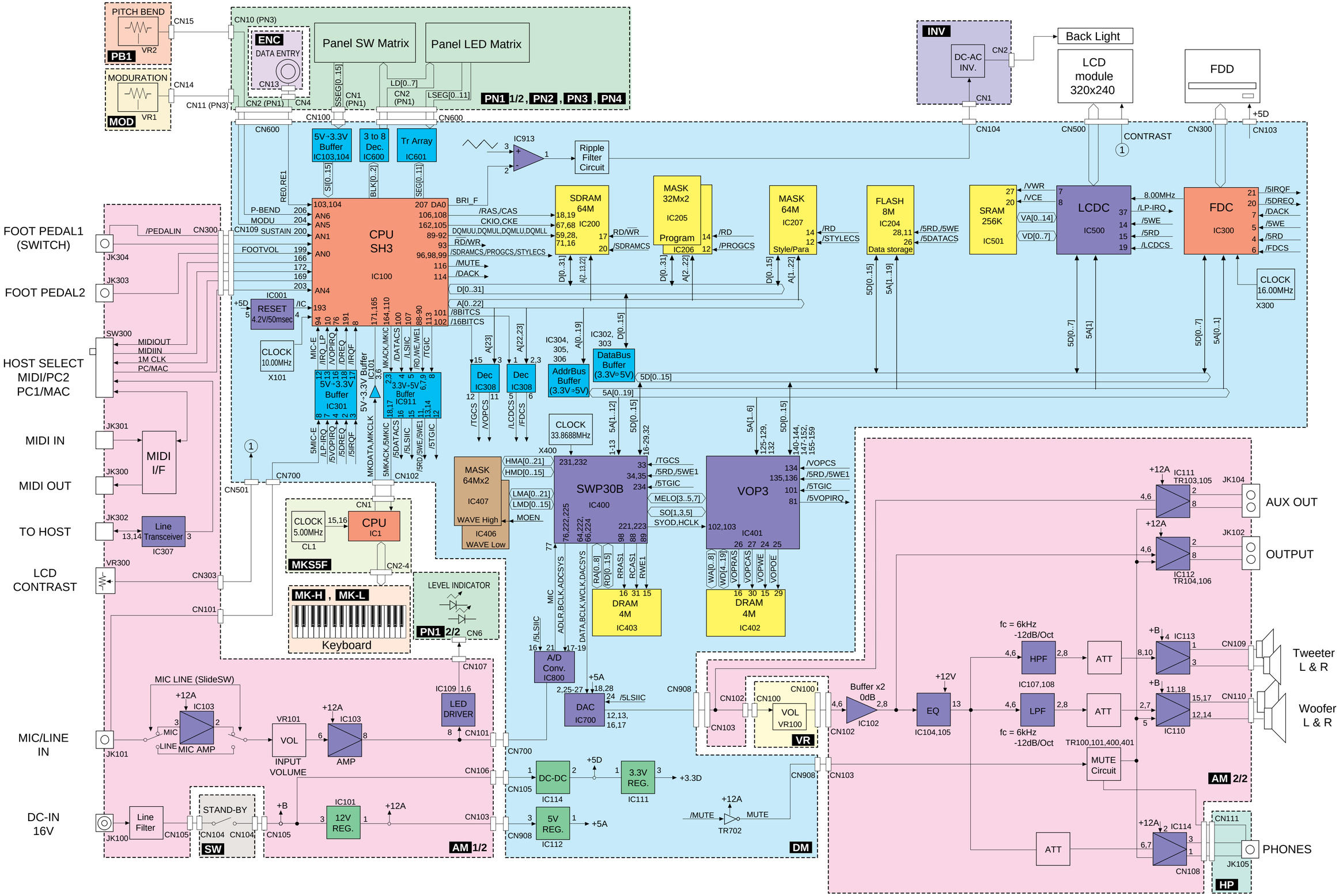
All Music Finder records can be stored together as a single file. When calling up a stored file, a message appears prompting you to replace or append the records as desired.
Replace:
All Music Finder records currently in the instrument are deleted and replaced with the records of the selected file.
Append:
The records called up are added to the vacant record numbers.

■PSR-1000 BLOCK DIAGRAM

PITCH BEND
VR3
PB2
CN16
CN10 (PN3)
ENC
DATA ENTRY
CN13
CN4
CN2 (PN1)
Panel SW Matrix
Panel LED Matrix
SSEG[0..15]
CN1 (PN1)
LD[0..7]
CN2 (PN1)
LSEG[0..11]
PN1 , PN2 , PN3 , PN4
CN100
CN600
INV
DC-AC INV.
CN2
CN1
CN104
Back Light
LCD module 320x240
CN500
CONTRAST
FDD
CN300
+5D
CN103
5V→3.3V Buffer IC103,104
3 to 8 Dec. IC600
Tr Array IC601
SI[0..15]
BLK[0..2]
SEG[0..11]
IC913
Ripple Filter Circuit
RE0,RE1
P-BEND
206
CPU SH3
IC100
103,104
AN6
AN1
AN0
AN4
193
207 DA0
106,108
162,105
89-92
93
96,98,99
116
114
BRI_F
/RAS,/CAS
CKIO,CKE
DQMUU,DQMUL,DQMLU,DQMLL
RD/WR
/SDRAMCS,/PROGCS,/STYLECS
/MUTE
/DACK
SDRAM 64M
IC200
18,19
67,68
59,28, 71,16
RD/WR
/SDRAMCS
MASK 32Mx2
IC205
Program
IC206
/RD
/PROGCS
MASK 64M
IC207
Style/Para
/RD
/STYLECS
FLASH 8M
IC204
28,11
26
Data storage
/5RD,/5WE
/5DATACS
SRAM 256K
IC501
/VWR
/VCE
VA[0..14]
VD[0..7]
LCDC
IC500
8.00MHz
/LP-IRQ
/5WE
/5RD
/LCDCS
FDC
IC300
/5IRQF
/5DREQ
/DACK
/5WE
/5RD
/FDCS
CLOCK 16.00MHz
X300
D[0..31]
A[2..13,22]
D[0..15]
A[1..22]
A[0..22]
/8BITCS
/16BITCS
5D[0..15]
5A[1..19]
5D[0..7]
5A[1]
5A[0..1]
CN109 SUSTAIN 200
FOOTVOL 199
166
172
169
203
/PEDALIN
CN300
FOOT PEDAL1 (SWITCH)
JK304
FOOT PEDAL2
JK303
IC001
RESET
4.2V/50msec
+5D
5
/IC
4
CLOCK 10.00MHz
X101
/IRQ_LP
/DREQ
/IRQF
5V→3.3V Buffer IC301
5V→3.3V Buffer IC101
3,6
MKACK,/MKIC
/DATACS
/LSIIC
/RD,/WE,/WE1
/TGIC
3.3V→5V Buffer IC911
MKDATA,MKCLK
5MKACK,/5MKIC
/5DATACS
/5LSIIC
/5RD,/5WE,/5WE1
/5TGIC
CN102
CN501
CN1
CLOCK 5.00MHz
15,16
CL1
CPU IC1
MKS5F
CN2-4
MK-H , MK-L
Keyboard
SW300
MIDIOUT
MIDIIN
1M CLK
PC/MAC
HOST SELECT MIDI/PC2 PC1/MAC
JK301
MIDI IN
MIDI I/F
JK300
MIDI OUT
JK302
TO HOST
Line Transceiver
IC307
13,14
3
VR300
LCD CONTRAST
CN303
A[23]
A[22,23]
A[0..19]
IC304, 305, 306
AddrBus Buffer (3.3V÷5V)
IC302, 303
DataBus Buffer (3.3V÷5V)
D[0..15]
5D[0..15]
5A[0..19]
Dec IC308
/TGCS
/LCDCS
/FDCS
CLOCK 33.8688MHz
X800
MASK 64M
IC803
WAVE
SMA[0..21]
SMD[0..15]
/SOE
/SCS0
SWX00B
IC801
/TGCS
/5RD,/5WE1
/5TGIC
158,164, 163,160
CMA[0..8]
CMD[0..15]
SRAS
SCAS
/CWE
DRAM 4M
IC800
DATA,BCLK,WCLK,DACSYS
+5A
2,25-27
18,28
/5LSIIC
DAC
IC700
12,13, 16,17
CN908
CN103
CN100
CN100
VOL
VR100
VR
CN102
Buffer x2
0dB
IC102
+12V
EQ
IC104,105
13
fc = 6kHz
-12dB/Oct
HPF
IC107,108
LPF
ATT
ATT
ATT
MUTE Circuit
TR100,101,400,401
+12A
IC111
TR103,105
JK104
AUX OUT
JK102
OUTPUT
IC112
TR104,106
+B
IC113
CN109
Tweeter L & R
IC110
CN110
Woofer L & R
AM 2/2
DC-IN 16V
JK100
Line Filter
CN105
STAND-BY
CN104
CN104
SW
+B
IC101
12V REG.
+12A
CN106
CN103
DC-DC
IC114
+5D
3.3V REG.
IC111
+3.3D
5V REG.
IC112
+5A
/MUTE
MUTE
TR702
DM
IC114
CN111
JK105
PHONES
CN108
HP
28CA1-8820767

PSR-1000

■PSR-2000 BLOCK DIAGRAM



28CA1-8820768

PSR-2000

■PSR-1000 OVERALL CIRCUIT DIAGRAM (DM1/2, INV)

Note: See parts list for details of circuit board component parts.

[ ]: Mylar Capacitor
[ ]: Ceramic Capacitor
: Metal Oxide Film Resistor

■PSR-2000 OVERALL CIRCUIT DIAGRAM (DM1/2, INV)

INV

DM 1/2

V420040
✶ATTENTION
High Voltage

LCD

Note: See parts list for details of circuit board component parts.

(マ): Mylar Capacitor
(セ): Ceramic Capacitor
抵抗: Metal Oxide Film Resistor

•Floppy Disk Drive

✶PROGRAM-L ROM:
IC205 (MASK) or
IC915 (FLASH) installed

✶PROGRAM-H ROM:
IC206 (MASK) or
IC916 (FLASH) installed

✶STYLE/PARA ROM: IC207 (MASK) or IC917 (FLASH) installed

○: installed
×: not installed

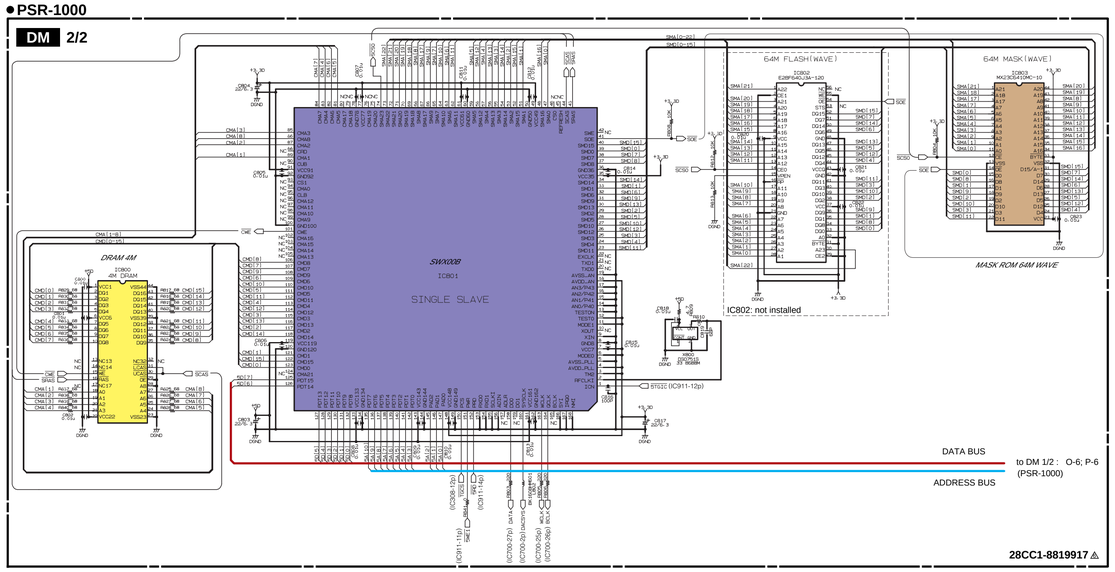
ADDRESS BUS
to DM 2/2 : A-6 (PSR-2000)

DATA BUS
to DM 2/2 : A-6
(PSR-2000)

■PSR-1000/PSR-2000 OVERALL CIRCUIT DIAGRAM (DM 2/2, PN1, PN2, PN3, PN4, ENC, PB1, PB2, MOD)

●PSR-1000

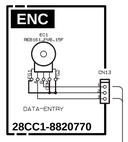
DM 2/2



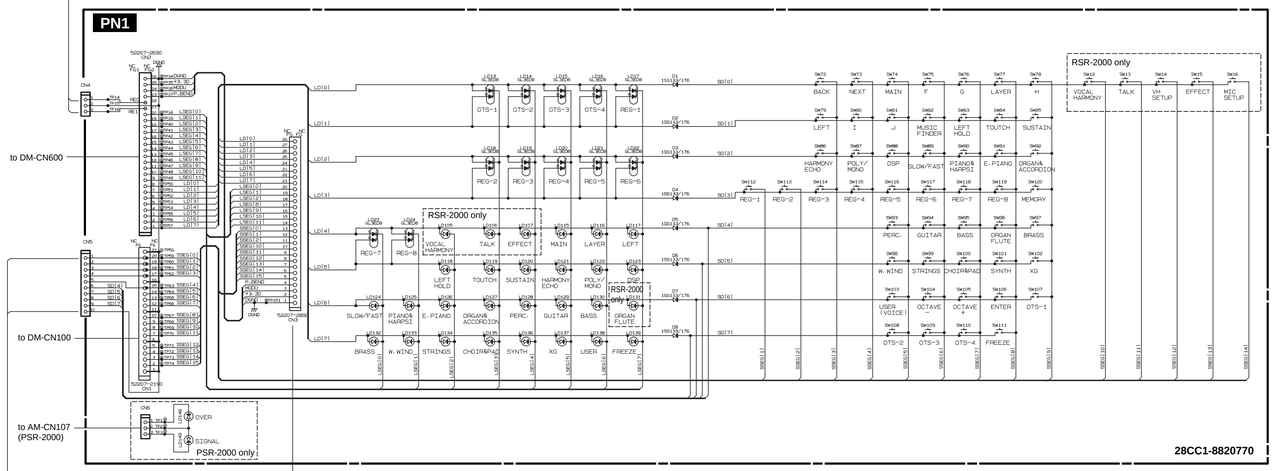
●PSR-2000

DM 2/2

ENC



PN1



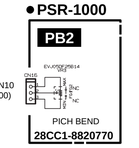
PN2

PN4

PN3

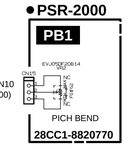
●PSR-1000

PB2



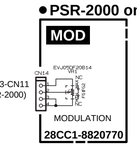
●PSR-2000

PB1



●PSR-2000 only

MOD



to PN3-CN10 (PSR-1000)

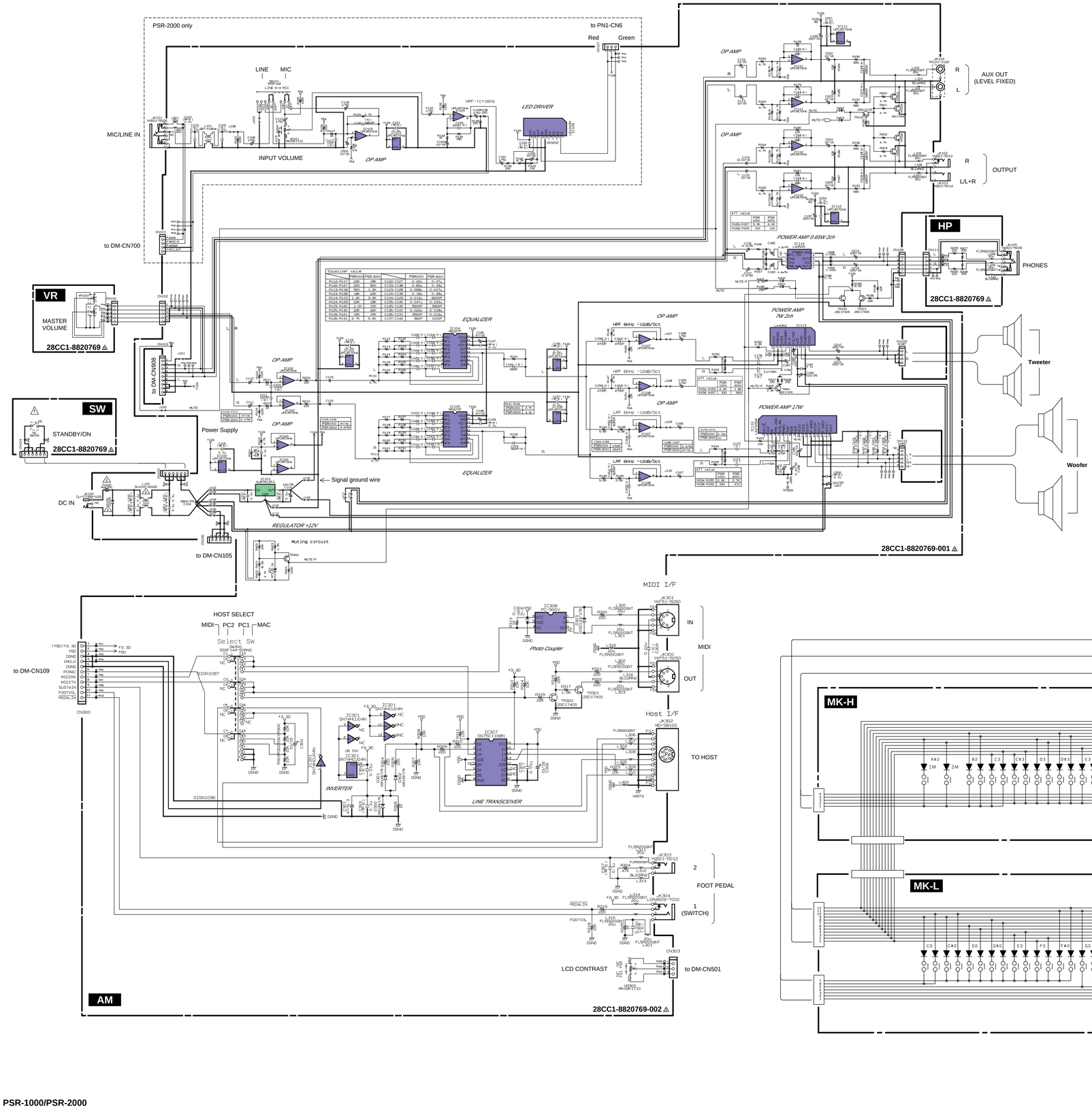
to PN3-CN10 (PSR-2000)

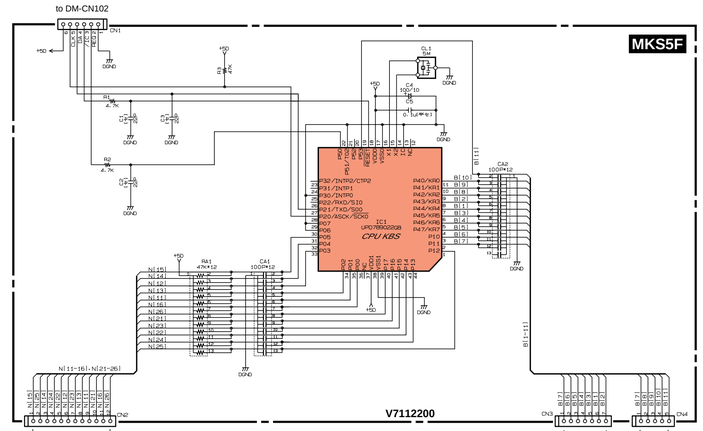
to PN3-CN11 (PSR-2000)

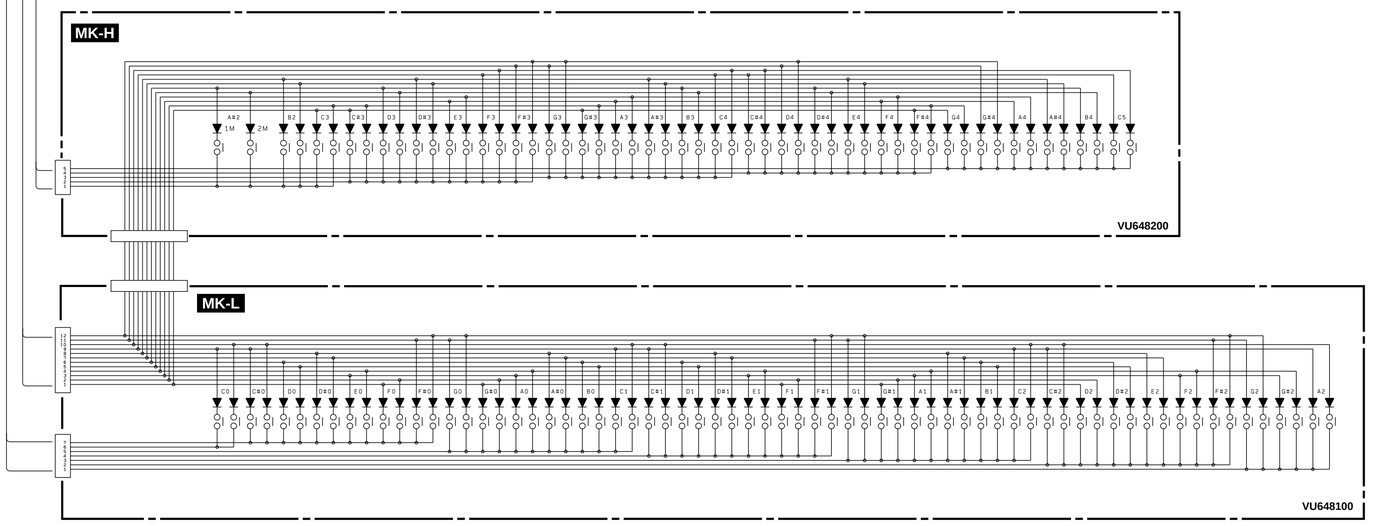
(⊣⊢): Ceramic Capacitor

Note: See parts list for details of circuit board component parts.

■PSR-1000/PSR-2000 OVERALL CIRCUIT DIAGRAM (AM, VR, HP, SW, MKS5F, MK-L, MK-H)







•S3V20 (VR313500) DIODE 1: ANODE 2: CATHODE	•SI-8050S(LF1111) (X0548A00) DC-DC CONVERTER 1: V in 2: SW OUT 3: GND 4: V os 5: S.S	•NJM78L05UA(XJ598A00) REGULATOR +5V 1: OUTPUT 2: COMMON 3: INPUT
•NJM7812FA(XJ608A00) REGULATOR +12V 1: OUTPUT 2: COMMON 3: INPUT	•AN7812F(XM169A00) REGULATOR +12V 1: INPUT 2: COMMON 3: OUTPUT	• µPC2933T(XS516A00) REGULATOR +3.3V 1: V in 2: GND 3: V out

■TO SERVICE PERSONNEL

Critical Components Information
Components having special characteristics are marked ⚠ and must be replaced with parts having specifications equel to those originally installed.

(マ): Mylar Capacitor
(セ): Ceramic Capacitor
(ﾊﾝﾄｳ): Semiconductive Cera Cap

Note: See parts list for details of circuit board component parts.