PORTATONE

PSR-740/PSR-640

SERVICE MANUAL

PSR-740

PSR-640

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PK 001627

PSR-740 19990901-160000
PSR-640 19990901-120000

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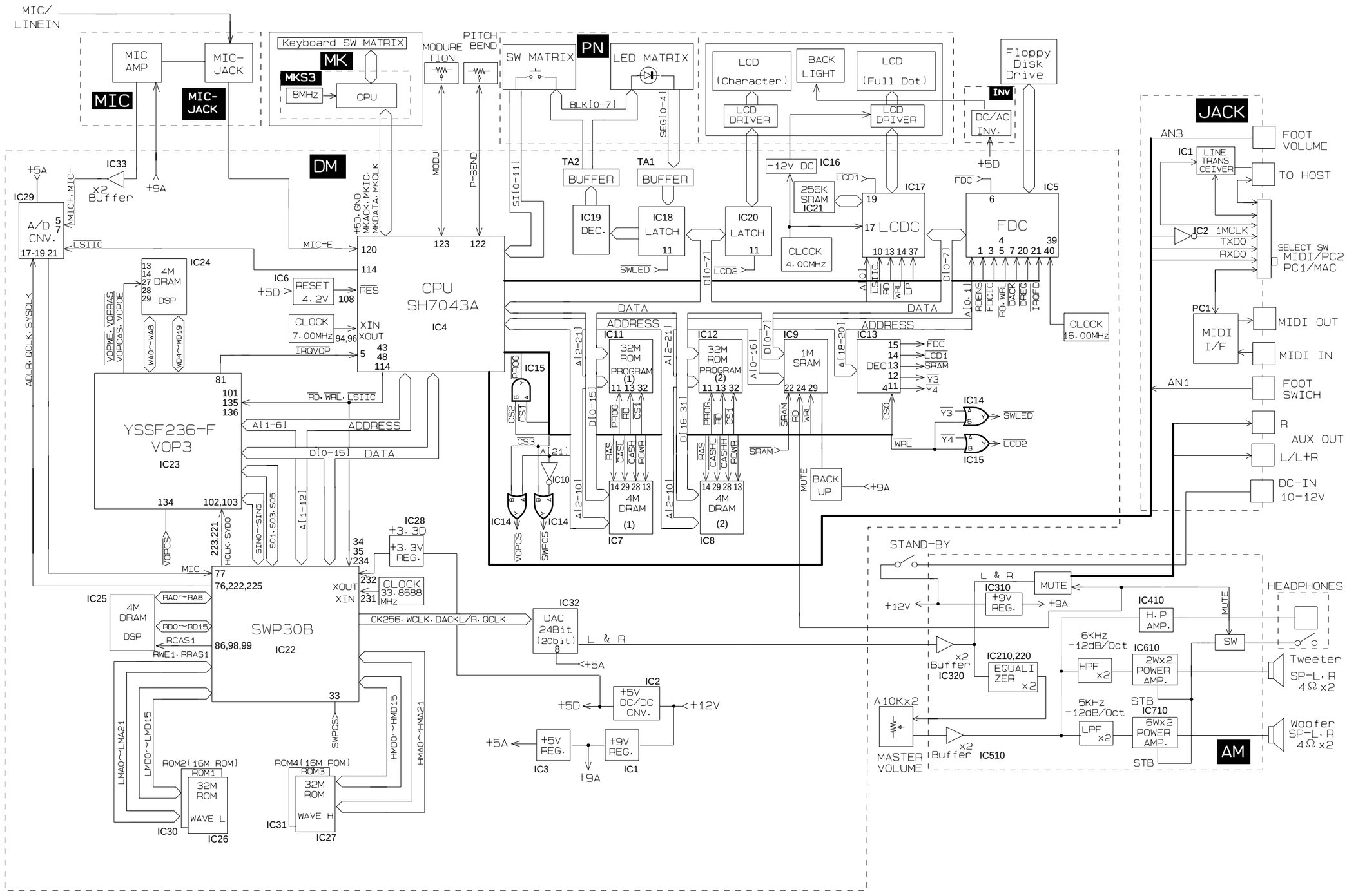
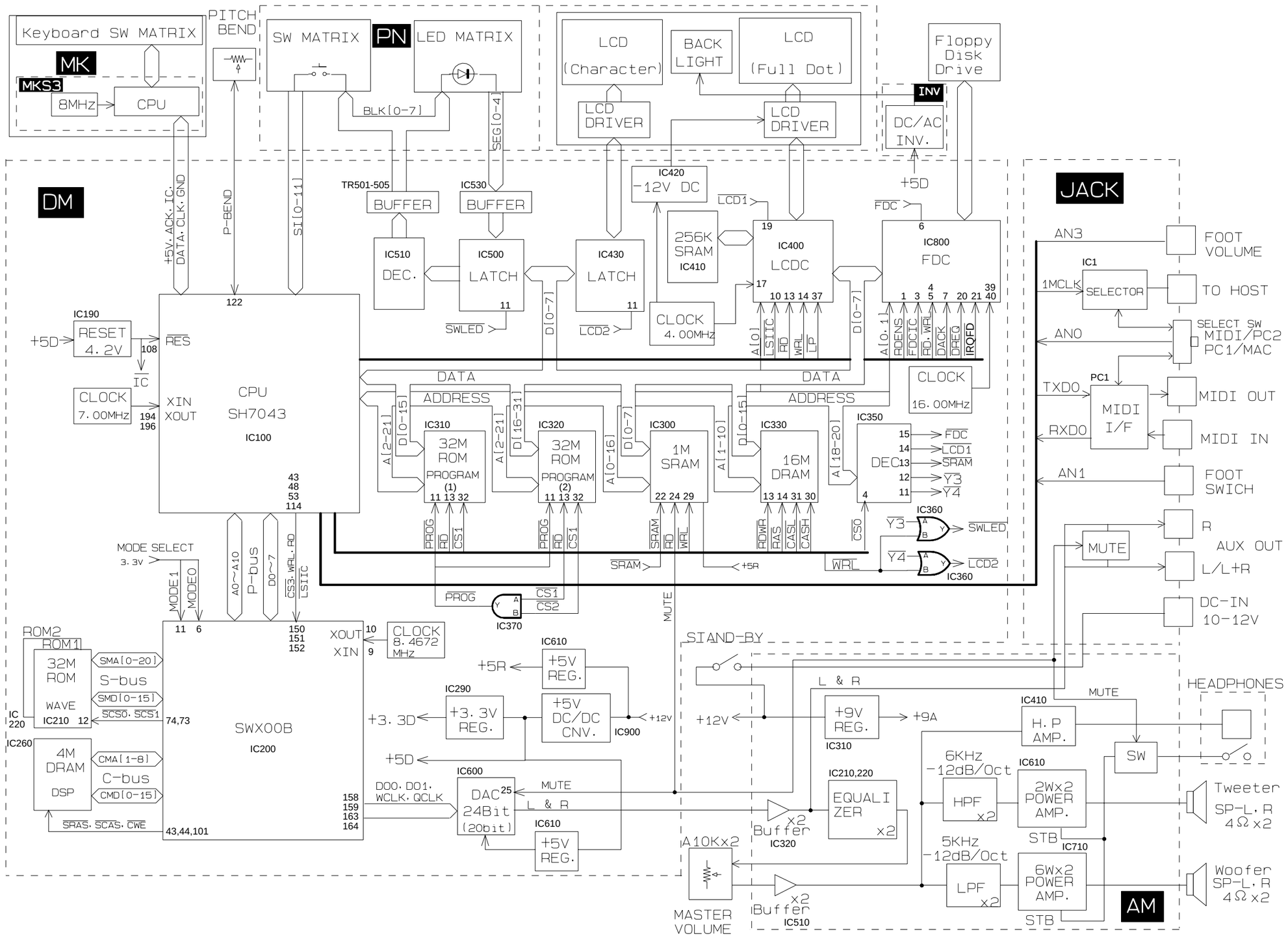
PSR-740 BLOCK DIAGRAM



■ PSR-640 BLOCK DIAGRAM



LSI PIN DESCRIPTION

● **SH-7043A** (XW485100) **CPU**
SH-7043 (XW180100) **CPU**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	/WRHH/PA23	O	HH write/Port A	73	D15	I/O	
2	DACK0/PE14	O	DMA transfer strobe/Port E	74	D14	I/O	Data bus
3	/WRHL/PA22	O	HL write/Port A	75	D13	I/O	
4	/CASHH/PA21	I/O	HH Column address strobe/Port A	76	D12	I/O	
5	DACK1/PE15	O	DMA transfer strobe/Port E	77	VCC	I	Power supply
6	VSS	I	Ground	78	D11	I/O	Data bus
7	A0	O		79	VSS	I	Ground
8	A1	O		80	D10	I/O	
9	A2	O	Address bus	81	D9	I/O	
10	A3	O		82	D8	I/O	Data bus
11	A4	O		83	D7	I/O	
12	VCC	I	Power supply	84	D6	I/O	
13	A5	O	Address bus	85	VCC	I	Power supply
14	VSS	I	Ground	86	D5	I/O	Data bus
15	A6	O		87	VSS	I	Ground
16	A7	O		88	D4	I/O	
17	A8	O		89	D3	I/O	
18	A9	O		90	D2	I/O	Data bus
19	A10	O		91	D1	I/O	
20	A11	O	Address bus	92	D0	I/O	
21	A12	O		93	VSS	I	Ground
22	A13	O		94	XTAL	I	Crystal oscillator
23	A14	O		95	MD3	I	Mode select
24	A15	O		96	EXTAL	I	Crystal oscillator
25	A16	O		97	MD2	I	Mode select
26	VCC	I	Power supply	98	NMI	-	Non-maskable interrupt
27	A17	O	Address bus	99	VCC/FW	I	Power supply
28	VSS	I	Ground	100	PA16	I/O	Port A
29	/CASHL/PA20	I/O	HL Column address strobe/Port A	101	PA17	I/O	Port A
30	PA19	I/O	Port A	102	MD1	I	Mode select
31	/RAS/PB2	O	Row address strobe/Port B	103	MD0	I	Mode select
32	/CASL/PB3	O	Column address strobe (low) /Port B	104	PLLVCC	I	PLL Power supply
33	PA18	I/O	Port A	105	PLLCAP	I	PLL capacitor
34	/CASH/PB4	O	Column address strobe (high) /Port B	106	PLLVSS	I	PLL Ground
35	VSS	I	Ground	107	CK/PA15	I/O	Clock/Port A
36	RDWR/PB5	O	DRAM read/write /Port B	108	/RES	I	Reset
37	A18	O		109	DREQ0/PE0	I/O	DMA transfer request/Port E
38	A19	O	Address bus	110	TIOC0B/PE1	I/O	MTU input capture/output compare (ch 0)/Port E
39	A20	O		111	/DREQ1/PE2	I/O	DMA transfer request/Port E
40	VCC	I	Power supply	112	VCC	I	Power supply
41	A21	O	Address bus	113	PE3	I/O	
42	VSS	I	Ground	114	PE4	I/O	Port E
43	/RD	O	Read	115	PE5	I/O	
44	/WDTOVF	O	Watch dog timer overflow	116	PE6	I/O	
45	D31	I/O	Data bus	117	VSS	I	Ground
46	D30	I/O	Data bus	118	AN0 /PF0	I	
47	/WRH	O	High write	119	AN1/ PF1	I	
48	/WRL	O	Low write	120	AN2 /PF2	I	
49	/CS1	O	Chip select	121	AN3 /PF3	I	Analog input/Port F
50	/CS0	O	Chip select	122	AN4 /PF4	I	
51	/IRQ3/PA9/TCLKD	I/O	Interrupt request/Port A/clock	123	AN5/PF5	I	
52	/IRQ2/PA8/TCKLC	I/O	Interrupt request/Port A/clock	124	AVSS	I	Analog ground
53	/CS3	O	Chip select	125	AN6/PF6	I	Analog input/ Port F
54	/CS2	O	Chip select	126	AN7/PF7	I	Analog input /Port F
55	VSS	I	Ground	127	AVREF	I	Analog reference voltage
56	D29	I/O		128	AVCC	I	Analog power supply
57	D28	I/O		129	VSS	I	Ground
58	D27	I/O	Data bus	130	RxDO	I	Receive data
59	D26	I/O		131	TxDO	O	Transmit data
60	D25	I/O		132	/IRQ0/SCK0	I	Interrupt request/Serial clock
61	VSS	I	Ground	133	RxD1	I	Receive data
62	D24	I/O	Data bus	134	TxD1/PA4	I/O	SCI/Port A
63	VCC	I	Power supply	135	VCC	I	Power supply
64	D23	I/O		136	/IRQ1/SCK1	I	Interrupt request/Serial clock
65	D22	I/O		137	PE7	I/O	
66	D21	I/O		138	PE8	I/O	Port E
67	D20	I/O	Data bus	139	PE9	I/O	
68	D19	I/O		140	PE10	I/O	
69	D18	I/O		141	VSS	I	Ground
70	D17	I/O		142	PE11	I/O	
71	VSS	I	Ground	143	PE12	I/O	Port E
72	D16	I/O	Data bus	144	PE13	I/O	

● **HG73C205AFD** (XU947C00) **SWX00B** TONE GENERATOR

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	ICN	I	Initial clear	85	CMA3	O	Program address bus
2	RFCLKI	I	PLL Clock	86	CMA8	O	Program address bus
3	TM2	I	PLL Control	87	CMA2	O	Program address bus
4	AVDD_PLL		Power supply	88	CRD	O	read signal
5	AVSS_PLL		Ground	89	CMA1	O	Program address bus
6	MODE0	I	SWX dual mode	90	CUB	O	high byte effective signal
7	VCC7		Power supply	91	VCC91		Power supply
8	GND8		Ground	92	GHND92		Ground
9	XIN	I	crystal oscillator	93	CS1	O	CS signal
10	XOUT	O	crystal oscillator	94	CMA0	O	Program address bus
11	MODE1	I	SWX separate mode	95	CLB	O	low byte effective signal
12	TEST0	I	TEST pin	96	CMA12	O	Program address bus
13	TESTON	I	TEST pin	97	CMA11	O	
14	AN0-P40	I	A/D converter	98	CMA10	O	
15	AN1-P41	I	A/D converter	99	CMA9	O	
16	AN2-P42	I	A/D converter	100	GND100		Ground
17	AN3-P43	I	A/D converter	101	CWE	O	write signal
18	AVDD_AN		Power supply	102	CMA16	O	Program address bus
19	AVSS_AN		Ground	103	CMA15	O	Program address bus
20	TXD0	O	for MIDI or TO-HOST	104	CMA14	O	Program address bus
21	TXD1	O	for MIDI	105	CMA13	O	Program address bus
22	EXCLK	I	Crystal oscillator	106	CMD8	I/O	Program memory Data bus
23	SMD11	I/O	Wave memory data bus	107	CMD7	I/O	Program memory Data bus
24	SMD4	I/O	Wave memory data bus	108	CMD9	I/O	Program memory Data bus
25	SMD3	I/O	Wave memory data bus	109	CMD6	I/O	Program memory Data bus
26	SMD12	I/O	Wave memory data bus	110	CMD10	I/O	Program memory Data bus
27	SMD10	I/O	Wave memory data bus	111	CMD5	I/O	Program memory Data bus
28	SMD5	I/O	Wave memory data bus	112	CMD11	I/O	Program memory Data bus
29	SMD2	I/O	Wave memory data bus	113	CMD4	I/O	Program memory Data bus
30	SMD13	I/O	Wave memory data bus	114	CMD12	I/O	Program memory Data bus
31	SMD9	I/O	Wave memory data bus	115	CMD3	I/O	Program memory Data bus
32	SMD6	I/O	Wave memory data bus	116	CMD13	I/O	Program memory Data bus
33	SMD1	I/O	Wave memory data bus	117	CMD2	I/O	Program memory Data bus
34	SMD14	I/O	Wave memory data bus	118	CMD14	I/O	Program memory Data bus
35	VCC35		Power supply	119	VCC119		Power supply
36	GND36		Ground	120	GND115		Ground
37	SMD8	I/O	Wave memory data bus	121	CMD1	I/O	Program memory Data bus
38	SMD7	I/O	Wave memory data bus	122	CMD15	I/O	Program memory Data bus
39	SMD0	I/O	Wave memory data bus	123	CMD0	I/O	Program memory Data bus
40	SMD15	I/O	Wave memory data bus	124	CMA21	O	Program address bus
41	SOE	O	read signal	125	PDT15	I/O	SWX access data bus
42	SWE	O	write signal	126	PDT14	I/O	
43	SRAS	O	RAS signal	127	PDT13	I/O	
44	SCAS	O	CAS signal	128	PDT12	I/O	
45	REFRESH	O	REFRESH signal	129	PDT11	I/O	
46	CS0	O	CS signal	130	PDT10	I/O	
47	SMA0	O	Memory address bus	131	PDT9	I/O	
48	SMA16	O	Memory address bus	132	PDT8	I/O	
49	VCC49		Power supply	133	VCC133		Power supply
50	GND50		Ground	134	GND134		Ground
51	SMA1	O	Memory address bus	135	PDT7	I/O	SWX access data bus
52	SMA15	O	Memory address bus	136	PDT6	I/O	
53	SMA2	O	Memory address bus	137	PDT5	I/O	
54	SMA14	O	Memory address bus	138	PDT4	I/O	
55	SMA3	O	Memory address bus	139	PDT3	I/O	
56	SMA13	O	Memory address bus	140	PDT2	I/O	
57	SMA4	O	Memory address bus	141	PDT1	I/O	
58	SMA12	O	Memory address bus	142	PDT0	I/O	
59	SMA5	O	Memory address bus	143	VCA143		Power supply
60	GND60		Ground	144	GND144		Ground
61	VCC61		Power supply	145	PAD2	I	SWX access address bus
62	SMA11	O	Memory address bus	146	PAD1	I	
63	SMA6	O	Memory address bus	147	PAD0	I	
64	SMA10	O	Memory address bus	148	VCC148		Power supply
65	SMA7	O	Memory address bus	149	GND149		Ground
66	SMA9	O	Memory address bus	150	PCS	I	Chip select
67	SMA17	O	Memory address bus	151	PWR	I	write enable
68	SMA8	O	Memory address bus	152	PRD	I	read enable
69	SMA18	O	Memory address bus	153	RXD0	I	for Midi or TO-HOST
70	SMA19	O	Memory address bus	154	RXD1	I	for Midi or Key scan
71	SMA20	O	Memory address bus	155	SCLKI	I	EXT Clock
72	SMA21	O	Memory address bus	156	ADIN	I	A/D converter
73	SMA22	O	Memory address bus	157	ADLR	O	A/D converter LR clock
74	SMA23	O	Memory address bus	158	DO0	O	DAC
75	CMA20	O	Program address bus	159	DO1	O	DAC
76	CMA19	O	Program address bus	160	SYSCLK	O	1/2 clock
77	VCC77		Power supply	161	VCC161		Power supply
78	GND78	O	Ground	162	GND162		Ground
79	CMA18	O	Program address bus	163	WCLK	O	for DAC LR clock
80	CMA17	O	Program address bus	164	QCLK	O	1/12 clock
81	CMA5	O	Program address bus	165	BCLK	O	IIS-DAC clock
82	CMA6	O	Program address bus	166	SYI	I	Synch signal
83	CMA4	O	Program address bus	167	IRQ0	I	Interrupt request
84	CMA7	O	Program address bus	168	NMI	I	Interrupt request

● **TC203C760HF-002** (XS725A00)
SWP30B (AWM Tone Generator coped with MEG) Standard Wave Processor

PIN NO.	NAME	I/O	FUNCTION
1	Vss		(Ground)
2	CA0	I	Address bus internal register
3	CA1	I	
4	CA2	I	
5	CA3	I	
6	CA4	I	
7	CA5	I	
8	CA6	I	
9	CA7	I	
10	CA8	I	
11	CA9	I	
12	CA10	I	
13	CA11	I	
14	VSS		(Ground)
15	CD0	I/O	Data bus of internal register
16	CD1	I/O	
17	CD2	I/O	
18	CD3	I/O	
19	CD4	I/O	
20	CD5	I/O	
21	CD6	I/O	
22	CD7	I/O	
23	CD8	I/O	
24	CD9	I/O	
25	CD10	I/O	
26	CD11	I/O	
27	CD12	I/O	
28	CD13	I/O	
29	CD14	I/O	
30	VDD		(Power supply)
31	VSS		(Ground)
32	CD15	I/O	
33	/CS	I	Chip select
34	/WR	I	Write strobe
35	/RD	I	Read strobe
36	VDDS		(Power supply)
37	SYSH0	O	NSYS/LNSYS upper 16 bits
38	SYSH1	O	
39	SYSH2	O	
40	SYSH3	O	
41	SYSH4	O	
42	SYSH5	O	
43	SYSH6	O	
44	SYSH7	O	
45	KONO0	O	Key on data
46	KONO1	O	
47	KONO2	O	
48	KONO3	O	
49	VSS		(Ground)
50	SYSL0	I/O	NSYS input/LNSYS output lower 8 bits
51	SYSL1	I/O	
52	SYSL2	I/O	
53	SYSL3	I/O	
54	SYSL4	I/O	
55	SYSL5	I/O	
56	SYSL6	I/O	
57	SYSL7	I/O	
58	KONI0	I	Key on data
59	KONI1	I	
60	VDDS	I	(Power supply)
61	VSS		(Ground)
62	KONI2	I	
63	KONI3	I	
64	DAC0	O	DAC output
65	DAC1	O	
66	WCLK	O	DAC0/DAC1 word clock
67	MELO0	O	MEL wave data output
68	MELO1	O	
69	MELO2	O	
70	MELO3	O	
71	MELO4	O	
72	MELO5	O	
73	MELO6	O	
74	MELO7	O	
75	VDDS		(Power supply)
76	ADLR	O	ADC word clock
77	MELI0	I	MEL wave data input
78	MELI1	I	
79	MELI2	I	
80	MELI3	I	
81	MELI4	I	
82	MELI5	I	
83	MELI6	I	
84	MELI7	I	
85	VSS		(Ground)
86	/RCAS	O	DRAM column address strobe
87	RA8	O	DRAM address bus
88	RA7	O	
89	RA6	O	
90	VDD		(Power supply)
91	VSS		(Ground)
92	RA5	O	
93	RA4	O	
94	RA3	O	
95	RA2	O	
96	RA1	O	
97	RA0	O	
98	/RRAS	O	DRAM row address strobe
99	/RWE	O	DARM write enable
100	VSS		(Ground)
101	RD7	I/O	DRAM data bus
102	RD6	I/O	
103	RD5	I/O	
104	RD4	I/O	
105	RD3	I/O	
106	RD2	I/O	
107	RD1	I/O	
108	RD0	I/O	
109	VSS		(Ground)
110	RD17	I/O	
111	RD16	I/O	
112	RD15	I/O	
113	RD14	I/O	
114	RD13	I/O	
115	RD12	I/O	
116	RD11	I/O	
117	RD10	I/O	
118	RD9	I/O	
119	RD8	I/O	
120	VDDS		(Power supply)

PIN NO.	NAME	I/O	FUNCTION
121	VSS		(Ground)
122	HMD0	I/O	Wave memory data bus (Upper data memory)
123	HMD1	I/O	
124	HMD2	I/O	
125	HMD3	I/O	
126	HMD4	I/O	
127	HMD5	I/O	
128	HMD6	I/O	
129	HMD7	I/O	
130	HMD8	I/O	
131	HMD9	I/O	
132	HMD10	I/O	
133	HMD11	I/O	
134	HMD12	I/O	
135	HMD13	I/O	
136	HMD14	I/O	
137	HMD15	I/O	
138	VSS		(Ground)
139	HMA0	O	Wave memory address bus (Upper 16 bits)
140	HMA1	O	
141	HMA2	O	
142	HMA3	O	
143	HMA4	O	
144	HMA5	O	
145	HMA6	O	
146	HMA7	O	
147	HMA8	O	
148	HMA9	O	
149	HMA10	O	
150	VSS		(Ground)
151	VDD		(Power supply)
152	HMA11	O	
153	HMA12	O	
154	HMA13	O	
155	HMA14	O	
156	HMA15	O	
157	HMA16	O	
158	HMA17	O	
159	HMA18	O	
160	HMA19	O	
161	HMA20	O	
162	HMA21	O	
163	HMA22	O	
164	HMA23	O	
165	HMA24	O	
166	VSS		(Ground)
167	/MRAS	O	RAS when DRAM(s) is connected to wave memory
168	/MCAS	O	CAS when DRAM(s) is connected to wave memory
169	/MOE	O	Wave memory output enable
170	/MWE	O	Wave memory write enable
171	VSS		(Ground)
172	LMD0	I/O	Wave memory data bus (Lower data memory)
173	LMD1	I/O	
174	LMD2	I/O	
175	LMD3	I/O	
176	LMD4	I/O	
177	LMD5	I/O	
178	LMD6	I/O	
179	LMD7	I/O	
180	VDDS		(Power supply)
181	VSS		(Ground)
182	LMD8	I/O	
183	LMD9	I/O	
184	LMD10	I/O	
185	LMD11	I/O	
186	LMD12	I/O	
187	LMD13	I/O	
188	LMD14	I/O	
189	LMD15	I/O	
190	VSS		(Ground)
191	LMA0	O	Wave memory address bus (Lower data memory)
192	LMA1	O	
193	LMA2	O	
194	LMA3	O	
195	LMA4	O	
196	LMA5	O	
197	LMA6	O	
198	LMA7	O	
199	LMA8	O	
200	LMA9	O	
201	LMA10	O	
202	LMA11	O	
203	VSS		(Ground)
204	LMA12	O	
205	LMA13	O	
206	LMA14	O	
207	LMA15	O	
208	LMA16	O	
209	LMA17	O	
210	VDD		(Power supply)
211	VSS		(Ground)
212	LMA18	O	
213	LMA19	O	
214	LMA20	O	
215	LMA21	O	
216	LMA22	O	
217	LMA23	O	
218	LMA24	O	
219	VSS		(Ground)
220	SYO	O	Sync. signal for master clock
221	SYOD	O	Sync. signal for HCLK/QCLK
222	QCLK	O	1/12 master clock (64 Fs)
223	HCLK	O	1/6 master clock (128 Fs)
224	CK256	O	1/3 master clock (256 Fs)
225	SYSCLK	O	1/2 master clock (384 Fs)
226	VDDS		(Power supply)
227	SYI	I	Sync. clock
228	MCLKI	I	Master clock input
229	MCLKO	O	Master clock output
230	VDD		(Power supply)
231	XIN	I	Crystal osc. input
232	XOUT	O	Crystal osc. output
233	VSS		(Ground)
234	/IC	I	Initial clear
235	CHIP2	I	2 chips mode enable
236	SLAVE	I	Master/Slave select when 2 chips mode
237	/TESTO	I	Test pin
238	/ACI	I	
239	DCTEST	I	
240	VDDS		(Power supply)

● YSS236-F (XT013A00) VOP3

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	VSS		Power supply	81	SO7	O	
2	WA17	O		82	SO6	O	Serial output
3	WA16	O		83	SO5	O	
4	WA15	O		84	VDD		Ground
5	WA14	O		85	VSS		Power supply
6	WA13	O	External memory address bus	86	SO4	O	
7	WA12	O		87	SO3	O	
8	WA11	O		88	SO2	O	Serial output
9	WA10	O		89	SO1	O	
10	VDD		Ground	90	SO0	O	
11	VSS		Power supply	91	WDCK	O	Data enable for DAC
12	WA09	O		92	SWPKON	O	SWP00 format key on output
13	WA08	O		93	IRQN	O	EG interrupt
14	WA07	O		94	VDD		Ground
15	WA06	O		95	VSS		Power supply
16	WA05	O	External memory address bus	96	XTAL_I	I	Quartz crystal terminal
17	WA04	O		97	XTAL_O	O	Quartz crystal terminal
18	WA03	O		98	MCLK	O	Oscillate clock output
19	WA02	O		99	VDD		Ground
20	VDD		Ground	100	VSS		Power supply
21	VSS		Power supply	101	MICN	I	Initial clear
22	WA01	O	External memory address bus	102	CLKIN	I	Master clock input
23	WA00	O		103	SYWIN	I	Sync.signal input
24	WEN	O	External memory control (WEN)	104	SYW	O	Sync.signal output
25	OEN	O	External memory control (OEN)	105	SYWD	O	Sync.signal output
26	RASN	O	External memory control (RASN)	106	VDD		Ground
27	CASN	O	External memory control (CASN)	107	VSS		Power supply
28	CEN	O	External memory control (CEN)	108	CLKO	O	For test (512 fs output)
29	VDD		Ground	109	WCLK	O	2 times sync.clock output (256 fs)
30	VSS		Power supply	110	HCLK	O	4 times sync.clock output (128 fs)
31	WD19	I/O		111	QCLK	O	8 times sync.clock output (64 fs)
32	WD18	I/O		112	TSTCI	I	PLL test input
33	WD17	I/O	External memory data bus	113	VDD		Ground
34	WD16	I/O		114	VSS		Power supply
35	WD15	I/O		115	(NC)		
36	WD14	I/O		116	VDD(PLL)		
37	VDD		Ground	117	CPO	O	PLL control output
38	VSS		Power supply	118	CPIN	I	PLL control input
39	WD13	I/O		119	REF	I	PLL control intput
40	WD12	I/O		120	VSS(PLL)		
41	WD11	I/O		121	(NC)		
42	WD10	I/O	External memory data bus	122	VDD		Ground
43	WD09	I/O		123	VSS		Power supply
44	WD08	I/O		124	TSTCS	I	PLL test input
45	WD07	I/O		125	CA6	I	
46	VDD		Ground	126	CA5	I	CPU address bus
47	VSS		Power supply	127	CA4	I	
48	WD06	I/O		128	CA3	I	
49	WD05	I/O		129	CA2	I	
50	WD04	I/O		130	VDD		Ground
51	WD03	I/O	External memory data bus	131	VSS		Power supply
52	WD02	I/O		132	CA1	I	CPU address bus
53	WD01	I/O		133	CA0	I	Lo/Hi select in 8 bits write
54	WD00	I/O		134	CSN	I	Chip select
55	VDD		Ground	135	RDN	I	Register read
56	VSS		Power supply	136	WRN	I	Register write
57	TST2	O		137	BTYP		Data bus type select
58	TST1	O	Test output	138	VDD		Ground
59	TST0	O		139	VSS		Power supply
60	MS	I	Memory select	140	CD15	I/O	
61	LRCLK	O	LR clock for ADC	141	CD14	I/O	
62	SI7	I	Serial input	142	CD13	I/O	CPU data bus
63	SI6	I		143	CD12	I/O	
64	VDD		Ground	144	CD11	I/O	
65	VSS		Power supply	145	VDD		Ground
66	SI5	I		146	VSS		Power supply
67	SI4	I		147	CD10	I/O	
68	SI3	I	Serial input	148	CD09	I/O	
69	SI2	I		149	CD08	I/O	CPU data bus
70	SI1	I		150	CD07	I/O	
71	SI0	I		151	CD06	I/O	
72	DB1	I	Output bit type select for DAC	152	CD05	I/O	
73	DB0	I		153	VDD		Ground
74	VDD		Ground	154	VSS		Power supply
75	VSS		Power supply	155	CD04	I/O	
76	ODFM	I	Output mode select for DAC	156	CD03	I/O	
77	OFS3	I		157	CD02	I/O	CPU data bus
78	OFS2	I	Serial output format select	158	CD01	I/O	
79	OFS1	I		159	CD00	I/O	
80	OFS0	I		160	VDD		Ground

● **HD63B05V0F073P** (XR951A00) **CPU**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	/RES	I	Reset	21	C7	I/O	
2	/INT	I	Interrupt request	22	C6	I/O	
3	NUM	I	Non-maskable interrupt	23	C5	I/O	
4	A7	I/O		24	C4	I/O	Port C
5	A6	I/O		25	C3	I/O	
6	A5	I/O		26	C2	I/O	
7	A4	I/O	Port A	27	C1	I/O	
8	A3	I/O		28	C0	I/O	
9	A2	I/O		29	D0	I/O	
10	A1	I/O		30	D1	I/O	Port D
11	A0	I/O		31	D2	I/O	
12	B0	I/O		32	D3/TX	O	(Serial data output)
13	B1	I/O		33	D4/RX	I	(Serial data input)
14	B2	I/O		34	D5//CK	O	(Clock for serial operation)
15	B3	I/O	Port B	35	D6//INT2	I	(Interrupt request 2)
16	B4	I/O		36	/STBY	I	(Standby mode signal)
17	B5	I/O		37	TIMER	I	Timer
18	B6	I/O		38	XTAL	O	Clock
19	B7	I/O		39	EXTAL	I	
20	VSS		Ground	40	VCC		Power supply

● **AK5351-VF-E2** (XV510A00) **ADC** (Analog to Digital Converter)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	AINR+	I	Analog signal input (R channel +)	13	DGND	-	Digital ground
2	AINR-	I	Analog signal input (R channel -)	14	TST4	I/O	Test mode setting 4
3	VREF	O	Reference voltage	15	AMODE2		Interface clock select 2
4	VA	-	Analog power supply	16	/PD	I	Power-down mode
5	AGND	-	Analog ground	17	MCLK	I	Master clock input
6	AINL+	I	Analog signal input (L channel +)	18	SCLK	I/O	Serial data clock
7	AINL-	I	Analog signal input (L channel -)	19	LRCK	I	Input/Output channel clock
8	TST1	I/O	Test mode setting 1	20	FSYNC	I/O	Frame synch. clock
9	HPFE		HPF on/off	21	SDATA	O	Serial data output
10	TST2	I/O	Test mode setting 2	22	CMODE	I	Master clock select
11	TST3	I/O	Test mode setting 3	23	SMODE1	I	Interface clock select 1
12	VD	-	Digital power supply	24	VB	-	Digital power supply

● **PCM1716E** (XU829A00) **DAC** (Digital to Analog Converter)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	LRCK	I		15	Vcc1	-	Analog power supply (+5 V)
2	DATA	I	Data input	16	VOUTL	O	Lch, analog voltage output
3	BCK	I	Bit clock	17	NC	-	
4	CLKO	O	Clock input	18	EXTL	O	Lch, analog output
5	XTI	I	Clock input	19	AGND2L	-	Analog ground
6	XTO	O	Clock out	20	Vcc2L	-	Analog power supply (+5 V)
7	DGND	-	Digital ground	21	/ZERO	O	Zero data flag
8	VDD	-	Digital power supply (+5 V)	22	/RST	I	Reset
9	Vcc2R	-	Analog power supply (+5 V)	23	/CS/IWO	I	Chip select
10	AGND2R	-	Analog ground	24	MODE	I	Mode control select (H: Software, L: Hardware)
11	EXTR	O	Rch, analog output	25	/MUTE	I	Mute control
12	NC	-		26	MD/DM0	I	Mode control data/ De-emphasis select1
13	VOUTR	O	Rch, analog voltage output	27	MC/DM1	I	Mode control BCK/De-emphasis select2
14	AGND1	-	Analog ground	28	ML/IIS	I	Mode control Latch/input format select

● **HD63266F** (XI939A00) **FDC** (Floppy Disk Controller)

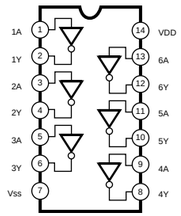
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	8"//5"	I	Data transmission speed	33	/TRKO	I	Track 00 signal
2	XTALSET	I	Clock select	34	/INDEX	I	Index signal
3	/RESET	I	Rest	35	/RDATA	I	Read data input from FDD
4	E//RD	I	Enable/Read	36	XTAL2		Clock
5	RW//WR	I	Read/write/Write	37	EXTAL2		
6	/CS	I	Chip select	38	NC		
7	/DACK	I	DMA acknowledge	39	XTAL1		Clock
8	RS0	I	Register select	40	EXTAL1		
9	RS1	I		41	VSS4		Ground
10	VSS1		Ground	42	VSS5		
11	VSS2			43	NC		
12	D0	I/O	Data bus	44	VCC2		Power supply
13	D1	I/O		45	VCC3		
14	D2	I/O		46	VCC4		
15	D3	I/O		47	/WGATE	O	Write control
16	D4	I/O		48	/WDATA	O	Writ data to FDD
17	D5	I/O		49	VSS6		Ground
18	D6	I/O		50	/STEP	O	Step signal to control head of FDD
19	D7	I/O		51	/HDIR	O	Direction
20	/DREQ	O	DMA request	52	/HLOAD	O	Head load
21	/IRQ	O	Interrupt request	53	/HSEL	O	Head select
22	/DEND	I	Data end	54	VSS7		Ground
23	VSS3		Ground	55	/DS0	O	Drive select
24	1/2 EX1			56	/DS1	O	
25	VCC1		Power supply	57	/DS2	O	
26	NUM1	I		58	/DS3	O	
27	NUM3	I		59	VSS8		Ground
28	IFS	I	Host interface select	60	/MON0	O	Motor on
29	SFORM	I	Format data	61	/MON1	O	
30	/INP	I	Index pulse	62	/MON2	O	
31	/READY	I	Ready from FDD	63	/MON3	O	
32	/WPRT	I	Write control signal	64	VSS9		Ground

● **SED1335F0B** (XQ595A00) **LCDC** (LCD Controller)

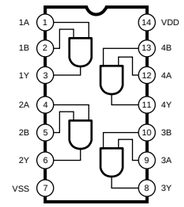
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	VA5	O	VRAM address bus	31	XD2	O	Data bus output for 4 bit dot
2	VA4	O		32	XD1	O	
3	VA3	O		33	XD0	O	
4	VA2	O		34	XECL	O	S driver enable, chain clock
5	VA1	O		35	XSCL	O	Data bus shift clock
6	VA0	O		36	Vss	-	Ground
7	/VWR	O	VRAM read/write	37	LP	O	X driver latch pulse
8	/VCE	O	Memory control	38	WF	O	Frame signal for X/Y driver
9	/VRD	-	Not used	39	YDIS	O	Power down signal for displaying off mode
10	/RES	I	Initial clear	40	YD	O	Scan start signal
11	NC	-	Not used	41	YSCL	O	Scan shift clock
12	NC	-	Not used	42	VD7	I/O	VRAM data bus
13	/RD	I	Read strobe	43	VD6	I/O	
14	/WR	I	Write strobe	44	VD5	I/O	
15	SEL2	I	Bus select	45	VD4	I/O	
16	SEL1	I	Bus select	46	VD3	I/O	
17	OSC1	I	Clock	47	VD2	I/O	
18	OSC2	O	Clock	48	VD1	I/O	
19	/CS	I	Chip select	49	VD0	I/O	
20	A0	I	Data mode select	50	VA15	O	VRAM address bus
21	Vdd	-	Power supply	51	VA14	O	
22	D0	I/O	Data bus	52	VA13	O	
23	D1	I/O		53	VA12	O	
24	D2	I/O		54	VA11	O	
25	D3	I/O		55	VA10	O	
26	D4	I/O		56	VA9	O	
27	D5	I/O		57	VA8	O	
28	D6	I/O		58	VA7	O	
29	D7	I/O		59	VA6	O	
30	XD3	O	Data bus output for 4 bit dot	60	NC	-	Not used

■ IC BLOCK DIAGRAM

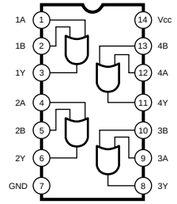
● **SN74HCU04NSR** (XC723A00)
SN74HCU04N (IG142250)
Hex Inverter
DM: IC10,16(PSR-740) IC420(PSR-640)
JACK: IC02



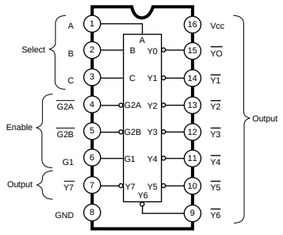
● **SN74HC08NSR** (XD831A00)
HD74LVC08FP (XU720A00)
Quad 2 Input AND
DM: IC15(PSR-740) IC370(PSR-640)



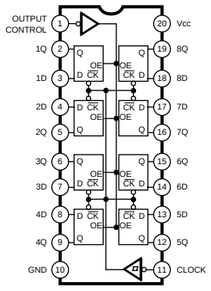
● **TC74HC32AF** (XN241A00)
Quad 2 Input OR
DM: IC14(PSR-740) IC360(PSR-640)



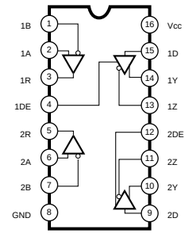
● **TC74HC138AF** (XM970A00)
TC74HC138AFEL (XW762A00)
3 to 8 Demultiplexer
DM: IC13,19(PSR-740) IC350,510(PSR-640)



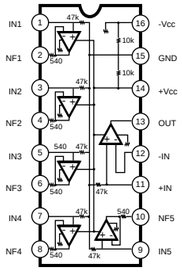
● **SN74HC374ANSR** (XQ042A00)
Octal 3-State D-Type Flip-Flop
DM: IC18,20(PSR-740) IC430,500(PSR-640)



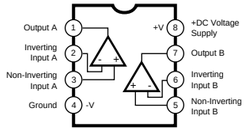
● **SN75C1168N** (XU463A00)
Line Driver / Receiver
JACK: IC01



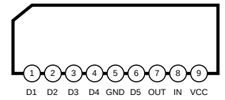
● **M5227P** (XF751A00)
5-Band Graphic Equalizer
AM: IC210,220



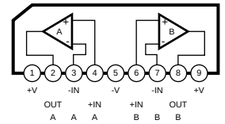
● **M5223AFP** (XV117A00)
M5223AL (XW373A00)
Dual Operational Amplifier
DM: IC33(PSR-740)
MIC: IC100(PSR-740)



● **LB1443N** (XF483A00)
LED Driver
MIC: IC001(PSR-740)



● **μPC4570HA** (XB247A00)
Dual Operational Amplifier
AM: IC320,510



TEST PROGRAM

A. PREPARATION

1) PA-6 (AC adaptor) is used.
2) The volume is usually moved to the use position when no volume change is required.
3) Measuring instruments: frequency counter, level meter (with JIS-C filter)
   Note: Connect a stereo plug to the [PHONES] jack at 33 ohms.
4) Jigs: foot switch, MIDI cable, floppy disk (2HD & 2DD)

B. HOW TO ENTER THE TEST PROGRAM

AUTO MODE

While pressing the C3#, F3 and G3# keys, turn the [STANDBY/ON] switch on.

MANUAL MODE

While pressing the C2#, F2 and G2# keys, turn the [STANDBY/ON] switch on.

C. PROCEEDING THROUGH THE TEST PROGRAM

AUTO MODE

When the test program is started, the test is automatically executed.

When confirmation is necessary, the test program stops operating and waits for the instruction. At this time, press the [START/STOP] button; the next test is automatically executed.

MANUAL MODE

The LCD will display "TEST" when entering the test program.

To select the program number, use the [BACK] and [NEXT] buttons.

To execute the test, press the [START/STOP] button.

To proceed to the next test, press the [START/STOP] button.

D. TEST PROGRAM LIST

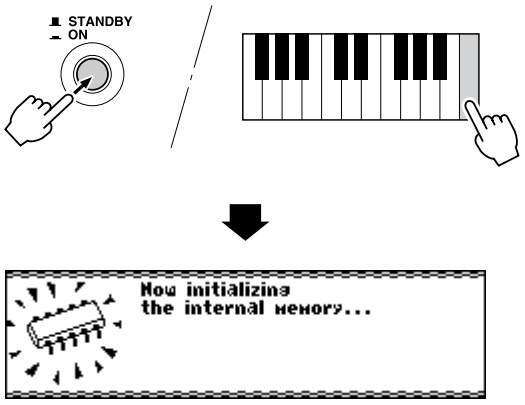
TEST NO.	LCD (initial)	Test Functions and Judgment Criteria
1	001: Version	Displays ROM version ROM (Program, Wave) versions are displayed alternately on the LCD.
2	002: Rom Chk1	Checks the ROM The test results appear on the LCD.
3	003: Ram Chk1	Checks all the RAMs that are connected to the CPU The test results appear on the LCD.
4	004: WaveRomChk1	Checks the WAVE ROMs that are connected to the CPU The test results appear on the LCD.
7	007: FDD Chk	Insert the floppy disks one by one (2DD and 2HD). Checks the floppy disk drive unit
9	009: Eff1Ram Chk	Checks the effect RAM1
10	010: Eff2Ram Chk (PSR-740 only)	Checks the effect RAM2
11	011: TG1 Chk	Outputs the sine wave by changing the channels in sequence from C1 to C6 After auto-scaling is finished, individual keys can be played. (If playing two or more keys simultaneously, the first pressed key has priority to make a sound.)
13	013: Pitch Chk	Connect the frequency counter to the [PHONES] jack. Sets PAN to Center and produces a signal at 440 +/- 0.22 Hz Check that the correct signal is produced.
14	014: Output R	Connect the level meter (with a JIS-C filter) to the [PHONES] jack. (33 ohm load) Set the [MASTER VOLUME] at maximum and check the output level (1 kHz). PHONES L: less than -50.0 dBm PHONES R: -8.0 dBm +/- 2 dB Connect the monaural plugs of the level meter (with a JIS-C filter) to the [AUX OUT] jacks. AUX OUT L: less than -50.0 dBm AUX OUT R: -6.0 dBm +/- 2 dB

15	015: Output L	Connect the level meter (with a JIS-C filter) to the [PHONES] jack. (33 ohm load) Set the [MASTER VOLUME] at maximum and check the output level (1 kHz). PHONES L: -8.0 dBm +/- 2 dB PHONES R: less than -50.0 dBm Connect the monaural plugs of the level meter (with a JIS-C filter) to the [AUX OUT] jacks. AUX OUT L: -6.0 dBm +/- 2 dB AUX OUT R: less than –50.0 dBm
19	019: D/A Noise	Connect the level meter (with a JIS-C filter) to the [PHONES] jack. (33 ohm load) Set the [MASTER VOLUME] at maximum. Check D/A converter noise. PHONES L/R: Less than -72.0 dBm (PSR-740), Less than -80.0 dBm (PSR-640)
20	020: SW,LED Chk	Check the switches on the panel. Press the switches that are displayed on the LCD. A pre-assigned note is output when pressing the switch. (With some switches, the corresponding LED will light up.) The test results appear on the LCD.
21	021: All LED On	Check that the all LEDs on the panel are on.
22	022: Red LED On	Check that the all red LEDs on the panel are on.
23	023: GreenLED on	Check that the all green LEDs on the panel are on.
28	028: All LCD On	Check that all LCD dots are on. The LCD becomes black.
29	029: All LCD Off	Check that all LCD dots are off. The LCD becomes white.
31	031: Pedal1 Chk	Connect the foot switch (FC-4 or FC-5) to the [FOOT SWITCH] jack. Check that the C3 note is output when pressing and releasing the pedal and the C4 note is output when pressing the pedal again.
33	033: PB Chk	Check that the C3 note is output when rotating the [PITCH BEND] wheel to minimum and the C4 note is output when rotating it to maximum.
34	034: MOD Chk	Check that the C3 note is output when rotating the [MODULATION] wheel to minimum and the C4 note is output when rotating it to maximum.
35	035: EXP Pedal Chk	Connect the expression pedal (FC-7) to the [FOOT VOLUME] jack. Check that the C3 note is output and the LCD displays 0 when pressing the expression pedal to the lowered position and the C4 note is output and the LCD displays 127 when backing it to the raised position.
37	037: Midi Chk	After connecting the [MIDI IN] jack and [MIDI OUT] jack with a MIDI cable, execute the test. Set the [HOST SELECT] switch to MIDI Check that the C4 note is output and that the test results appear on the LCD.
38	038: To Host Chk	For factory test use only
39	039: MIC Chk (PSR-740 only)	Connect a microphone to the [MIC/LINE IN] jack and speak to it. Set the [MIC/LINE] select switch to MIC and set the [INPUT VOLUME] at maximum. Check that the voice is converted to the 1-octave- upper tone without noise.
41	041: Rom Chk2	Checks the ROMs that are connected to the CPU. The test results appear on the LCD.
42	042: Ram Chk2	Checks the RAMs that are connected to the CPU. The test results appear on the LCD.
43	043: WaveRomChk2	Checks the WAVE ROM. The test results appear on the LCD.
46	046: BackUp Chk2	Performs the RAM back-up check. Check that the display reads “NG,” then turn off the power switch. Enter the test program and perform the RAM back-up checks, then check again. Check that the LCD displays “OK.” Note: Do not turn on the power switch by normal mode while standing by, as the RAM data will be lost.
47	047: Factory Set	All the RAMs are initialized and set to the factory preset data when executing this test. The results appear on the LCD.
48	048: Test Exit	Exit from the test program after executing this test.

* NOTE: The above tests **Nos. 41-46**, require approximately 25 minutes to conduct.
If the time is not available to perform the tests, proceed the test No.47 by pressing several the [NEXT] button.

DATA INITIALIZATION

All data can be initialized and restored to the factory preset condition by turning on the power while holding the highest (rightmost) white key on the keyboard. "Now initializing the internal memory..." will appear briefly on the display.



⚠ *CAUTION*

- ***All registration and User Style/Pad memory data, plus the other settings listed above, will be erased and/or changed when the data initialization procedure is carried out.***
- ***Carrying out the data initialization procedure will usually restore normal operation if the PSR-740/640 freezes or begins to act erratically for any reason.***

ALERT MESSAGE LIST

No file on disk! **Insert another disk.**	The disk contains no file to be loaded, copied, or be deleted. Insert the disk that contains files to be loaded, copied, or deleted.
Unformatted disk!	An unformatted disk is inserted.
Disk error!	An error occurred during execution of a disk operation. Try changing the disk. This message also may appear when executing the Load operation if the internal memory becomes full.
Disk write-protected!	The floppy disk's write-protect tab is set to ON. Remove the disk, set write-protect to off, re-insert the disk and attempt the operation again.
Disk file protected! **Can't copy or record** **this file.**	The file is a purposely "copy-protected" disk. The Copy function is not possible.
No disk! **Insert a disk.**	There is no floppy disk inserted into the disk drive. Insert a disk.
Disk removed!	An error occured because the disk was removed during a disk operation. Never remove a disk during a disk operation since this could damage both the disk and the drive.
Disk full! **Cannot continue.**	The disk's memory capacity is full and no additional data can be recorded. Delete one or more unneeded songs (using Delete), and attempt the operation again.
Wrong disk! **Reinsert** **the proper disk.**	When using the Copy operation, the inserted disk is different from the source or destination disk. Remove the disk and re-insert the proper Disk.
Same name on disk! **Change the file name.**	More than one file has the same name on the disk. Change the name.
Cannot record! **Maximum of 60 songs** **can be recorded.**	Maximum of 60 songs can be recorded. Delete one or more unneeded songs (using Delete), and attempt the song recording again.
Memory full! **Cannot continue.**	If the internal memory becomes full during Style/Pad recording, this message will appear on the display and recording will stop.

Memory full! **Clear unnecessary data.**	This message appears when executing the Quantize or Recording operations (in the Style Recording mode) when the internal memory is full.
Data not found!	This message appears when you attempt to edit, quantize or clear the track which contains no data in the Record mode.
User style full!	This message indicates that recording a new User style cannot be started when all three User styles have recorded data. Make sure to clear at least one of the three User styles before recording a new User style.
Cannot quantize the preset data.	This message appears when you attempt to edit or quantize the track (other than RHYTHM) which contains preset data in the Style Record mode.
Cannot operate during recording.	This function cannot be used during Song/Style/Pad recording.
Cannot set the MIDI function during disk operations, etc.	The MIDI function cannot be set during recording, playback, and disk operations.
Cannot turn harmony ON during Style/Pad recording.	Harmony cannot be turned on during Style/Pad recording.
Cannot turn DSP ON during Style/Pad recording.	DSP cannot be turned on during Style/Pad recording.
Cannot enter the functions during Pad recording.	This message appears to indicate you cannot enter the function when you select Multi Pad function in the Multi Pad Recording mode.
Backup error!	The backup data is faulty. Use the data initialization function.
Now initializing the internal memory...	All data can be initialized and restore to the factory preset condition by turning the STANDBY switch ON while holding the highest (rightmost) white key on the keyboard.
Host is offline!	This message may appear when the Host Select switch is set appropriately and the serial cable is connected to the TO HOST but not to the PC's serial port (or the cable is properly connected to the PC which is currently turned off).

■PSR-740 CIRCUIT DIAGRAM (DM1/2, MKS3, MKH, MKL, INV)

MKS3

CPU

28CC1-8812655

MKH

28CC1-8811360

MKL

28CC1-8811360

DM 1/2

FDC

CPU

DECODER

SRAM 1M

DRAM 4M

DRAM 4M

EPROM MAIN1 32M

EPROM MAIN2 32M

AND

OR

OR

AND

OR

INVETER

D-FF

TRANSISTOR ARRAY

TRANSISTOR ARRAY

DECODER

TRANSISTOR ARRAY

D-FF

TRANSISTOR ARRAY

SRAM 256K

INVERTER

LCDC

INVERTER

to PN1-CN8

to JACK-JK5

to MIC-JACK - CN5

to AM-CN310

to PN1-CN2

to PN1-CN1

REGULATOR +9V

REGULATOR +5V

DC-DC CONVERTER

Floppy Disk Drive

N.C.

28CC1-8814267

LCD

to Back - light Assembly

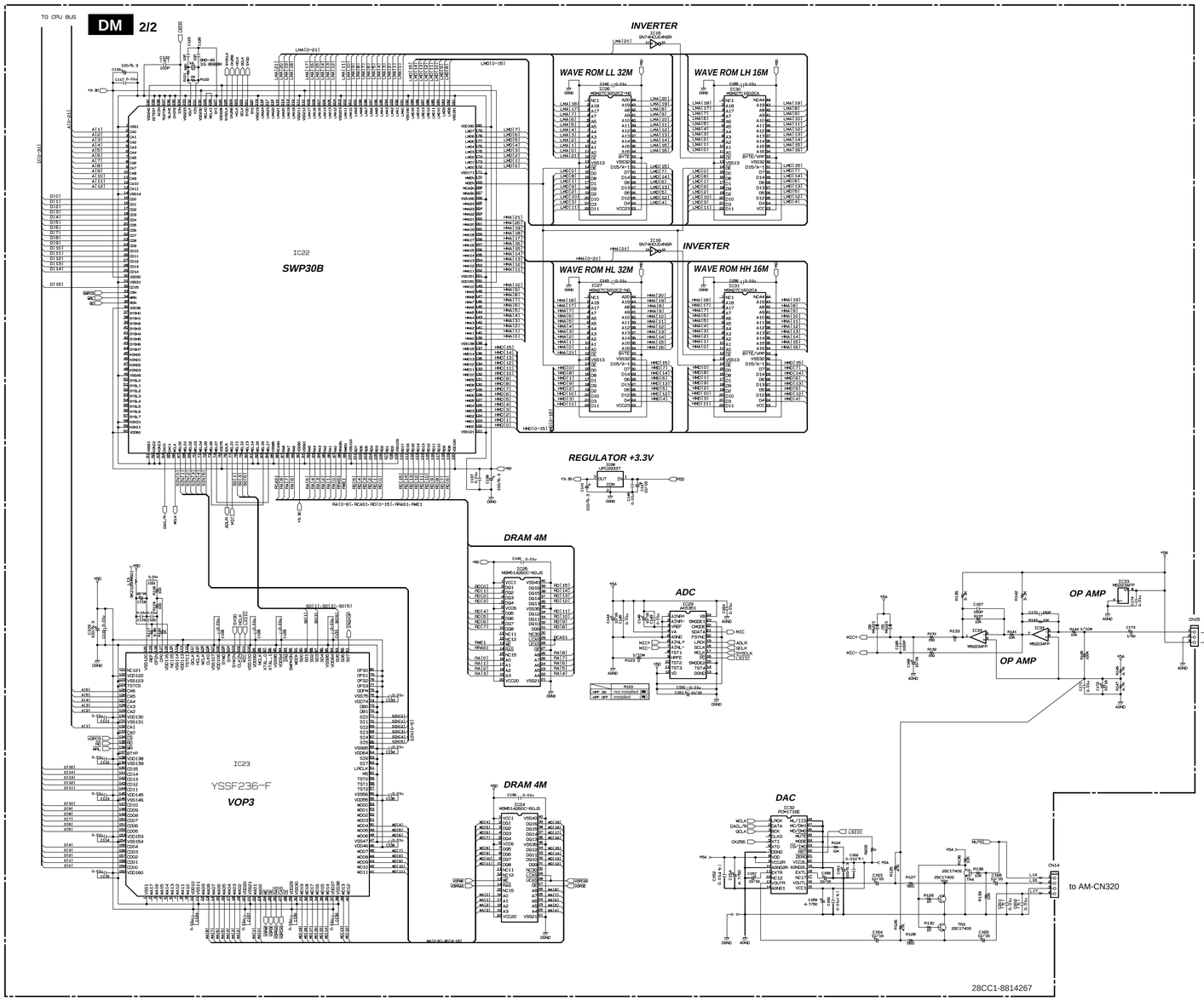
INV

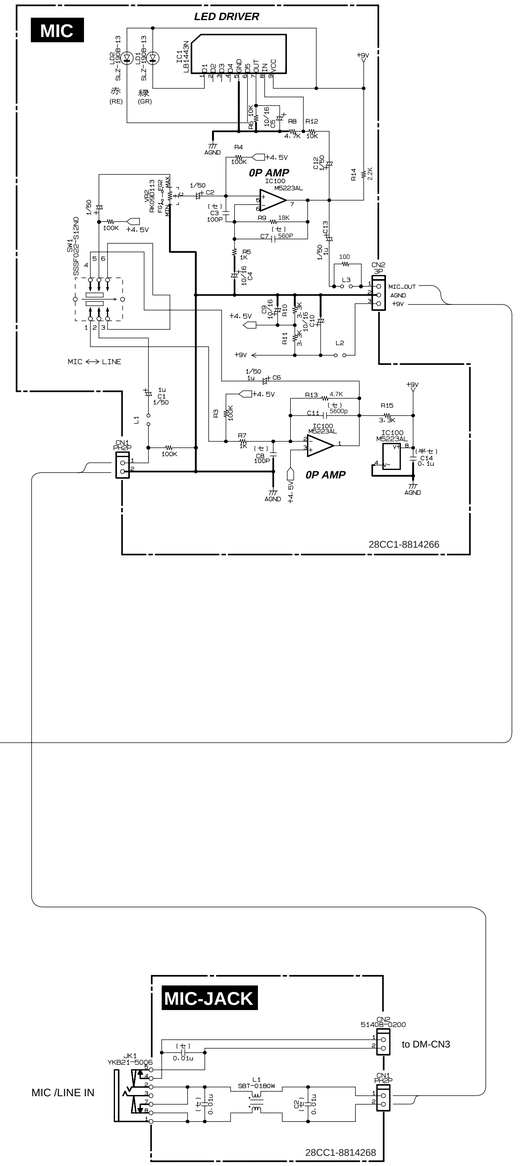
2NA-8814265

(セ): Ceramic Capacitor
(マ): Mylar Capacitor
酸金: Metal Oxide Film Resistor

Note : See parts list for details of circuit board component parts

■PSR-740 CIRCUIT DIAGRAM (DM2/2, MIC-JACK, MIC)





to AM-CN320

(セ): Ceramic Capacitor
(半セ): Semi-Conductive Ceramic Capacitor

Note : See parts list for details of circuit board component parts

PSR-740

■PSR-640 CIRCUIT DIAGRAM (DM, MKS3, MKH, MKL, INV)

MKS3

CPU

28CC1-8812655

MKH

28CC1-8811360

MKL

28CC1-8811360

DM

RESET

DECODER

OR

AND

DECODER

AND

D-FF

LATCH

TRANSISTOR ARRAY

DECODER

DEC

TRANSISTOR ARRAY

D - FF

LATCH

SRAM 1M

PROGRAM1 ROM H 32M

DRAM 16M

PROGRAM2 ROM L32M

IC100
SH7043
CPU

SWX00B
IC200

ROM WAVE1 32M

ROM WAVE2 32M

DRAM 4M

REGULATOR +3.3V

REGULATOR +5V

DAC

IC400
SED1339F0B
LCDC

SRAM 256K

INVERTER

INVERTER

IC800
HD63266F
FDC

DC-DC CONVERTER

28CC1-8813199

LCD

Floppy Disk Drive

INV

2NA-8814265

to PN1-CN2

to PN1-CN1

to PN1-CN8

to JACK-JK5

to Back - light Assembly

to AM - CN310

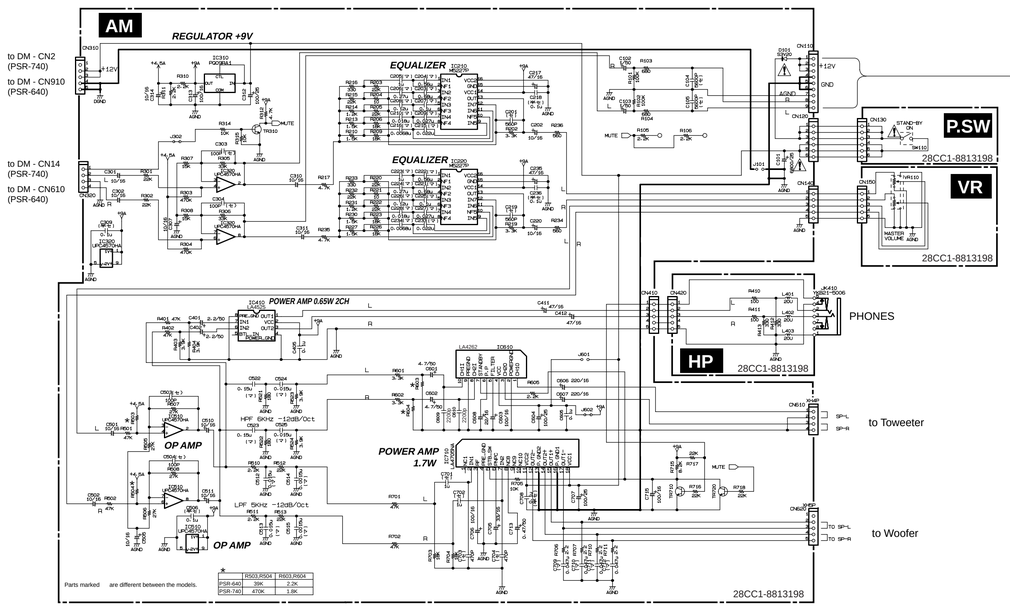
to AM - CN320

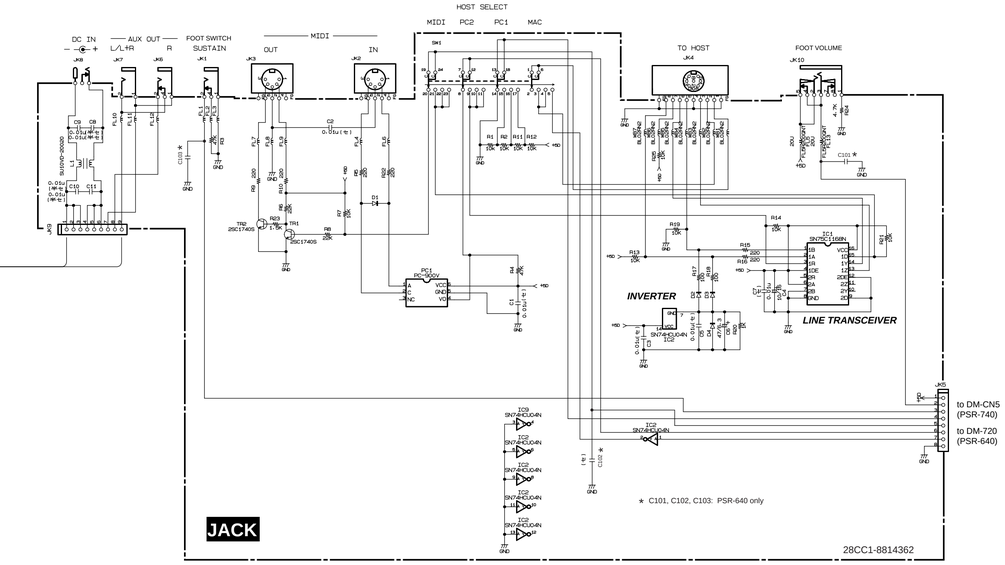
Note : See parts list for details of circuit board component parts

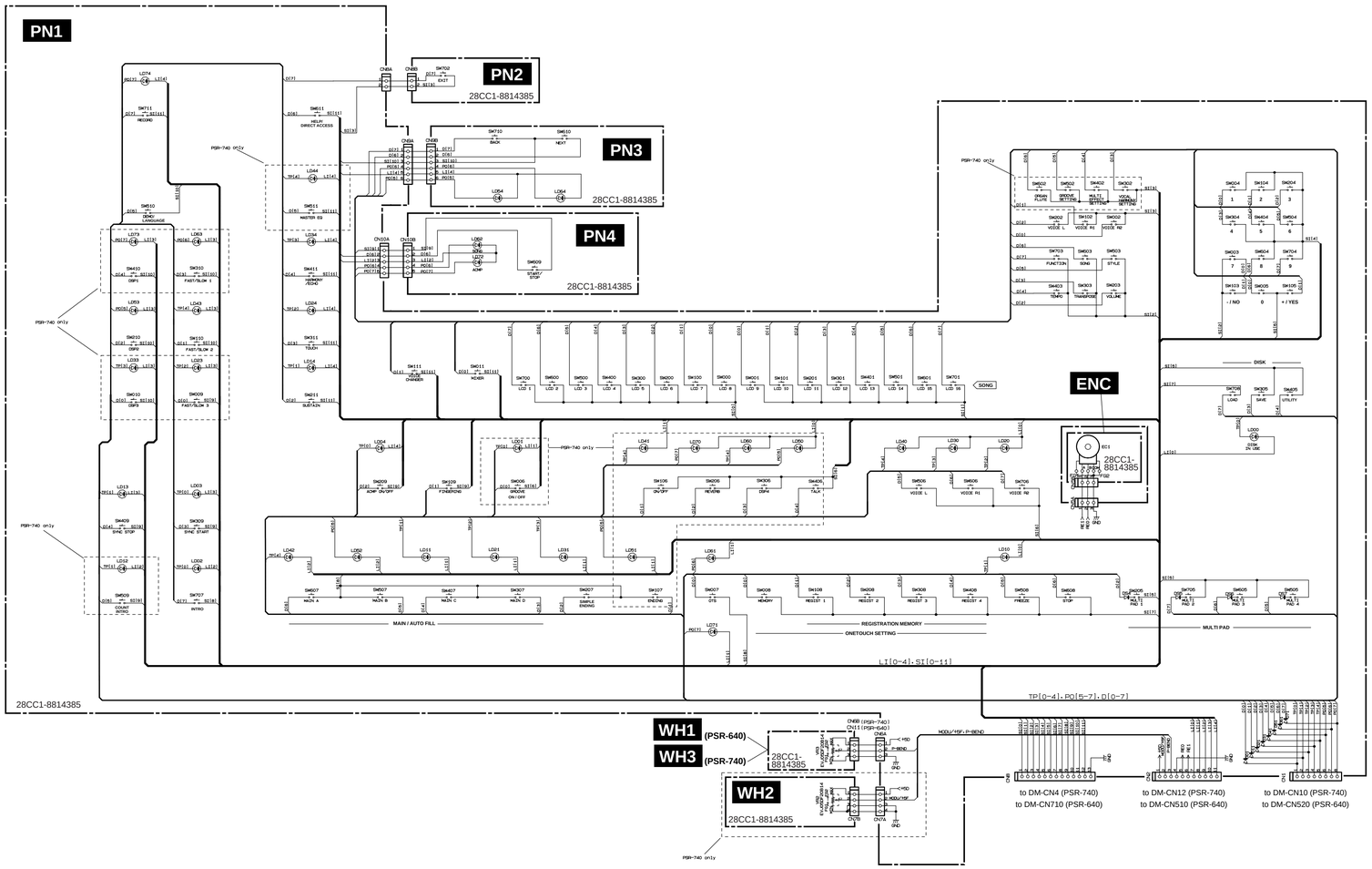
(セラ): Ceramic Capacitor

(マ): Mylar Capacitor

■PSR-740 / PSR-640 OVERALL CIRCUIT DIAGRAM (AM, HP, P.SW, VR, JACK, PN1, PN2, PN3, PN4, WH1, WH2, WH3, ENC)







- •NJM78L05A-T3(X)757A00) REGULATOR +5V — 1: OUTPUT 2: COMMON 3: INPUT
- •NJM78L05A(XJ596A00) REGULATOR +5V — 1: OUTPUT 2: COMMON 3: INPUT
- •PQ09RA1(XQ774A00) REGULATOR +9V — 1: IN 2: OUT 3: GND 4: ON/OFCont.
- • µPC2933T-E1(XS516A00) • µPC29M33T-E1(XU965A00) REGULATOR +3.3V — 1: V in 2: GND 3: V out
- •SI-8050S(LF1103) (XT514A00) REGULATOR +5V — 1: V in 2: SW out 3: GND 4: V os 5: S.S
- •AN77L09-TA (XT676A00) REGULATOR +9V — 1: OUTPUT 2: COMMON 3: INPUT
- •S3V20 (VR313500) DIODE — 1: ANODE 2: CATHODE

Note : See parts list for details of circuit board component parts

■ TO SERVICE PERSONNEL

Critical Components Infomation
Components having special characteristics are marked ⚠ and must be replaced with parts having specifications equel to those originally installed.

(セ): Ceramic Capacitor
(MセI): Semi-Conductive Ceramic Capacitor
(マ): Mylar Capacitor

PSR-740 / PSR-640