PORTATONE

PSR-540

SERVICE MANUAL

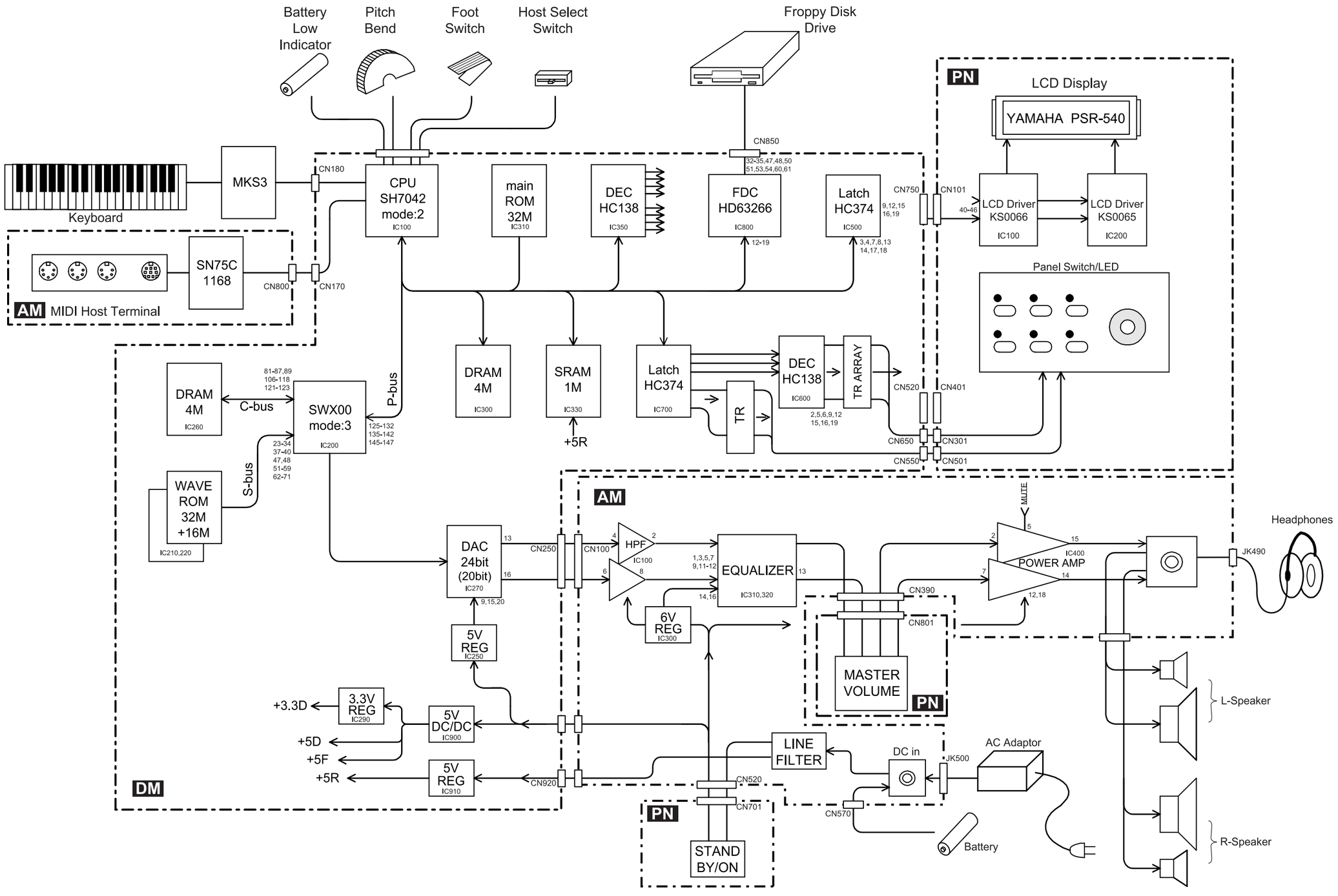
■ **CONTENTS**

PK 001629

YAMAHA

HAMAMATSU,JAPAN
1.45K-536 Ⓘ Printed in Japan'99.06

■ BLOCK DIAGRAM



28CA1-8813687

LSI PIN DESCRIPTION

HG73C205AFD (XU947C00) SWX00B **TONE GENERATOR**

(DM IC200)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	ICN	I	Initial clear	85	CMA3	O	Program address bus
2	RFCLKI	I	PLL Clock	86	CMA8	O	Program address bus
3	TM2	I	PLL Control	87	CMA2	O	Program address bus
4	AVDD_PLL		Power supply	88	CRD	O	read signal
5	AVSS_PLL		Ground	89	CMA1	O	Program address bus
6	MODE0	I	SWX dual mode	90	CUB	O	high byte effective signal
7	VCC7		Power supply	91	VCC91		Power supply
8	GND8		Ground	92	GHND92		Ground
9	XIN	I	crystal oscillator	93	CS1	O	CS signal
10	XOUT	O	crystal oscillator	94	CMA0	O	Program address bus
11	MODE1	I	SWX separate mode	95	CLB	O	low byte effective signal
12	TEST0	I	TEST pin	96	CMA12	O	Program address bus
13	TESTON	I	TEST pin	97	CMA11	O	Program address bus
14	AN0-P40	I	A/D converter	98	CMA10	O	Program address bus
15	AN1-P41	I	A/D converter	99	CMA9	O	Program address bus
16	AN2-P42	I	A/D converter	100	GND100		Ground
17	AN3-P43	I	A/D converter	101	CWE	O	write signal
18	AVDD_AN		Power supply	102	CMA16	O	Program address bus
19	AVSS_AN		Ground	103	CMA15	O	Program address bus
20	TXD0	O	for MIDI or TO-HOST	104	CMA14	O	Program address bus
21	TXD1	O	for MIDI	105	CMA13	O	Program address bus
22	EXCLK	I	Crystal oscillator	106	CMD8	I/O	Program memory Data bus
23	SMD11	I/O	Wave memory data bus	107	CMD7	I/O	Program memory Data bus
24	SMD4	I/O	Wave memory data bus	108	CMD9	I/O	Program memory Data bus
25	SMD3	I/O	Wave memory data bus	109	CMD6	I/O	Program memory Data bus
26	SMD12	I/O	Wave memory data bus	110	CMD10	I/O	Program memory Data bus
27	SMD10	I/O	Wave memory data bus	111	CMD5	I/O	Program memory Data bus
28	SMD5	I/O	Wave memory data bus	112	CMD11	I/O	Program memory Data bus
29	SMD2	I/O	Wave memory data bus	113	CMD4	I/O	Program memory Data bus
30	SMD13	I/O	Wave memory data bus	114	CMD12	I/O	Program memory Data bus
31	SMD9	I/O	Wave memory data bus	115	CMD3	I/O	Program memory Data bus
32	SMD6	I/O	Wave memory data bus	116	CMD13	I/O	Program memory Data bus
33	SMD1	I/O	Wave memory data bus	117	CMD2	I/O	Program memory Data bus
34	SMD14	I/O	Wave memory data bus	118	CMD14	I/O	Program memory Data bus
35	VCC35		Power supply	119	VCC119		Power supply
36	GND36		Ground	120	GND115		Ground
37	SMD8	I/O	Wave memory data bus	121	CMD1	I/O	Program memory Data bus
38	SMD7	I/O	Wave memory data bus	122	CMD15	I/O	Program memory Data bus
39	SMD0	I/O	Wave memory data bus	123	CMD0	I/O	Program memory Data bus
40	SMD15	I/O	Wave memory data bus	124	CMA21	O	Program address bus
41	SOE	O	read signal	125	PDT15	I/O	SWX access data bus
42	SWE	O	write signal	126	PDT14	I/O	SWX access data bus
43	SRAS	O	RAS signal	127	PDT13	I/O	SWX access data bus
44	SCAS	O	CAS signal	128	PDT12	I/O	SWX access data bus
45	REFRESH	O	REFRESH signal	129	PDT11	I/O	SWX access data bus
46	CS0	O	CS signal	130	PDT10	I/O	SWX access data bus
47	SMA0	O	Memory address bus	131	PDT9	I/O	SWX access data bus
48	SMA16	O	Memory address bus	132	PDT8	I/O	SWX access data bus
49	VCC49		Power supply	133	VCC133		Power supply
50	GND50		Ground	134	GND134		Ground
51	SMA1	O	Memory address bus	135	PDT7	I/O	SWX access data bus
52	SMA15	O	Memory address bus	136	PDT6	I/O	SWX access data bus
53	SMA2	O	Memory address bus	137	PDT5	I/O	SWX access data bus
54	SMA14	O	Memory address bus	138	PDT4	I/O	SWX access data bus
55	SMA3	O	Memory address bus	139	PDT3	I/O	SWX access data bus
56	SMA13	O	Memory address bus	140	PDT2	I/O	SWX access data bus
57	SMA4	O	Memory address bus	141	PDT1	I/O	SWX access data bus
58	SMA12	O	Memory address bus	142	PDT0	I/O	SWX access data bus
59	SMA5	O	Memory address bus	143	VCA143		Power supply
60	GND60		Ground	144	GND144		Ground
61	VCC61		Power supply	145	PAD2	I	SWX access address bus
62	SMA11	O	Memory address bus	146	PAD1	I	SWX access address bus
63	SMA6	O	Memory address bus	147	PAD0	I	SWX access address bus
64	SMA10	O	Memory address bus	148	VCC148		Power supply
65	SMA7	O	Memory address bus	149	GND149		Ground
66	SMA9	O	Memory address bus	150	PCS	I	Chip select
67	SMA17	O	Memory address bus	151	PWR	I	write enable
68	SMA8	O	Memory address bus	152	PRD	I	read enable
69	SMA18	O	Memory address bus	153	RXD0	I	for Midi or TO-HOST
70	SMA19	O	Memory address bus	154	RXD1	I	for Midi or Key scan
71	SMA20	O	Memory address bus	155	SCLKI	I	EXT Clock
72	SMA21	O	Memory address bus	156	ADIN	I	A/D converter
73	SMA22	O	Memory address bus	157	ADLR	O	A/D converter LR clock
74	SMA23	O	Memory address bus	158	DO0	O	DAC
75	CMA20	O	Program address bus	159	DO1	O	DAC
76	CMA19	O	Program address bus	160	SYSCLK	O	1/2 clock
77	VCC77		Power supply	161	VCC161		Power supply
78	GND78	O	Ground	162	GND162		Ground
79	CMA18	O	Program address bus	163	WCLK	O	for DAC LR clock
80	CMA17	O	Program address bus	164	QCLK	O	1/12 clock
81	CMA5	O	Program address bus	165	BCLK	O	IIS-DAC clock
82	CMA6	O	Program address bus	166	SYI	I	Synch signal
83	CMA4	O	Program address bus	167	IRQ0	I	Interrupt request
84	CMA7	O	Program address bus	168	NMI	I	Interrupt request

HD63266F (XI939A00) **FDC** (Floppy Disk Controller)

(DM IC800)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	8"//5"	I	Data transmission speed	33	/TRKO	I	Track 00 signal
2	XTALSET	I	Clock select	34	/INDEX	I	Index signal
3	/RESET	I	Rest	35	/RDATA	I	Read data input from FDD
4	E//RD	I	Enable/Read	36	XTAL2		Clock
5	RW//WR	I	Read/write/Write	37	EXTAL2		
6	/CS	I	Chip select	38	NC		
7	/DACK	I	DMA acknowledge	39	XTAL1		Clock
8	RS0	I	Register select	40	EXTAL1		
9	RS1	I		41	VSS4		Ground
10	VSS1		Ground	42	VSS5		
11	VSS2			43	NC		
12	D0	I/O		44	VCC2		
13	D1	I/O		45	VCC3		Power supply
14	D2	I/O		46	VCC4		
15	D3	I/O	Data bus	47	/WGATE	O	Write control
16	D4	I/O		48	/WDATA	O	Writ data to FDD
17	D5	I/O		49	VSS6		Ground
18	D6	I/O		50	/STEP	O	Step signal to control head of FDD
19	D7	I/O		51	/HDIR	O	Direction
20	/DREQ	O	DMA request	52	/HLOAD	O	Head load
21	/IRQ	O	Interrupt request	53	/HSEL	O	Head select
22	/DEND	I	Data end	54	VSS7		Ground
23	VSS3		Ground	55	/DS0	O	
24	1/2 EX1			56	/DS1	O	Drive select
25	VCC1		Power supply	57	/DS2	O	
26	NUM1	I		58	/DS3	O	
27	NUM3	I		59	VSS8		Ground
28	IFS	I	Host interface select	60	/MON0	O	
29	SFORM	I	Format data	61	/MON1	O	Motor on
30	/INP	I	Index pulse	62	/MON2	O	
31	/READY	I	Ready from FDD	63	/MON3	O	
32	/WPRT	I	Write control signal	64	VSS9		Ground

KS0065B(XV933A00) **LCD DRIVER**

(PN IC200)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	SC29	O		31	Vcc		LCD driver circuit (-5V)
2	SC28	O		32	CL1	I	Data shift
3	SC27	O		33	CL2	I	Latch clock
4	SC26	O		34	GND(Vss)		GND (0V)
5	SC25	O		35	DL1	I/O	
6	SC24	O		36	DR1	I/O	
7	SC23	O		37	DL2	I/O	Data input / output
8	SC22	O		38	DR2	I/O	
9	SC21	O		39	NC		
10	SC20	O		40	M	I	Alternated signal for LCD driver output
11	SC19	O		41	SHL1	I	Data interface
12	SC18	O	Segment signal output	42	SHL2	I	Data interface
13	SC17	O	for LCD driving	43	FCS	I	Mods selection
14	SC16	O		44	V1	I	
15	SC15	O		45	V2	I	
16	SC14	O		46	V3	I	Power supply
17	SC13	O		47	V4	I	
18	SC12	O		48	V5	I	
19	SC9	O		49	V6	I	
20	SC10	O		50	SC40	O	
21	SC11	O		51	SC39	O	
22	SC8	O		52	SC38	O	
23	SC7	O		53	SC37	O	
24	VDD		Power supply	54	SC36	O	Segment signal output
25	SC6	O		55	SC35	O	for LCD driving
26	SC5	O		56	SC30	O	
27	SC4	O	Segment signal output	57	SC31	O	
28	SC3	O	for LCD driving	58	SC32	O	
29	SC2	O		59	SC33	O	
30	SC1	O		60	SC34	O	

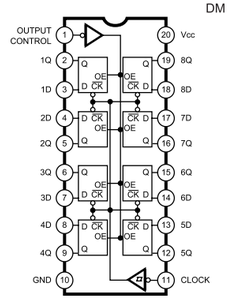
KS0066U-10B(XV226A00) LCD DRIVER

(PN IC100)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	S22	O		41	DB2	I/O	
2	S21	O		42	DB3	I/O	
3	S20	O		43	DB4	I/O	Data interface
4	S19	O		44	DB5	I/O	
5	S18	O		45	DB6	I/O	
6	S17	O		46	DB7	I/O	
7	S16	O		47	C1	O	
8	S15	O		48	C2	O	
9	S14	O		49	C3	O	
10	S13	O		50	C4	O	
11	S12	O	Segment signal output for LCD	51	C5	O	
12	S11	O	driving	52	C6	O	
13	S10	O		53	C7	O	
14	S9	O		54	C8	O	Common signal output for LCD
15	S8	O		55	C9	O	driving
16	S7	O		56	C10	O	
17	S6	O		57	C11	O	
18	S5	O		58	C12	O	
19	S4	O		59	C13	O	
20	S3	O		60	C14	O	
21	S2	O		61	C15	O	
22	S1	O		62	C16	O	
23	Vss		Ground	63	S40	O	
24	OSC1	I	Oscillator	64	S39	O	
25	OSC2	O	Oscillator	65	S38	O	
26	V1			66	S37	O	
27	V2			67	S36	O	
28	V3		Power supply	68	S35	O	
29	V4			69	S34	O	
30	V5			70	S33	O	
31	CLK1	O	Data latch clock	71	S32	O	Segment signal output for LCD
32	CLK2	O	Data shift clock	72	S31	O	driving
33	Vdd		Power supply (+5V)	73	S30	O	
34	M	O	Altemated signal for LCD driver output	74	S29	O	
35	D	O	Display data interface	75	S28	O	
36	RS	I		76	S27	O	
37	R/W	I	Read / write	77	S26	O	
38	E	I	Enable	78	S25	O	
39	DB0	I/O	Data interface	79	S24	O	
40	DB1	I/O	Data interface	80	S23	O	

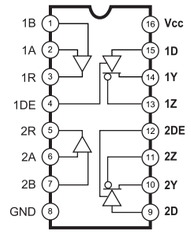
● **74HC374** (IR037400)
Octal 3-State D-Type Flip-Flop

DM IC500, 700



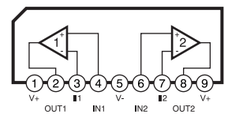
● **SN75C1168N**(XU463A00)
Line Driver/Receiver

AM IC700



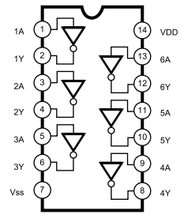
● μ **PC4572HA**(XF633A00)
Dual Operational Amplifier

AM IC100



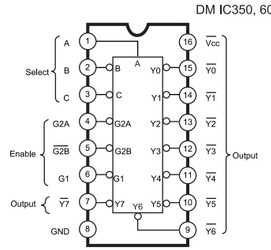
● **SN74HCU04N** (IG142250)
Hex Inverter

AM IC810



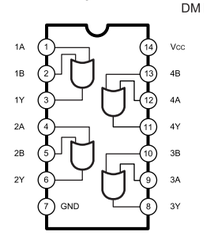
● **TC74HC138AP**(IR013850)
3 to 8 Demultiplexer

DM IC350, 600



● **TC74HC32AP(IR003200)**
Quad 2 Input OR

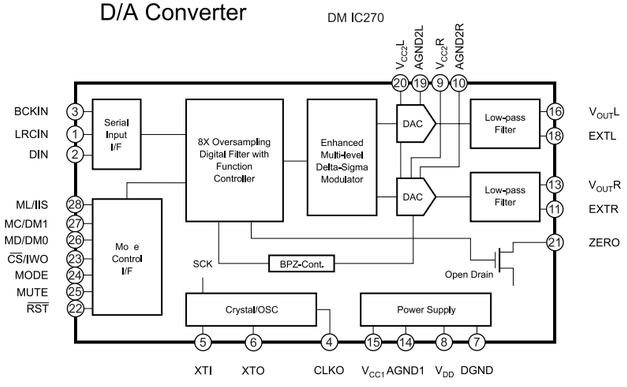
DM IC360



■ IC BLOCK DIAGRAM

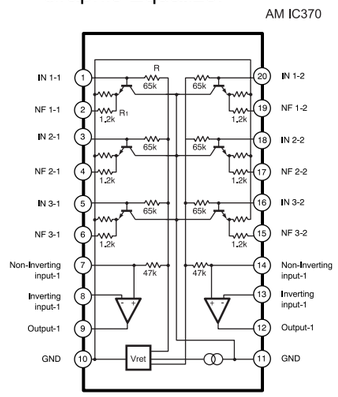
● **PCM1716E/T2** (XU829A00)
D/A Converter

DM IC270



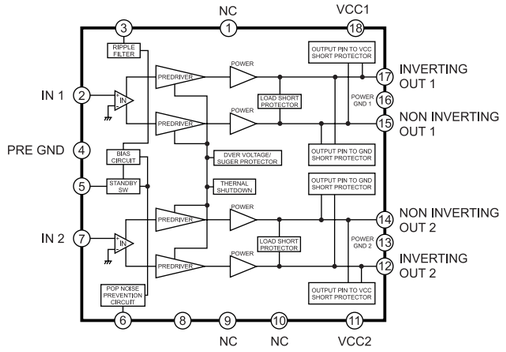
● **M5243AP06** (XU911A00)
Graphic Equalizer

AM IC370



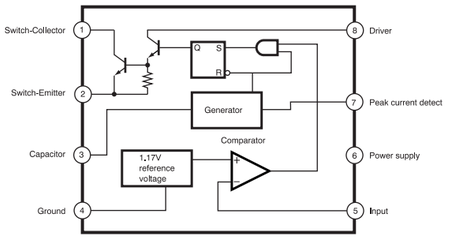
● **LA4705NA** (XQ619A00)
Power Amplifier

AM IC400



● **M5291P** (XV856A00)
DA / DA Converter

DM IC900



■ TEST PROGRAM & INITIALIZE

1. TEST PROGRAM

A. PREPARATION

1) PA-6 (AC adapter) is used.
2) The volume is usually moved to the use position when no volume change is required.
3) Measuring instruments:
   Frequency counter
   Level meter (with JIS-C filter)
   Note: Use a stereo plug to the [PHONES / AUX OUT] jack at 33 ohms.
4) Jigs:
   Foot switch, MIDI cable, Floppy Disk(2HD, 2DD)

B. HOW TO ENTER THE TEST PROGRAM

AUTO MODE

While pressing the C3#, F3 and G3# keys, turn the [STAND BY/ON] switch to the “ON” position.

MANUAL MODE

While pressing the C2#, F2 and G2# keys, turn the [STAND BY/ON] switch to the “ON” position.

C. PROCEEDING THROUGH THE TEST PROGRAM

AUTO MODE

When the test program is started, the test is automatically executed.
When confirmation is necessary, the test program stops operating and waits for instruction. At this time, press the [START/STOP] button; the next test is automatically executed.

MANUAL MODE

The LCD will display “TEST” when entering the test program.
To select the program number, use the [BANK +] and [NEXT -] buttons.
To execute the test, press the [START/STOP] button.
To proceed to the next test, press the [START/STOP] button.

D. TEST PROGRAM LIST

TEST.NO	LCD(initial)	Test functions and Judgement Criteria
1	001: Version	Displays Rom version Rom (Program, Wave) versions are displayed alternately on the LCD.
2	002: Rom Chk1	Checks the ROM The tset results appear on the LCD.
3	003: Ram Chk1	Checks all the RAMs that are connected to the CPU. The test results appear on the LCD.
4	004: WaveRomChk1	Checks the WAVE ROMs that are connected to the CPU. The test results appear on the LCD.
7	007: FDD Chk	Insert the floppy disks one by one (2DD and 2HD). Checks the floppy disk drive unit
9	009: Eff1Ram Chk	Checks the effect RAM1
11	011: TG1 Chk	Outputs the sine wave by changing the channels in sequence from C2 to G4. After auto-scaling is finished, individual keys can be played. (If playing two or more keys simultaneously, the first pressed key has priority to make a sound.)
13	013: Pitch Chk	Connect the frequency counter to the [PHONE/AUX OUT] jack. Set PAN to Center and produce a signal at 440 Hz +/- 0.22. Check that the correct signal is produced.
14	014: Output R	Connect the level meter (with a JIS-C filter) to the [PHONE/AUX OUT] jack. (33 ohm load) Set the [MASTER VOLUME] at maximum. Check the output level (1kHz). Phones L: Less than -60.0 dBm Phones R: -10 dBm +/- 2 dB
15	015: Output L	Connect the level meter (with a JIS-C filter) to the [PHONE/AUX OUT] jack. (33 ohm load) Set the [MASTER VOLUME] at maximum. Check the output level (1kHz). Phones L: -10 dBm +/- 2 dB Phones R: Less than -60.0 dBm
19	019: D/A Noise	Connect the level meter (with a JIS-C filter) to the [PHONE/AUX OUT] jack. (33 ohm load) Set the [MASTER VOLUME] at maximum. Phones L/R: Less than -80 dBm
20	020: SW, LED Chk	Check the switches on the panel. Press the switches that are displayed on the LCD. A pre-assigned note is output when pressing the switch. The test results appear on the LCD.
21	021: ALL LED On	Check that the LED on the panel is on.
22	022: Red LED On	Check that the red LED on the panel is on.
23	023: Green LED On	Check that the green LED on the panel is on.
28	028: All LCD On	Check that all LCD dots are on.
29	029: All LCD Off	Check that all LCD dots are off. The LCD becomes white
31	031: Pedal1 Chk	Connect the foot switch to the [FOOT SWITCH] jack. Check that the C3 note is output when starting the test program. Check that the C4 note is output when pressing the pedal and that the tone is turned off when releasing the pedal. The test results appear on the LCD.
37	037: Midi Chk	After connecting the [MIDI IN] jack and [MIDI OUT] jack with a MIDI cable, execute the test. Check that the C4 note is output and that the test results appear on the LCD.
38	038: To Host Chk	For factory test use only
40	040: Battery Chk	Checks the voltage of the Battery terminal
41	041: Rom Chk2	Checks the ROM The test results appear on the LCD.
42	042: Ram Chk2	Checks the RAMs that are connected to the CPU. The test results appear on the LCD.
43	043: WaveRom Chk2	Checks the WAVE ROMs that are connected to the CPU. The test results appear on the LCD.
44	044: WaveRam Chk1	Checks all the WAVE RAMs that are connected to the CPU. The test results appear on the LCD.
46	046: Backup Chk2	Performa the RAM back-up check. Check that the display reads “NG,” then turn off the power switch. Enter the test program and perform the RAM back-up checks, then check again. Check that the LCD displays “OK.” Note: Do not turn on the power switch by normal mode while standing by, as the RAM data will be lost.
47	047: Factry Set	All the RAMs are initialized and set to the factory preset date when executing this test. The results appear on the LCD.
48	048: Test Exit	Exit from the test program after executing this test.

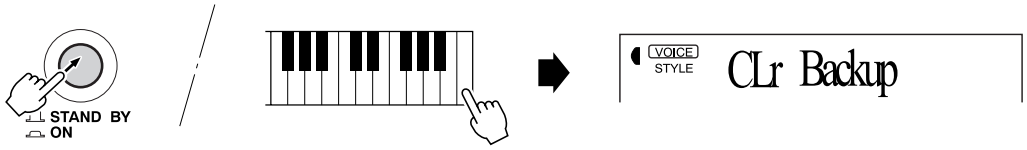
2. INITIALIZE

Except for the data listed below, all PSR-540 panel settings are reset to their initial settings whenever the power is turned on. The data listed below are backed up (i.e. retained in the memory) as long as either an AC adaptor is connected or a set of batteries is installed.

- User Song Data
- User One Touch Setting Data
- One Touch Setting Bank Number
- EZ Chord Data
- EZ Chord Bank Number Data
- Smart Chord Number
- Metronome Volume
- Touch On/Off
- Touch Sensitivity
- Split Point
- Accompaniment Split Point
- Footswitch Assign Function

Data Initialization

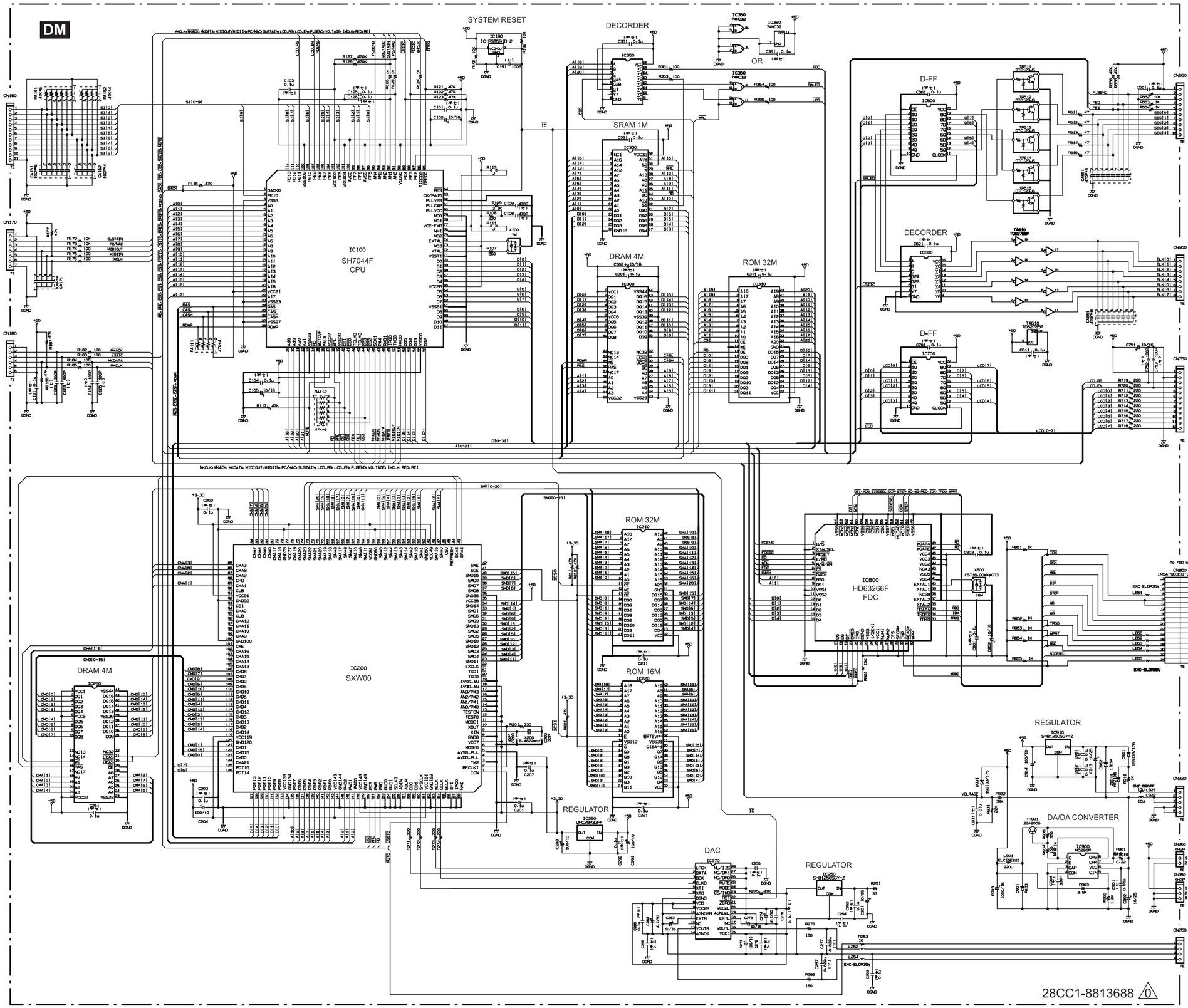
All data can be initialized and restored to the factory preset condition by turning on the power while holding the highest (rightmost) white key on the keyboard. “CLr Backup” will appear briefly on the display.



CAUTION

- All one touch setting (user) and song memory data, plus the other settings listed above, will be erased and/or changed when the data initialization procedure is carried out.
- Carrying out the data initialization procedure will usually restore normal operation if the PSR-540 freezes or begins to act erratically for any reason.

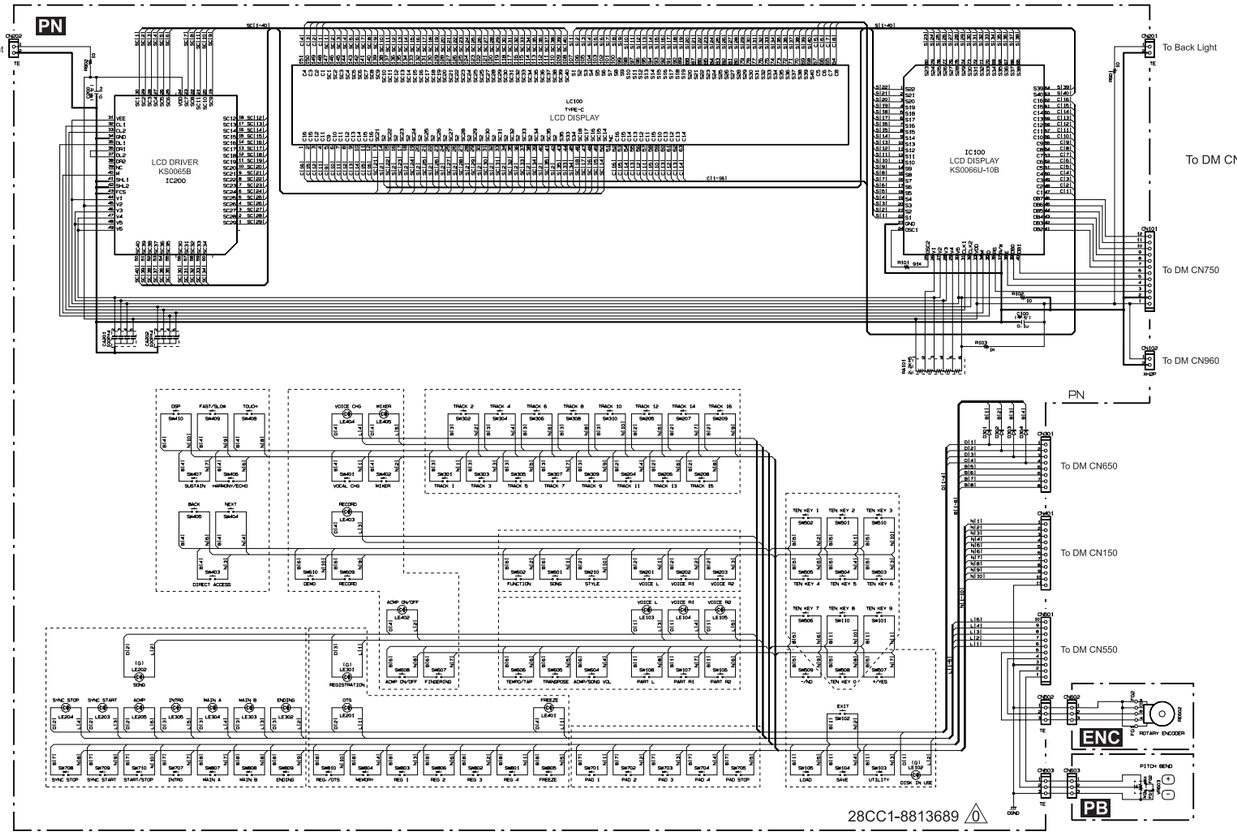
■ OVERALL CIRCUIT DIAGRAM 1/2 (DM)

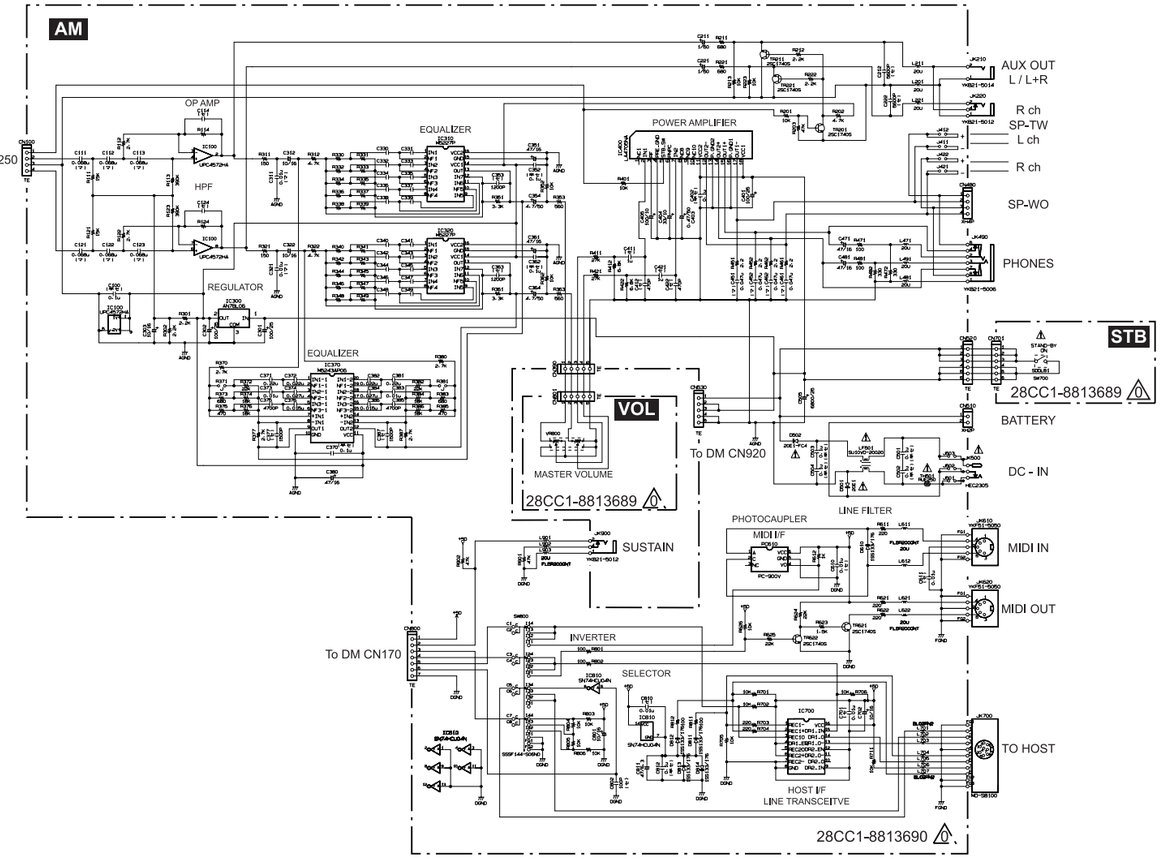


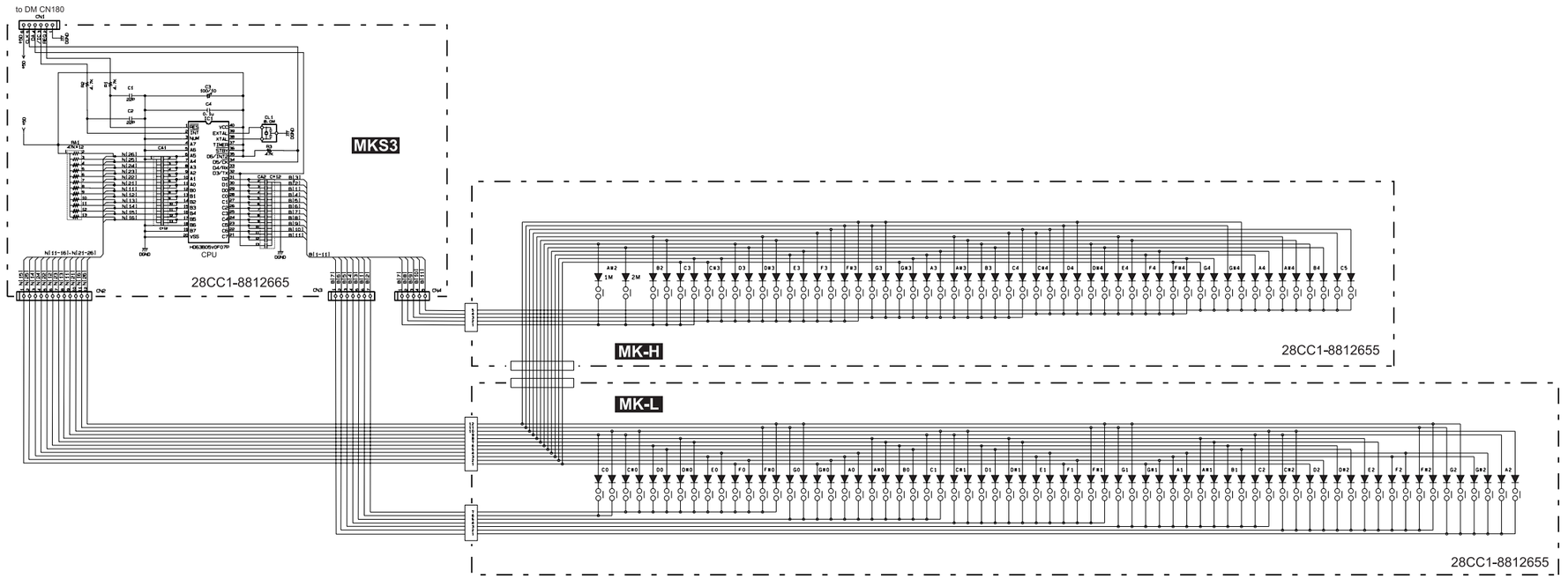
(マ): Mylar Capacitor
(セ): Ceramic Capacitor
(半セ): Semiconductive Ceramic Capacitor

Note: See parts list for details of circuit board component parts.

■ OVERALL CIRCUIT DIAGRAM 2/2 (AM,PN,MKS3,MK-H,MK-L)







(マ): Mylar Capacitor
(セ): Ceramic Capacitor
(半セ): Semiconductive Ceramic Capacitor

■ WARNING
Components having special characteristics are marked ⚠ and must be replaced with parts having specification equal to those originally installed.

Note: See parts list for details of circuit board component parts.