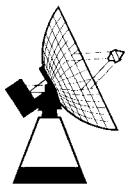
NEC

MODEL PX-50XM1A
PX-50XM1G

PlasmaSync™ Multimedia Monitor

SERVICE MANUAL

No. 005A



Better Service

Better Reputation

Better Profit

USE THIS SERVICE MANUAL WHEN SERVICING

Integra

Model PLA-50V1

SAFETY CAUTION:
Before servicing this chassis, it is important that the service technician read and follow the "Safety Precautions" and "Product Safety Notice" in this Service Manual.

WARNING:
SHOCK HAZARD - Use an isolation transformer when servicing.

NEC Corporation
TOKYO, JAPAN

TROUBLESHOOTING

1. Failure in the power supply

In the case of any abnormality in the power supply like no power available, go to “1. No power available” (P. 2).

2. Video error

(1) In the case of a video input error in VIDEO 1, 2, 3 (S-VIDEO), go to 2-1. “No video input signals available at VIDEO 1, 2, 3 (S-VIDEO)” (P. 6).

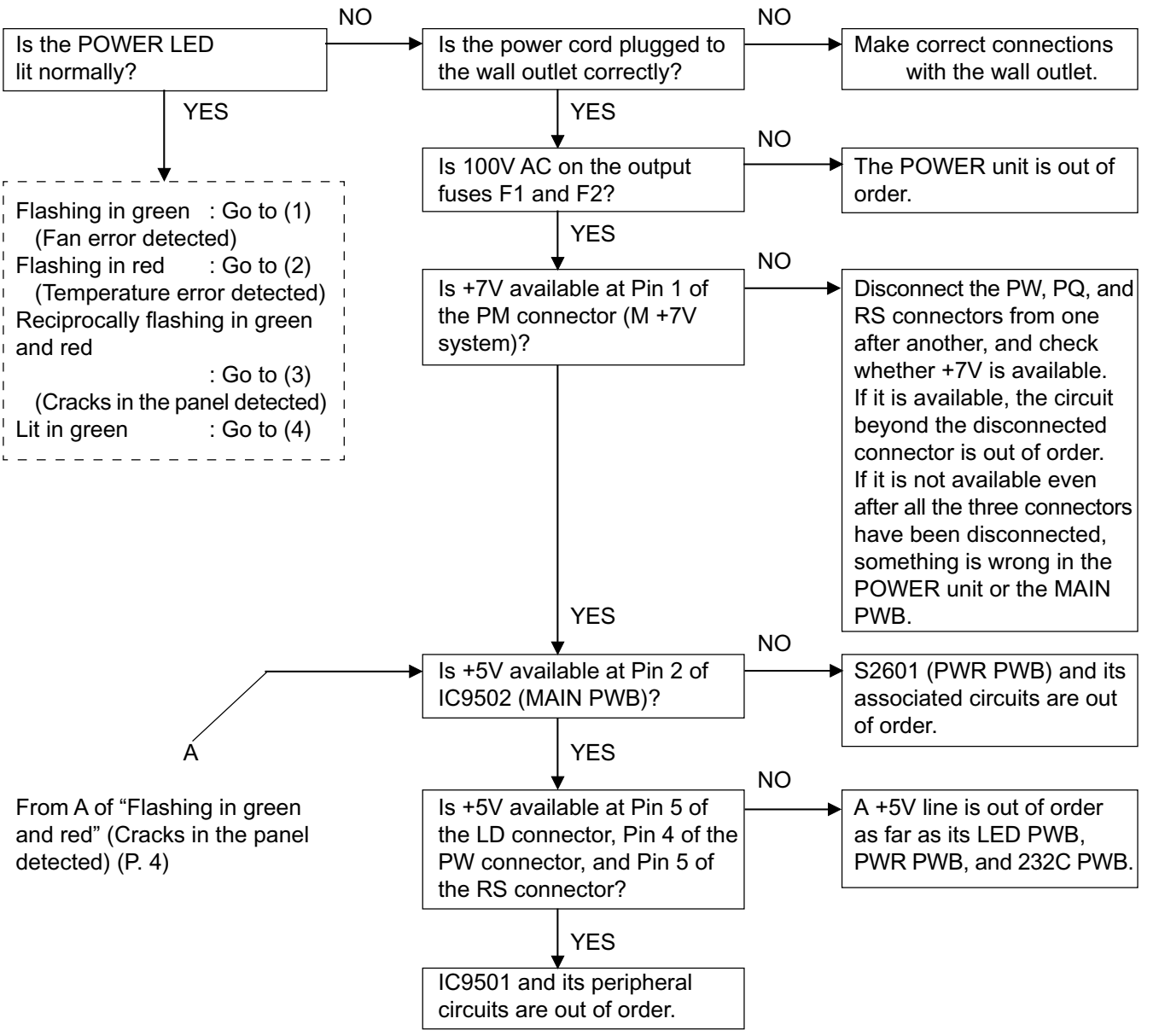
(2) In the case of a video error in the RGB 1 and 2 input circuits, go to 2-2. “No video input signals available at the RGB 1 and 2 input circuits (P. 9).
In this case, however, note the following:
① If the error remains only in the interlace motion pictures, go to 2-5. “No interlace motion pictures generated for VIDEO, DVD, HDTV, etc.” (P. 13).
② If the error remains only in the progressive motion pictures, go to 2-6. “No progressive motion pictures generated” (P. 14).
③ If the error remains only in the still pictures of PC, etc., go to 2-7. “No still pictures of PC, etc. generated” (P. 15).

(3) In the case of a video error in the DVD/HD input circuit, go to 2-3. “No video signals available at the DVD/HD input circuit (P. 10).
If this error remains only in the progressive motion pictures, go to 2-6. “No progressive motion pictures generated” (P. 14).

(4) If a video error occurs irrespective of any input selection, go to 2-4. “No video pictures available even with any input selection (P. 11).

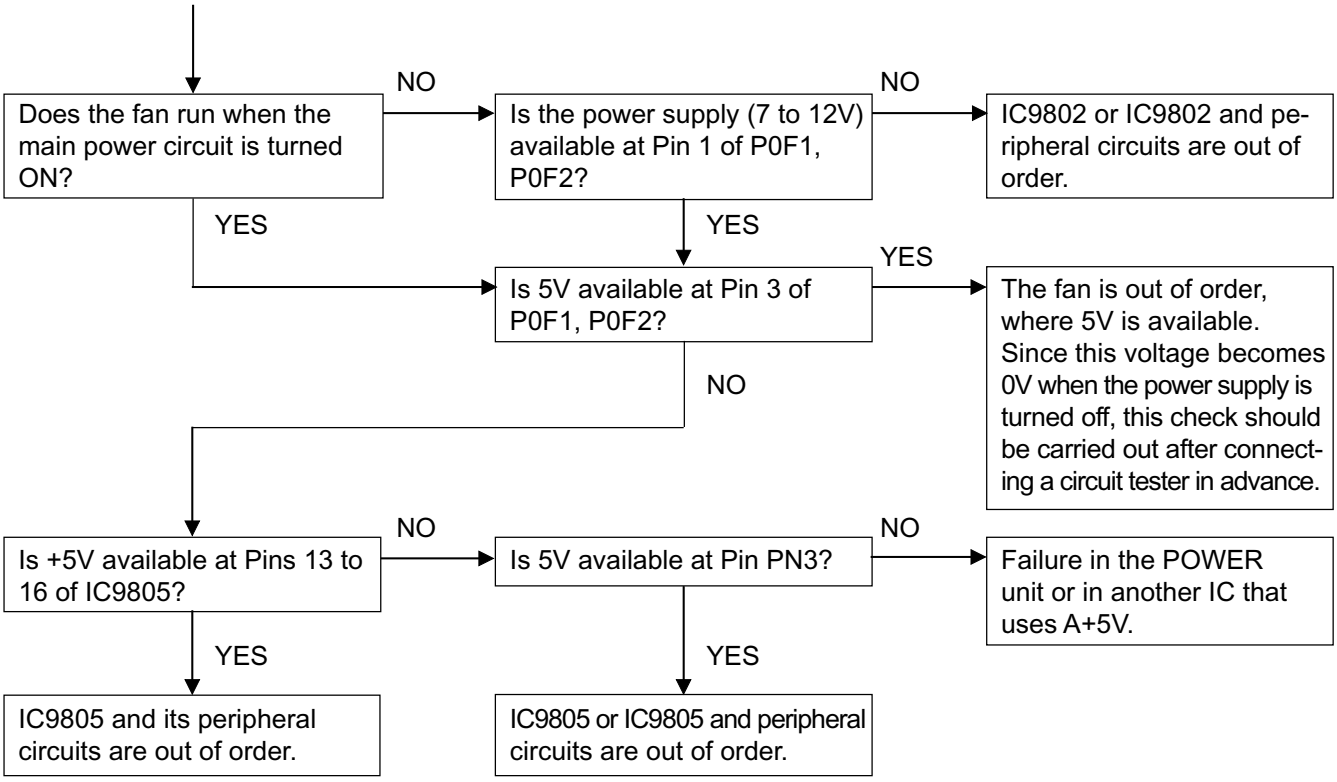
(Caution) If there is a description of □□□□ and peripheral circuit in the flow chart, the circuits used to control the □□□□ and the peripheral circuit (example: a bus from a microcomputer) are included.

1. No power available



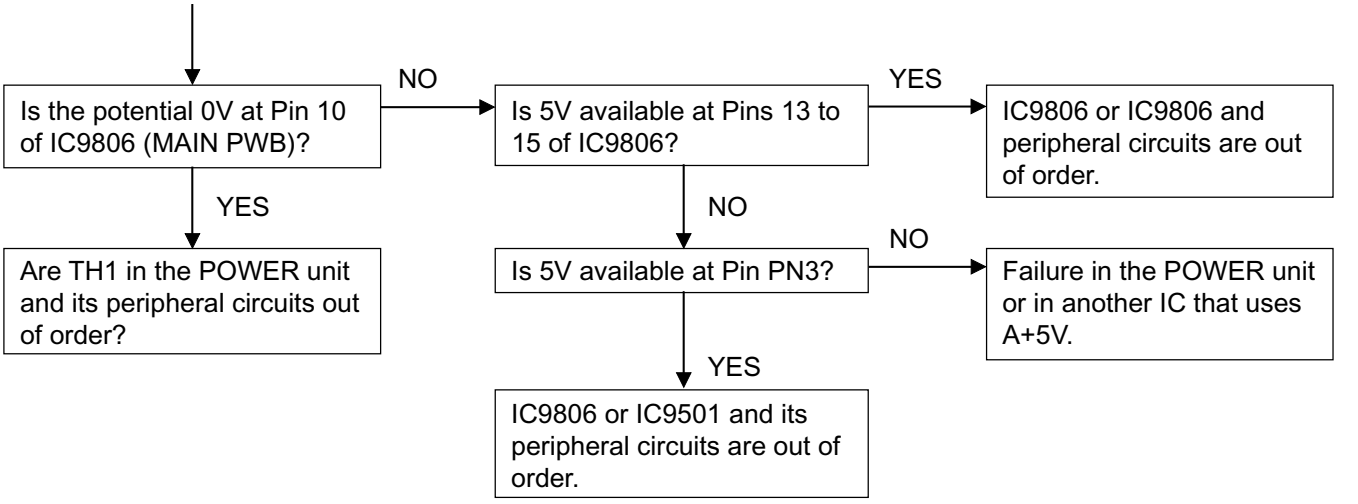
(Caution) When an LED is flashing (in the case of protector in operation), all power lines other than the M+7 system are automatically turned off. When checking these power lines other than the M+7 system, do it after connecting a circuit tester or the like to the measuring point, without fail.

(1) Flashing in green (Fan error detected)



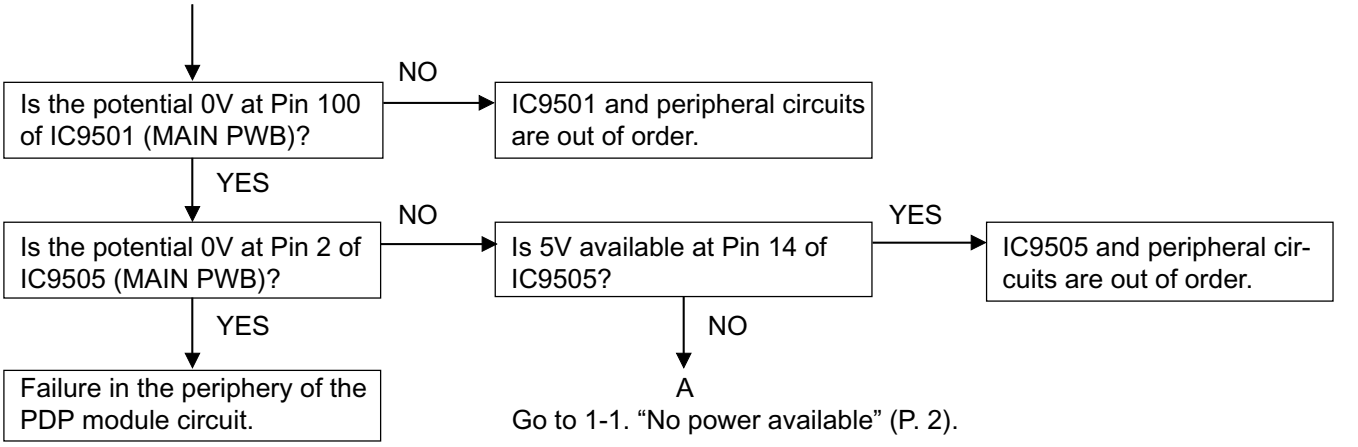
(Caution) How to reset the alarm:
• Turn the power circuit off and on at the main power supply, remote control, or the wall outlet.

(2) Flashing in red (Temperature error detected)



(Caution) How to reset the alarm:
- Turn the power circuit off and on at the main power supply, remote control, or the wall outlet.

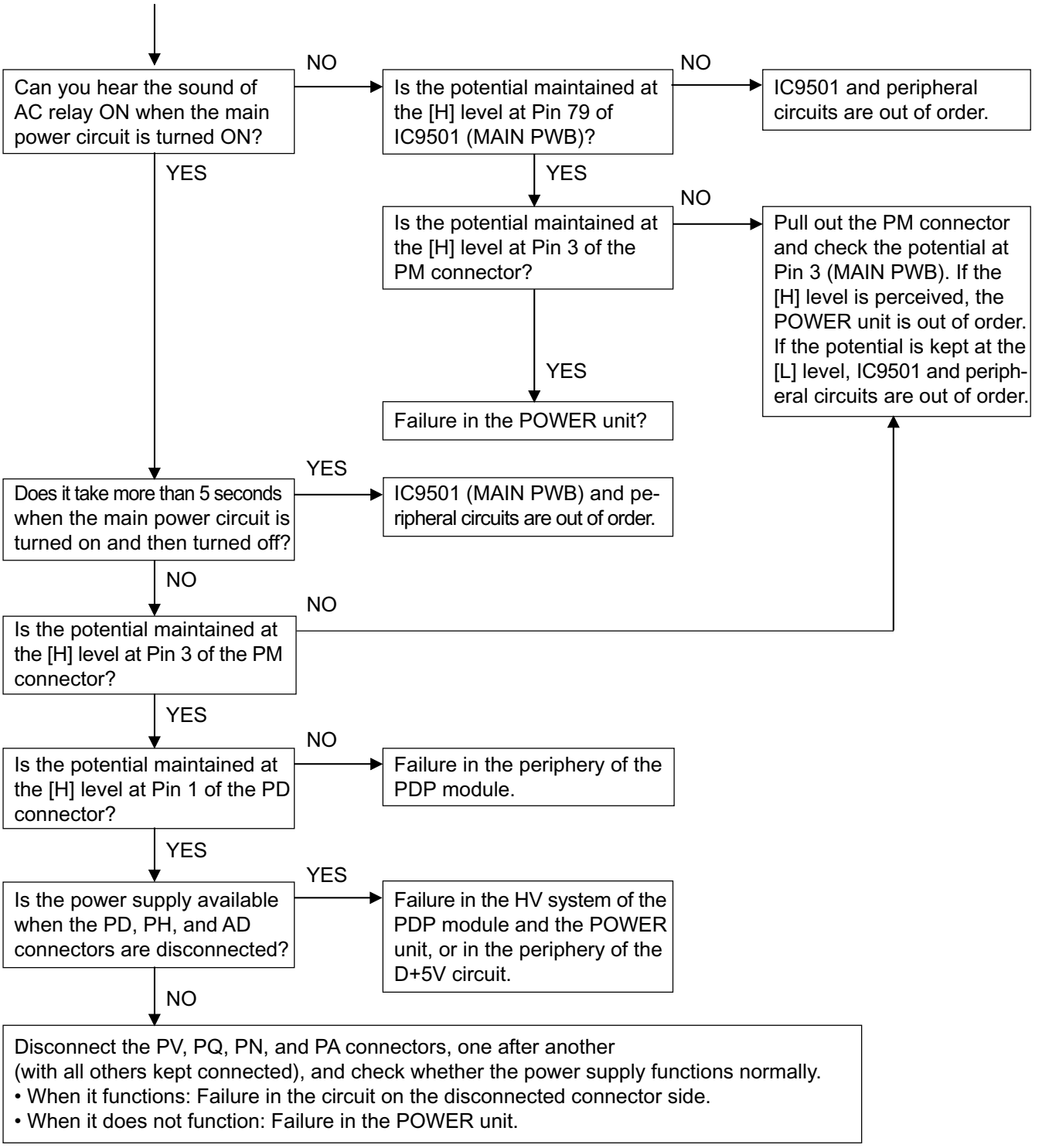
(3) Reciprocally flashing in green and red (Cracks in the panel detected)



Go to 1-1. “No power available” (P. 2).

(Caution) How to reset the alarm:
- Turn the power circuit [ON], with the input changeover key of the product kept pressed. In this state, keep on pressing the input changeover key for more than 2 seconds.

(4) Lit in green



2. Video error

2-1. No video input signals available at VIDEO 1, 2, 3 (S-VIDEO)

Are the RGB signals available at Pins 1, 3, and 5 of the P0YU connector? (See Figs. 1 to 3.)

YES → Are the horizontal sync signals available at Pins 7 and 5 of the P0YU connector and the vertical sync signals available at Pins 9 and 12? (See Figs. 4 and 5.)

YES → Failure in the MAIN PWB. Details described in Item 2-5. (P.13)

NO → Failure in the VIDEO PWB.

NO → Are the RGB signals available at TP5704 to TP5706? (See Figs. 1 to 3.)

YES → IC5709 and peripheral circuits are out of order.

NO → Is the RGB signal output generated from Pins 41 to 43 of IC5504? (Similar waveforms in Figs. 1 to 3)

YES → IC5702, IC5704, IC5706, and peripheral circuits are out of order.

NO → Is the Y signal input applied to Pin 15 of IC5504, and the C signal input to Pin 13? (See Figs. 6 and 7.)

YES → IC5504 and peripheral circuits are out of order.

NO → Ternary Y/C separation is defective in the NTSC mode.
→① No pictures available only in NTSC mode (P.7)
3-line Y/C separation defective in the PAL mode.
→② No pictures available only in PAL mode (P.8)

Conditions:
1. During the reception of VIDEO NTSC C-BAR
2. Mode VIDEO

Fig. 1 Signal G
Pin 1 of Connector P0YU : 1.4Vpp
TP5704 ; 8Vp-p

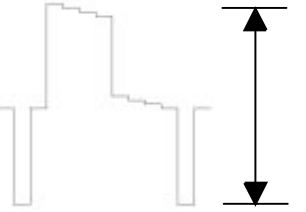


Fig. 2 Signal B
Pin 3 of Connector P0YU : 1.4Vpp
TP5705 ; 1.8Vpp

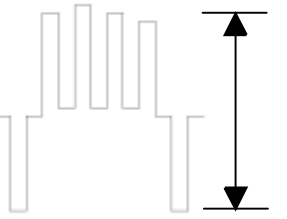


Fig. 3 Signal R
Pin 5 of Connector P0YU : 1.4Vpp
TP5706 ; 1.8Vpp

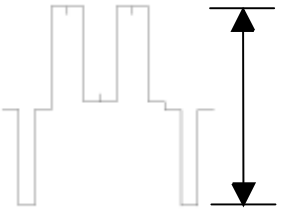


Fig. 4
Pins 7 and 10 of Connector P0YU
(horizontal sync signals)

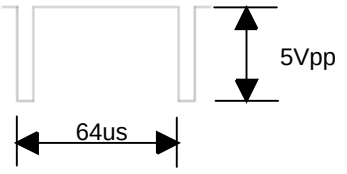


Fig. 5
Pins 9 and 12 of Connector P0YU
(vertical sync signals)

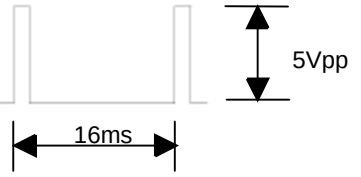


Fig. 6
Signal Y at Pin 15 of IC5504

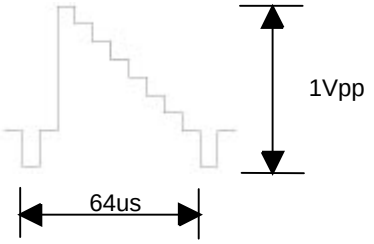
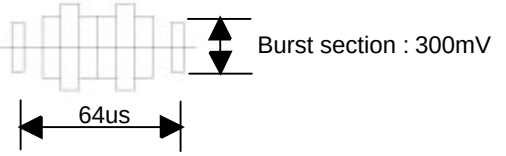


Fig. 7
Signal C at Pin 13 of IC5504



① No pictures available only in the NTSC mode (ternary Y/C separation defective)

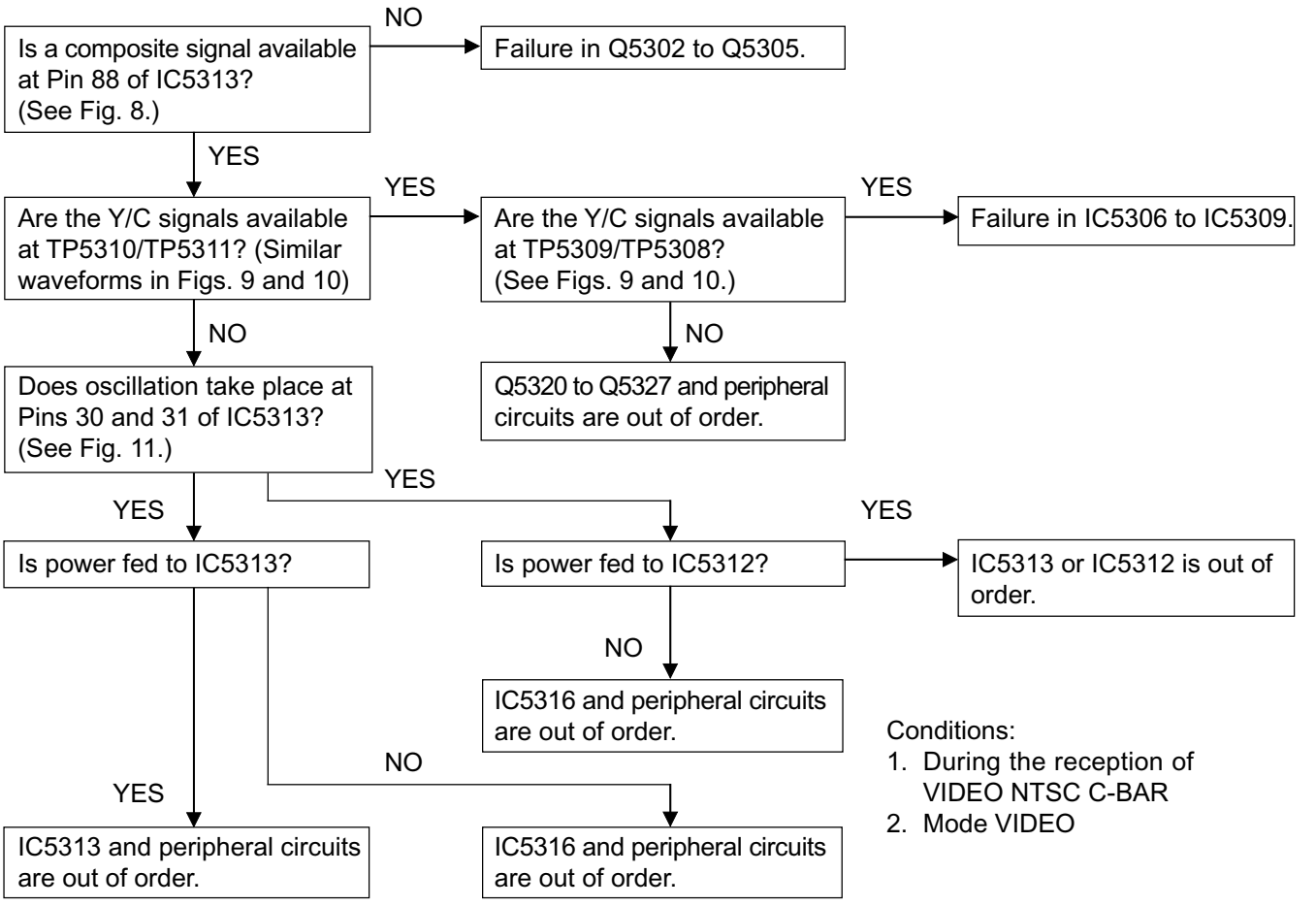


Fig. 8
Signal VIDEO at Pin 8 of IC5313

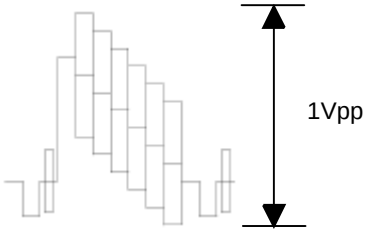


Fig. 9
Signal Y at TP5308

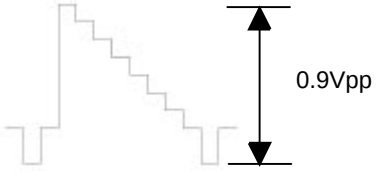
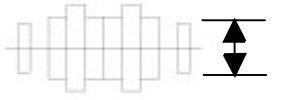
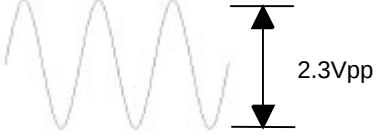


Fig. 10
Signal C at TP5309



Burst section ; 300mVpp

Fig. 11
Oscillation waveform at Pin 30 of IC5313



20MHz sine wave

② No pictures available only in PAL mode (3-line Y/C separation defective)

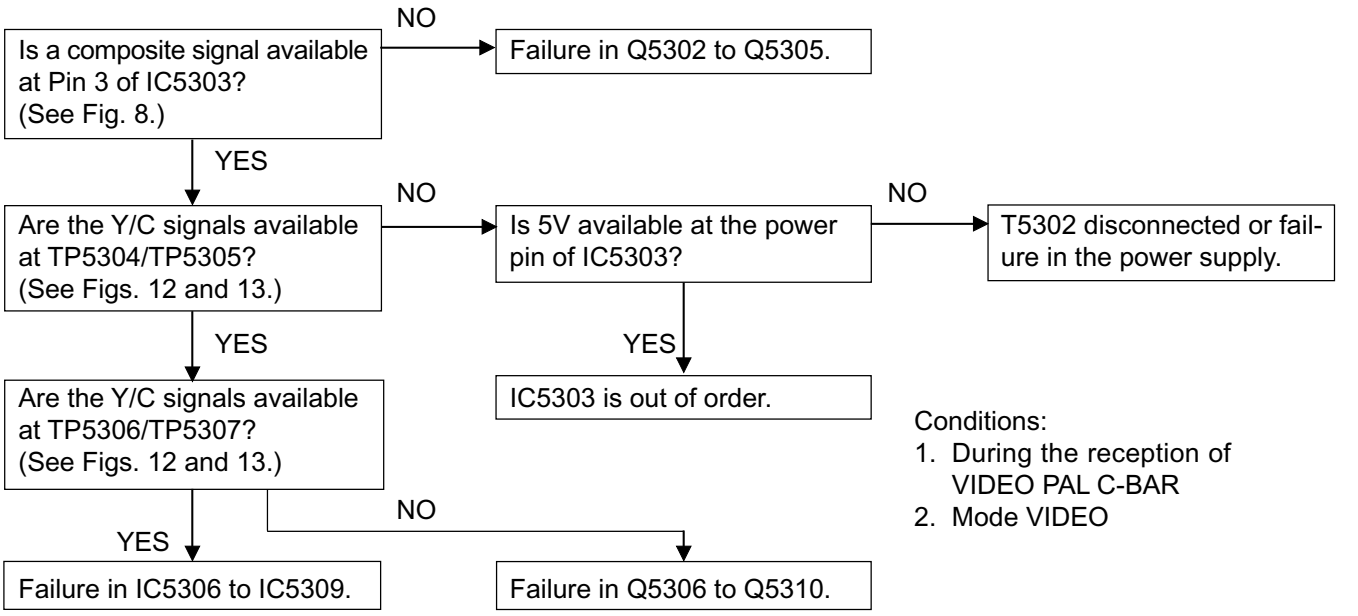


Fig. 12 Signal Y
TP5304 1.2Vpp
TP5306 1Vpp

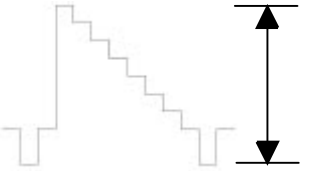
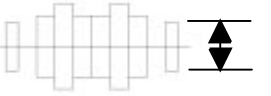


Fig. 13 Signal C
TP5305 Burst section : 300mVpp
TP5307 Burst section : 300mVpp



2-2. No video input signals available at the RGB 1 and 2 input circuits

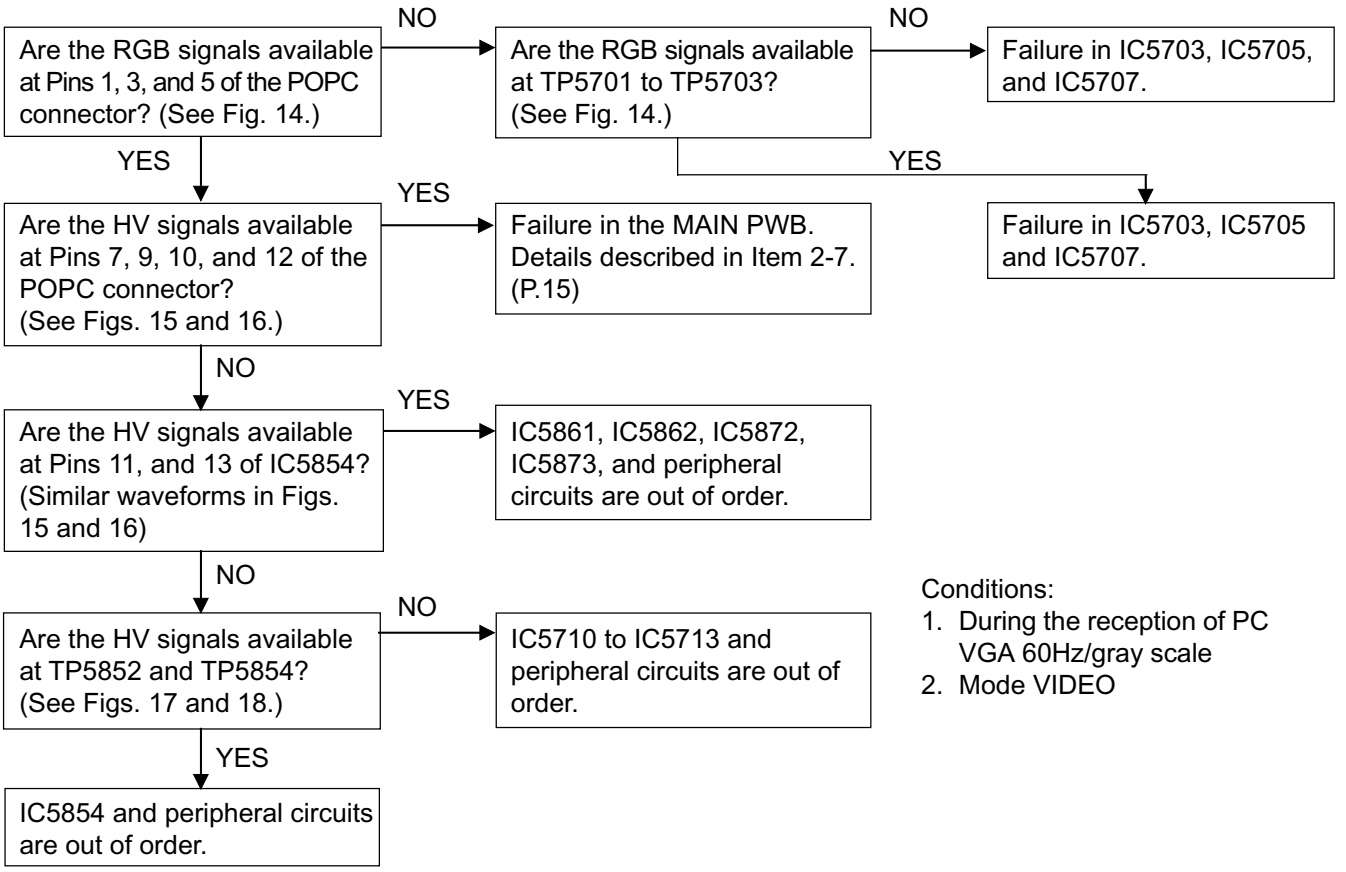


Fig. 14 Signal RGB
Pins 1, 3, and 5 of connector P0PC

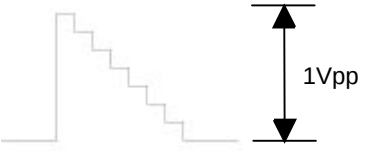


Fig. 15 Horizontal Sync Signals
Pins 13 of IC5864

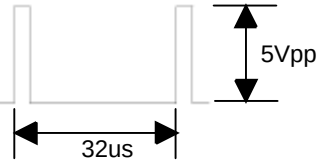


Fig. 16 Vertical Sync Signals
Pins 11 of IC5864

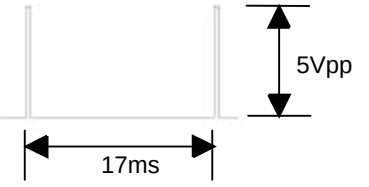


Fig. 17 Horizontal Sync Signals
TP5852

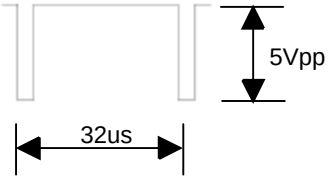
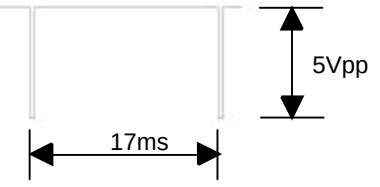
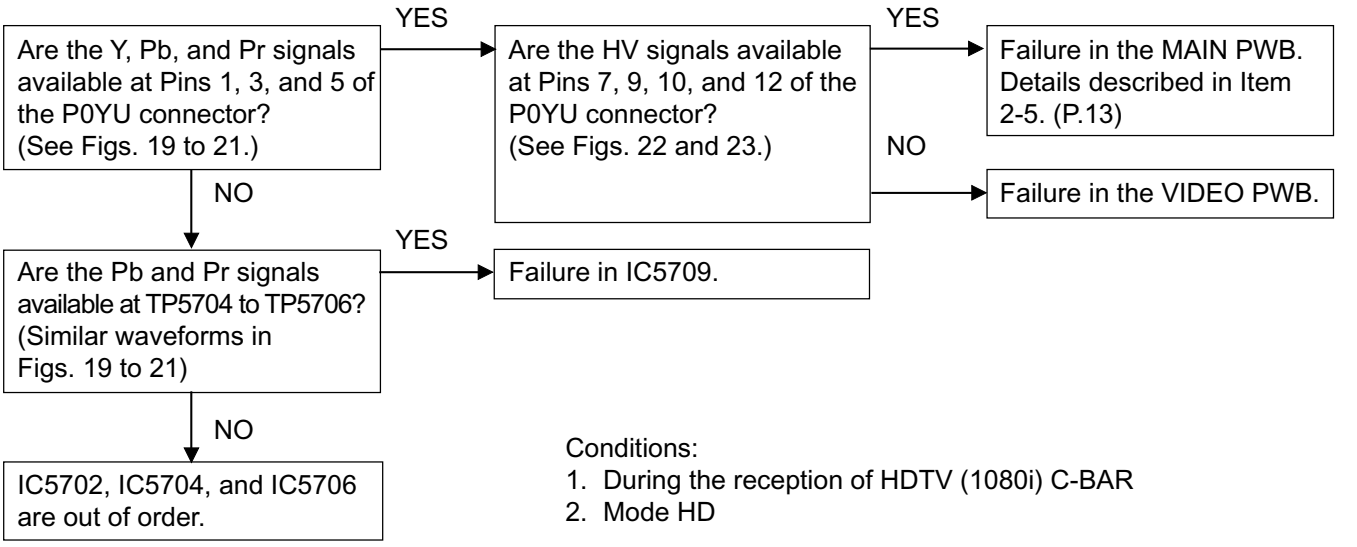


Fig. 18 Vertical Sync Signals
TP5854



2-3. No video signals available at the DVD/HD input circuit



Conditions:
1. During the reception of HDTV (1080i) C-BAR
2. Mode HD

Fig. 19 Signal Y
Pins 1 of Connector P0YU ; 1.3Vpp

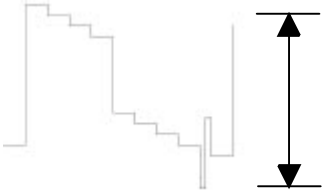


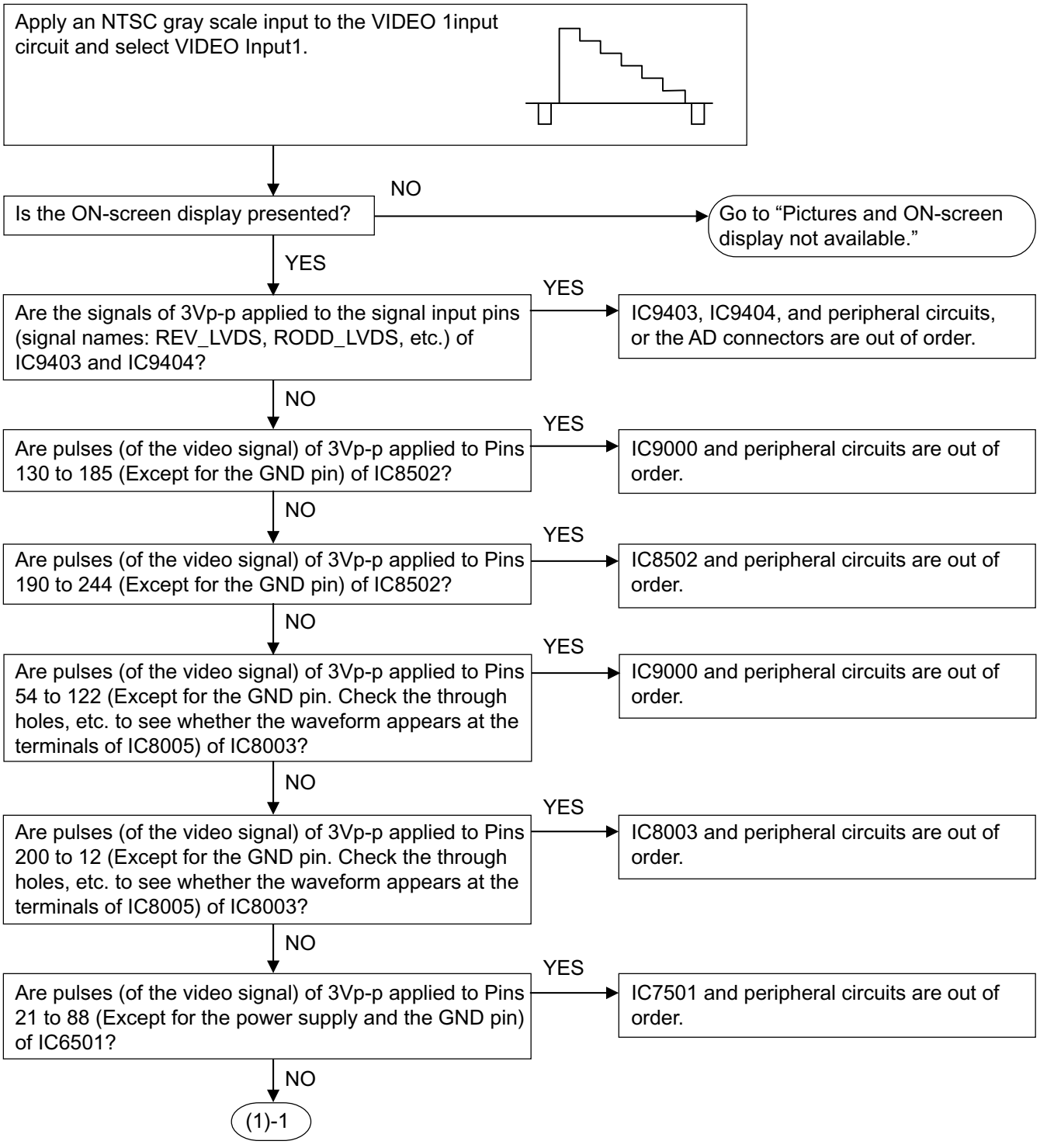
Fig. 20 Signal Pb
Pin 3 of Connector P0YU ; 1Vpp

Fig. 21 Signal Pr
Pin 5 of Connector P0YU ; 1Vpp

Fig. 22 Horizontal Sync Signals
Pins 7 and 10 of Connector P0YU ; 5Vpp

Fig. 23 Vertical Sync Signals
Pins 9 and 12 of Connector P0YU ; 5Vpp

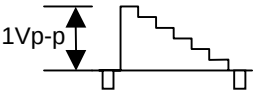
2-4. No video pictures available even with any input selection



(1)-1

NO

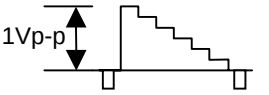
Is the video signal of 1Vp-p applied to Pins 124, 133,and 139 of IC6501?



YES → The VCC+5V system, IC9501, and peripheral circuits are out of order.

NO

Is the video signal of 1Vp-p applied to Pins 1, 2, and 3 of the YU connector?



YES → The analog circuit of the MAIN PWB is out of order.

NO

The YU connector cable or the circuits before the VIDEO PWB are out of order.

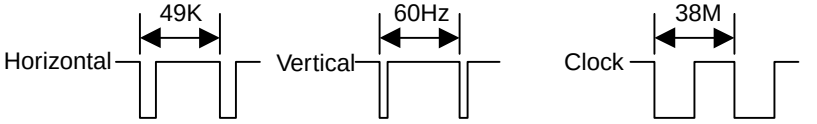
Go to “Pictures and ON-screen display not available.”

Are pulses of 3Vp-p applied to Pins 38, 39, and 40 of the AD connector?

NO → IC9402, IC9501, and peripheral circuits are out of order.

YES

Are the horizontal/vertical sync signals of 3Vp-p available at Pins 27 and 28 of IC9403, and the clock signals at Pin 31?



NO → IC9000, IC9501, and peripheral circuit are out of order.

YES

Are the signals of 3Vp-p applied to the signal input pins (signal names: REV_LVDS, RODD_LVDS, etc.) of IC9403 and IC9404?

NO → IC9000, IC9501, and peripheral circuits are out of order.

YES

Is a correct display presented when the AD, or the PD, or the PH cable is replaced?

YES → Each cable is defective.

NO

Is a correct display presented when the MAIN PWB is replaced?

YES → The MAIN PWB is out of order.

YES

Are normal outputs of 170V, 70V, and D+5V available in the POWER unit?

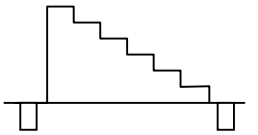
NO → Go to 1. “No power available” (P. 2).

YES

The PDP module is out of order.

2-5. No interlace motion pictures generated for VIDEO, DVD, HDTV, etc.

Apply an NTSC gray scale input to the VIDEO 1 input circuit and select VIDEO Input 1.



Are the signals of 3Vp-p applied to the signal input pins (signal names: REV_LVDS, RODD_LVDS, etc.) of IC9403 and IC9404?

YES → IC9403, IC9404, the AD connectors, and peripheral circuits are out of order.

NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 130 to185 (Except for the GND pin) of IC8502?

YES → IC9000 and peripheral circuits are out of order.

NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 190 to 244 (Except for the GND pin) of IC8502?

YES → IC8502 and peripheral circuits are out of order.

NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 54 to 122 (Except for the GND pin. Check the through holes, etc. to see whether the waveform appears at the terminals of IC8005) of IC8003?

YES → IC9000 and peripheral circuits are out of order.

NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 200 to 12 (Except for the GND pin. Check the through holes, etc. to see whether the waveform appears at the terminals of IC8005) of IC8003?

YES → IC8003 and peripheral circuits are out of order.

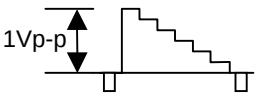
NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 21 to 88 (Except for the power supply and the GND pin) of IC6501?

YES → IC7501 and peripheral circuits are out of order.

NO

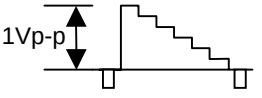
Is the video signal of 1Vp-p applied to Pins 124, 133, and 139 of IC6501?



YES → IC6501 and peripheral circuits are out of order.

NO

Is the video signal of 1Vp-p applied to Pins 1, 2, and 3 of the YU connector?

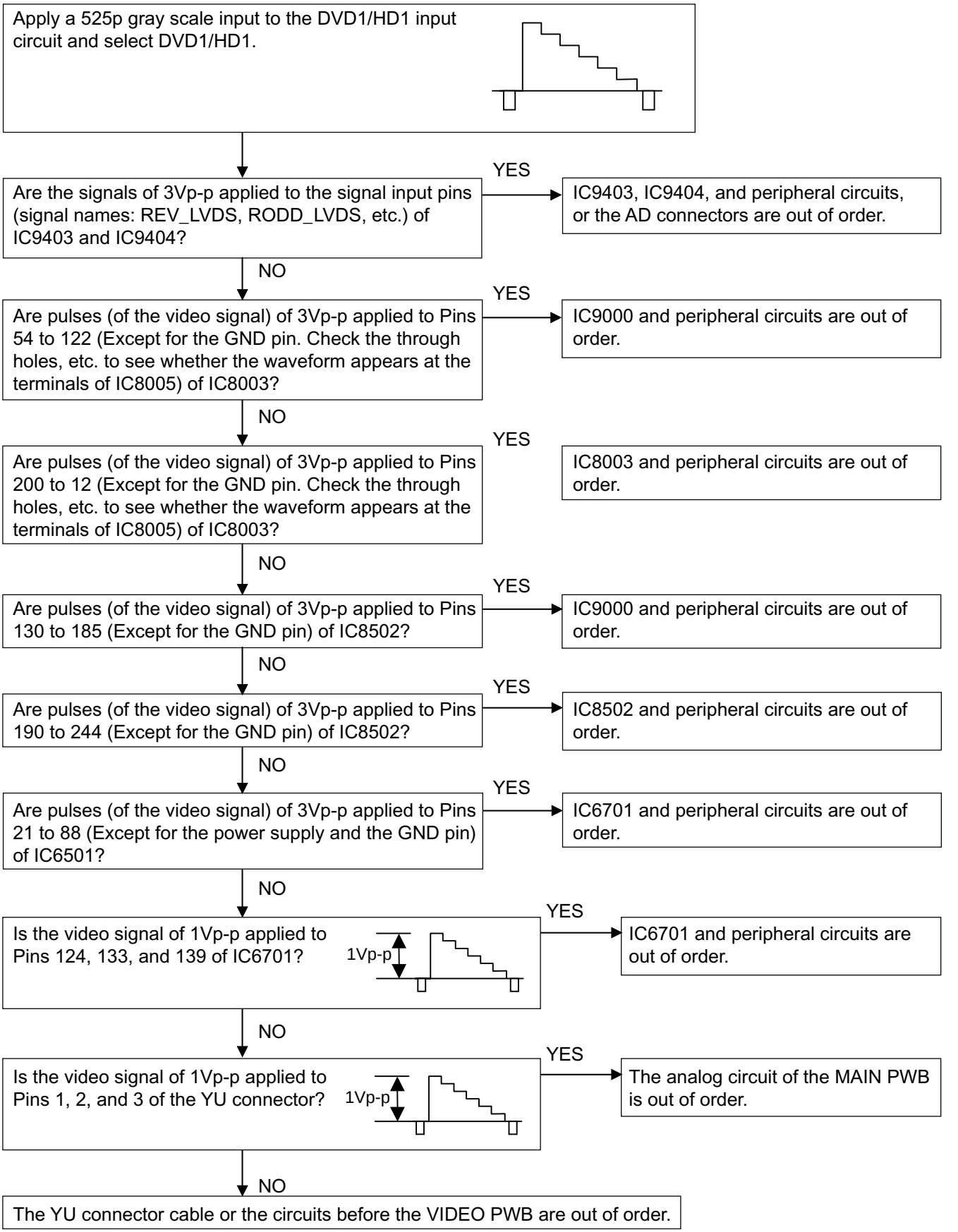


YES → The analog circuit of the MAIN PWB is out of order.

NO

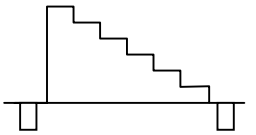
The YU connector cable or the circuits before the VIDEO PWB are out of order.

2-6. No progressive motion pictures generated



2-7. No still pictures of PC, etc. generated

Apply an XGA 60Hz gray scale input to the PC1 input circuit and select PC1.



Are the signals of 3Vp-p applied to the signal input pins (signal names: REV_LVDS, RODD_LVDS, etc.) of IC9403 and IC9404?

YES → IC9403, IC9404, and peripheral circuits, or the AD connectors are out of order.

NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 54 to 122 (Except for the GND pin. Check the through holes, etc. to see whether the waveform appears at the terminals of IC8005) of IC8003?

YES → IC9000 and peripheral circuits are out of order.

NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 200 to 12 (Except for the GND pin. Check the through holes, etc. to see whether the waveform appears at the terminals of IC8005) of IC8003?

YES → IC8003 and peripheral circuits are out of order.

NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 130 to 185 (Except for the GND pin) of IC8502?

YES → IC9000 and peripheral circuits are out of order.

NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 190 to 244 (Except for the GND pin) of IC8502?

YES → IC8502 and peripheral circuits are out of order.

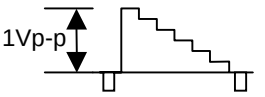
NO

Are pulses (of the video signal) of 3Vp-p applied to Pins 21 to 88 (Except for the power supply and the GND pin) of IC6701?

YES → IC6501 and peripheral circuits are out of order.

NO

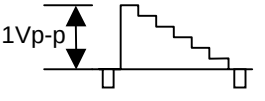
Is the video signal of 1Vp-p applied to Pins 124, 133, and 139 of IC6701?



YES → IC6701 and peripheral circuits are out of order.

NO

Is the video signal of 1Vp-p applied to Pins 1, 2, and 3 of the PC connector?



YES → The analog circuit of the MAIN PWB is out of order.

NO

The YU connector cable or the circuits before the VIDEO PWB are out of order.

METHOD OF ADJUSTMENTS

Adjustments should be carried out in accordance with the procedures described below.

1. When the PDP module is replaced, adjust the sections according to the adjusting items 1 to 4 specified below.
2. When the power unit is replaced, adjust the sections according to the adjusting items 1 to 3 specified below.
3. When the MAIN PWB or the VIDEO PWB is replaced, adjust the sections according to the adjusting item 4 specified below.
4. No adjustments are required in case of any replacement other than 1 and 2 above.

(CAUTION) When you exchange PDP module, please be sure to clear integrated time to “0” by the following “How to clear the integrated time”.

*** How to clear the integrated time**

Assume the folloing factory mode by the use of the remote control. Press “PROCEED” key six times to get the screen of “USAGE TIME”. In this state, the integrated time up to the present time is displayed.
The integrated time is cleared to “0” when the remote control keys are pressed in the order of “MUTE” → POSITION “UP” → POSITION “DOWN” → “OFF TIMER”.

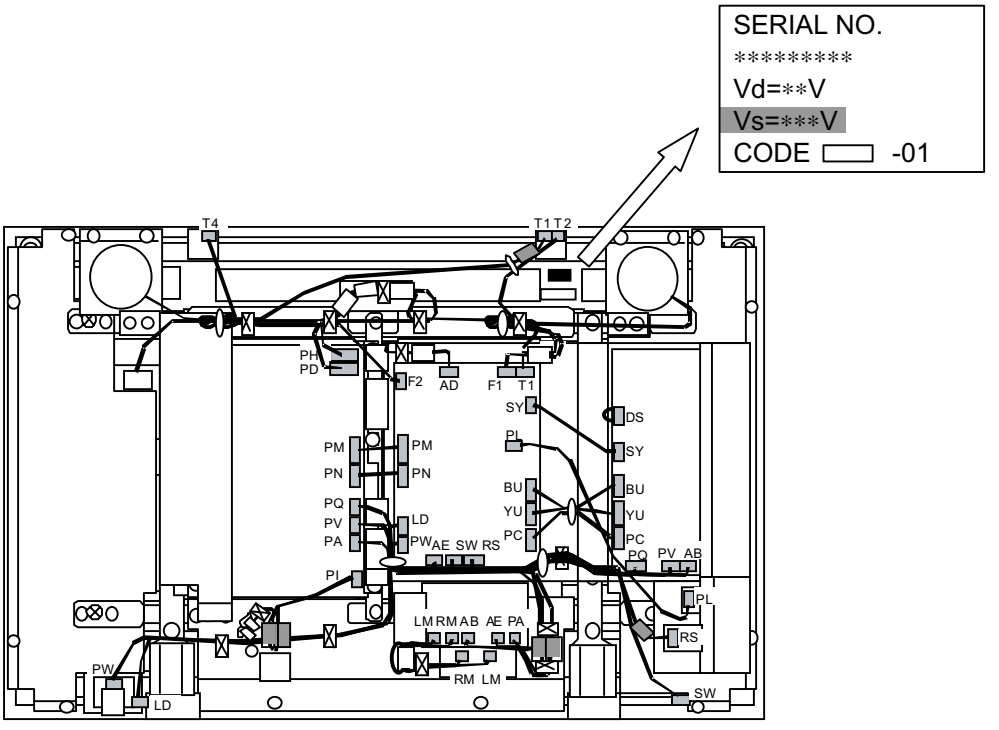
* How to enter or withdraw from the factory setting mode:
Press the keys in the sequential order of [OFF TIMER] → [EXIT] → [MUTE] → [OFF TIMER].

When a conventional remote control is used:
Press the keys in the sequential order of [OFF TIMER] → [OK] → [MUTE] → [OFF TIMER].
At that time, use the [MENU] key in place of the [PROCEED] key.

1. Adjustment of +170V

(1) Using any video signal of VIDEO input, DVD/HD input, or RGB input, and display a color bar signal. Turn on the power switch of the main unit.

(2) Turn the volume control (RV4) in the [+170V ADJ] section of the power unit, and adjust the voltage value between TP3 (+170V output) and TP4 (GND) of the power unit so that this voltage settles within the range of “specified voltage of the PDP module (Value Vs on the label shown below) ± 1V.”



2. Adjustment of +70V

(1) Using any video signal of VIDEO input, DVD/HD input, or RGB input, and display a color bar signal. Turn on the power switch of the main unit.
(2) Confirm that the voltage value between TP2 (+70V output) and TP4 (GND) of the power unit is maintained at "70 ± 1V."
Otherwise, turn the volume control (RV3) in the [D+70V ADJ] section so that the voltage value is maintained at "70 ± 1V."

3. Adjustment of +5V

(1) Use any video signal of VIDEO input, DVD/HD input, or RGB input, and display a color bar signal.
(2) Confirm that the voltage value between TP1 (+5V output) and TP4 (GND) of the power unit is maintained at "5.1 ± 0.1V."
Otherwise, turn the volume control (RV2) in the [+5V ADJ] section so that the voltage value is maintained at "5.1 ± 0.1V."

4. Screen position and phase adjustment

Adjustment of the range of horizontal display presented at the PDP module
Adjustment of the range of vertical display presented at the PDP module
Adjustment of the signal position in horizontal direction within the H POS display range
Adjustment of the signal position in vertical direction within the V POS display range

4-1. Adjustment of the VIDEO screen position

Make correct adjustments of the display range with [MHPOS] and [MVPOS].

(1) Enter an input of NTSC monoscopic signal in the VIDEO input terminal.
(2) Select the VIDEO input by the use of the relevant key of the remote control or the CTL PWB.
(3) Enter the factory shipment setting mode by using the factory shipment control command of the remote control.
(4) Press the [PROCEED] key to obtain the [POSITION] screen.
(5) Press the [WIDE] key to select the [STADIUM] mode. ([STADIUM] mode in the initial state)
(6) In case of any deviation from the display range of the PDP module, press the cursor key [^] or [v] of the remote control to select [MHPOS] or [MVPOS]. Press the cursor key [<] or [>] for adjustments.
(7) Press the cursor key [^] or [v] of the remote control to select [H POS].
(8) Press the cursor key [<] or [>] for adjustments so that the right and left are balanced.
(9) Press the cursor key [^] or [v] of the remote control to select [V POS].
(10) Press the cursor key [<] or [>] for adjustments so that the upper and lower are balanced.
(11) Confirm that [H PHA] is maintained at 0.
(12) Confirm that [H CLK] is maintained at 0.
(13) In the same manner, press the [WIDE] key to select the [ZOOM] mode, the [NORMAL] mode, or the [FULL] mode. Adjust the horizontal and vertical positions, and confirm that [H PHA] and [H CLK] are maintained at 0, respectively.
(14) Change the input signal to the PAL monoscopic signal and repeat the steps of (4) to (14) above.
(15) Withdraw from the factory mode.

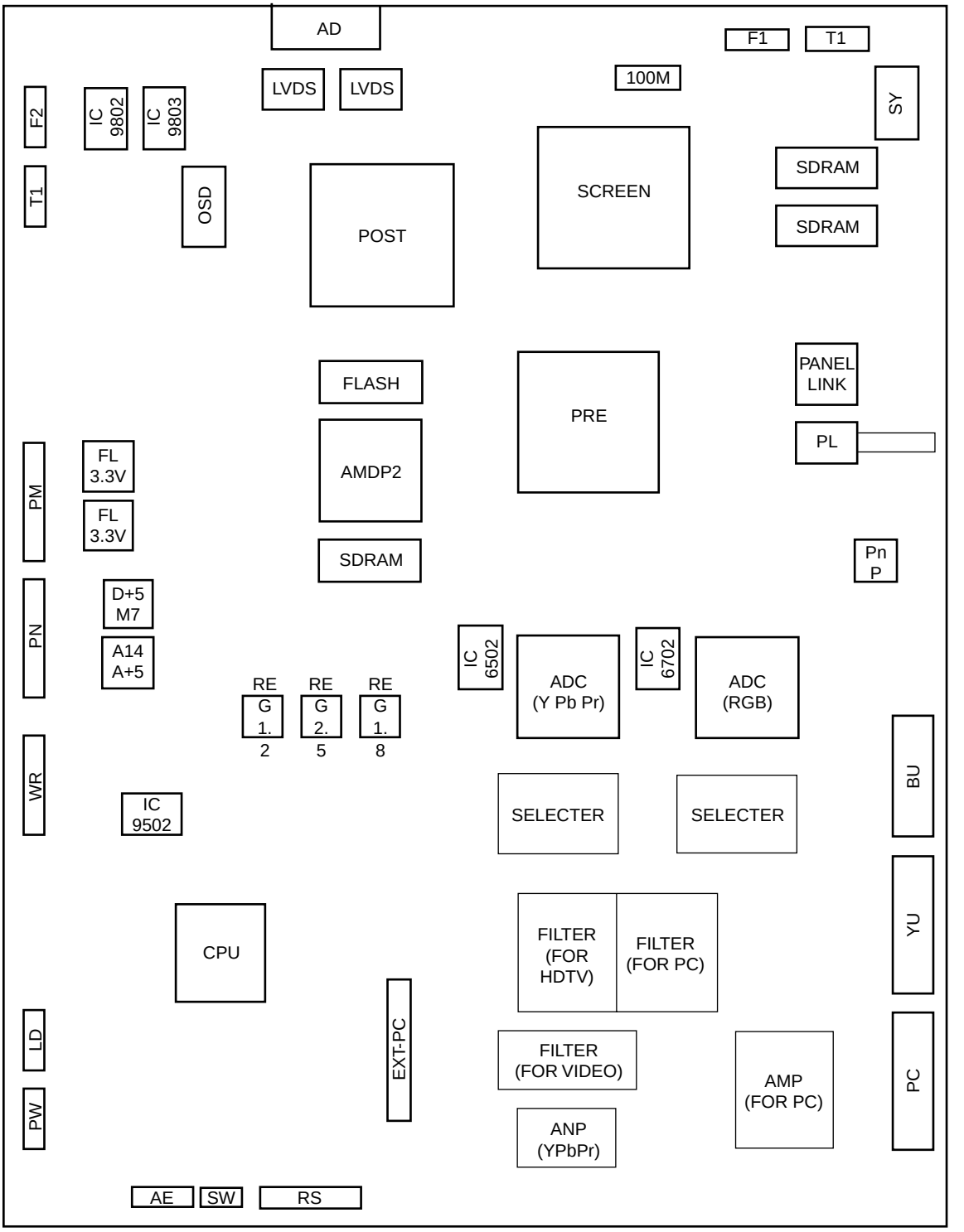
4-2. Adjustment of the DVD/HD screen position

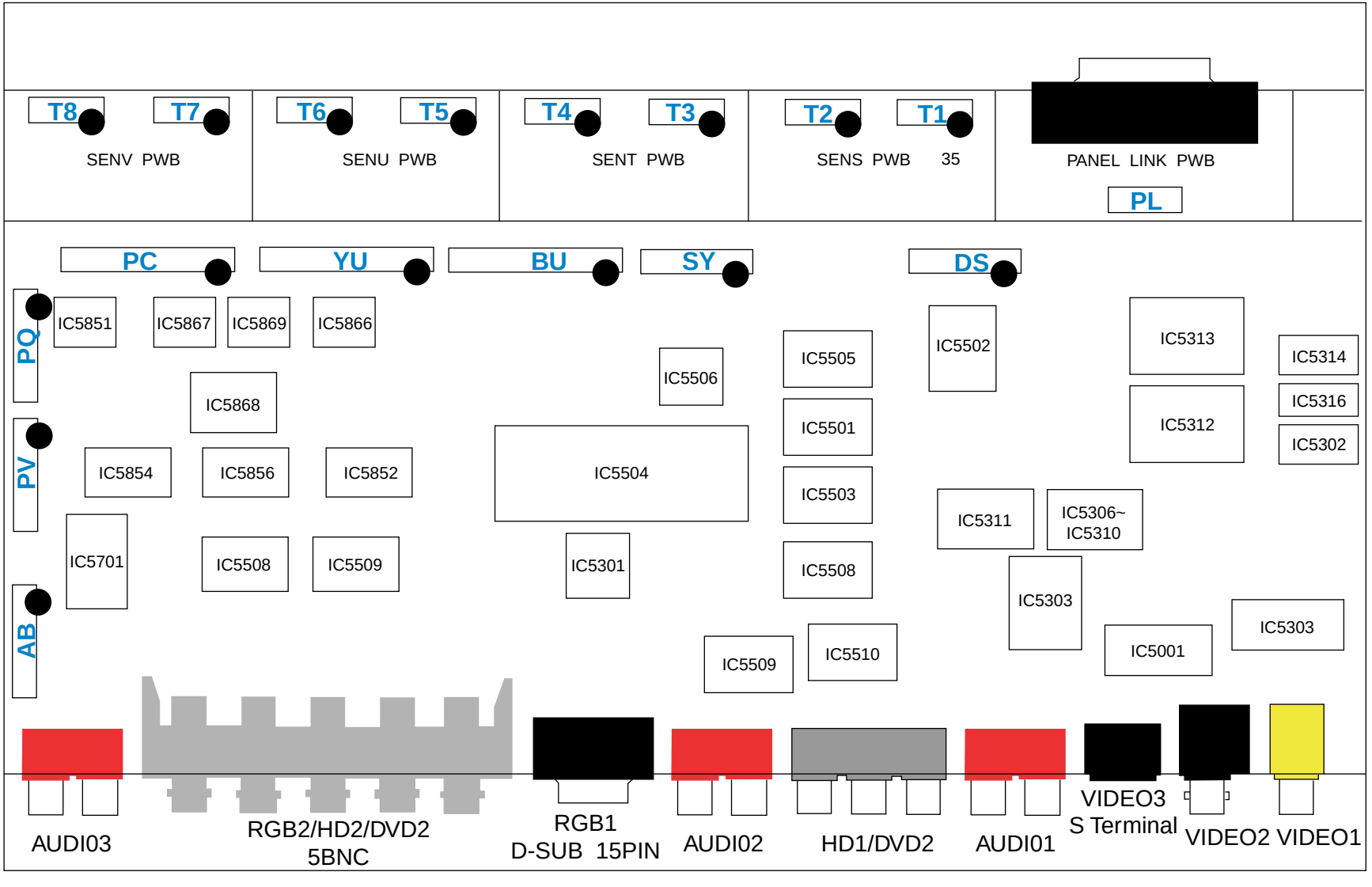
Make correct adjustments of the display range with [MHPOS] and [MVPOS].

(1) Enter an input of HDTV monoscopic signal in the DVD/HD input terminal. According to the “convenient functional setting” in the [MENU] screen, press the cursor key [^] or [v] of the remote control to confirm that [HD SELECT] has been set at [1035i].
(2) Select the HD input by the use of the relevant key of the remote control or the CTL PWB.
(3) Enter the factory shipment setting mode by using the factory shipment control command of the remote control.
(4) Press the [PROCEED] key to obtain the [POSITION] screen.
(5) In case of any deviation from the display range of the PDP module, press the cursor key [^] or [v] of the remote control to select [MHPOS] or [MVPOS]. Press the cursor key [<] or [>] for adjustments.
(6) Press the cursor key [^] or [v] of the remote control to select [H POS].
(7) Press the cursor key [<] or [>] for adjustments so that the right and left are balanced.
(8) press the cursor key [^] or [v] of the remote control to select [V POS].
(9) Press the cursor key [<] or [>] for adjustments so that the upper and lower are balanced.
(10) Confirm that [H PHA] is maintained at 0.
(11) Confirm that [H CLK] is maintained at 0.
(12) Change the input video signal to the NTSC component signal and repeat the steps of 1-1 (3) to (11) above.
(13) Change the input video signal to the DTV 1080i signal and repeat the steps of 1-1 (3) to (11) above.
(14) Change the input video signal to the DTV 1080i signal. Press the cursor key [<] or [>] of the remote control to select [1080B] for [HDS] of the screen. Repeat the steps of 1-1 (3) to (11) above. Return [HDS] to [1080i].
(15) Change the input video signal to the DTV 720P signal and repeat the steps of 1-1 (3) to (11) above.
(16) Change the input video signal to the DTV 480P signal and repeat the steps of 1-1 (3) to (11) above.
(17) Withdraw from the factory shipment setting mode.

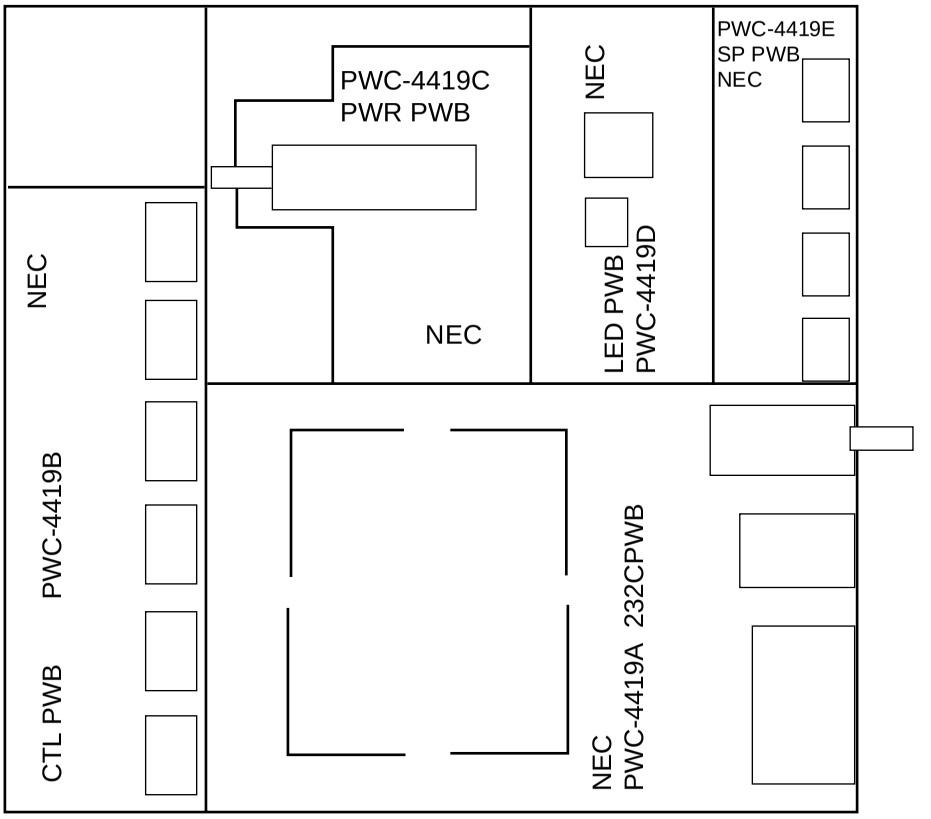
<PWB Layout>

1. MAIN PWB (PPCB-5502)

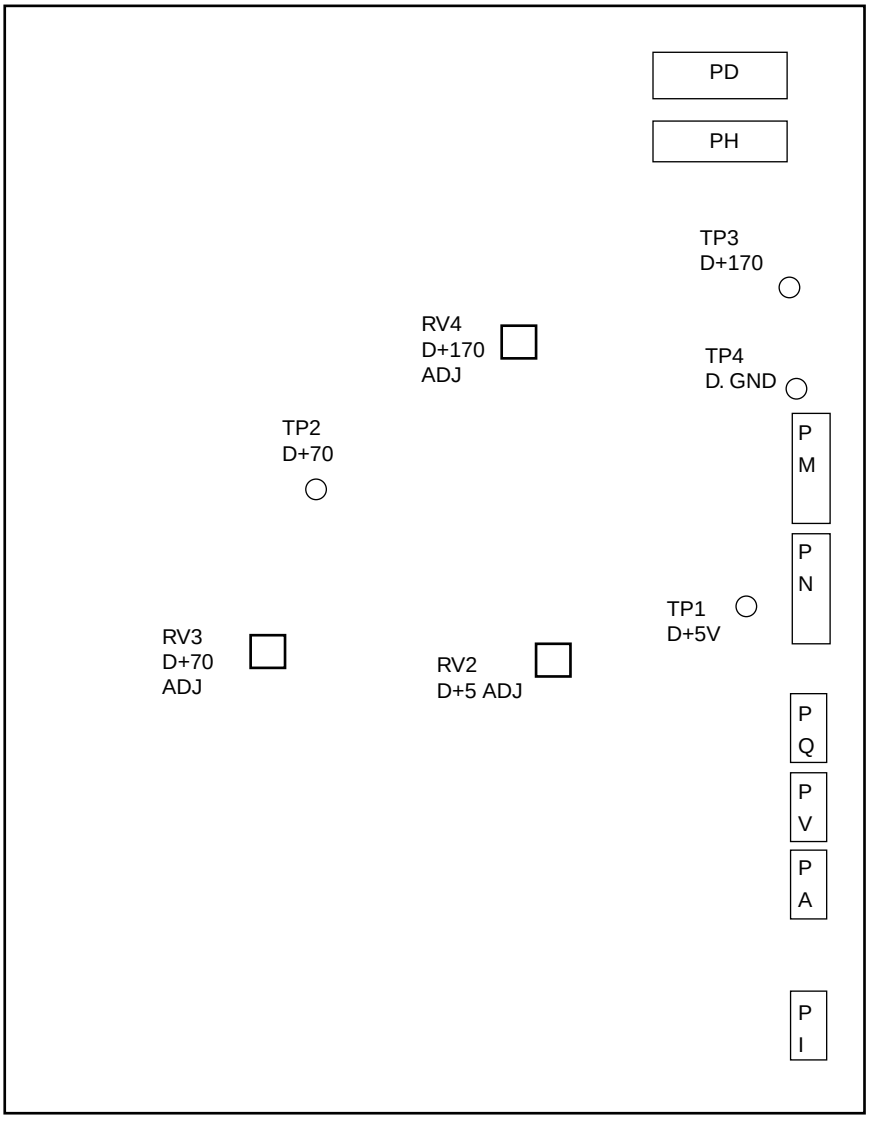



T8
T7
T6
T5
T4
T3
T2
T1
SENV PWB
SENU PWB
SENT PWB
SENS PWB
35
PANEL LINK PWB
PL
PC
YU
BU
SY
DS
PQ
PV
AB
IC5851
IC5867
IC5869
IC5866
IC5868
IC5854
IC5856
IC5852
IC5701
IC5508
IC5509
IC5504
IC5301
IC5506
IC5505
IC5501
IC5503
IC5508
IC5509
IC5510
IC5502
IC5311
IC5306~
IC5310
IC5303
IC5313
IC5312
IC5314
IC5316
IC5302
IC5303
IC5001
AUDI03
RGB2/HD2/DVD2
5BNC
RGB1
D-SUB 15PIN
AUDI02
HD1/DVD2
AUDI01
VIDEO3
S Terminal
VIDEO2
VIDEO1

3. SUB PWB (PWC-4419)



4. POWER unit layout



< Signal Generator >

① Digital RGB and component signal generator
- Equivalent to the Video Generator LT1615 (made by LEADER)
- Equivalent to the Panel Adapter LT9217 (made by LEADER)
- Equivalent to the Video Encoder LT1606 (made by LEADER)

② NTSC signal generator
- Equivalent to the NTSC Pattern Generator LCG-403YC (made by LEADER)

③ PAL signal generator
- Equivalent to the Color Bar Pattern Generator PM5518 (made by PHILIPS)

CIRCUIT DESCRIPTION

CIRCUIT DESCRIPTION

(Note) In regard to the contents of the text, please refer also to the relevant circuit diagrams.

■ Power unit block [Including the power-related μ-COM (microcomputer) operation]

- When a commercial power input is fed from an AC inlet, the power unit begins to generate an output of M+7V for the μ-COM system. M+7V is supplied to IC9502 from Pin ① of the PM connector. When the main POWER SW (S2601) is turned ON, M+5V is supplied to the μ-COM (IC9501). With the supply of M+5V, the μ-COM supplies a “POWER” signal to the power unit to actuate it.

- When the [H] input of the “POWER” signal is fed from Pin ③ of the PM connector, RL1 is turned ON to generate power outputs for the signal system (D+5V, D+3.3, A+14V, A+5V, S+13V, S-13V). These power outputs are fed to the respective signaling circuits. After each signaling power supply has been fed (for 200msec or more), the power outputs (D+170V, D+70V) are fed to the HV system, and extended further to the PDP module.

- When the temperature in the power unit attains about 100°C, the T-ALM2 signal begins to feed an “L” signal to the MAIN PWB (μ-COM) from Pin ⑧ of the PN connector. The μ-COM turns the “POWER” signal at the “L” level to turn off the power supply. In this state, the LED flashes in red. (T-ALM1 is not used.)
- When an LVP signal at the “L” level from the PDP module is entered in Pin 37 (MAIN PWB) of the AD connector and in Pin ① (power unit) of the PD connector, the μ-COM turns the “POWER” signal at the “L” level and makes the LED “flash in red and green reciprocally.” The power unit turns off all the power supplies other than the M+7V system.

- The POMUTE signal is used to detect AC OFF first of all and supplies an “L” output to Pin ④ of the PM connector. This signal is fed to Pin 93 of the μ-COM and Pin ④ of the AE connector (AUDIO unit). This circuit is used to perceive the occurrence of commercial power OFF due to a service interruption or a certain cause (prevention of misoperation). It is also used for MUTE.

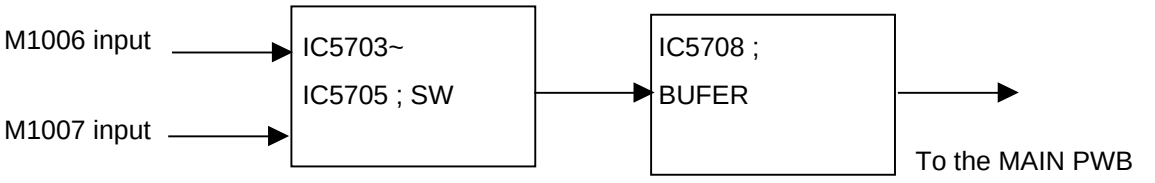
■ VIDEO PWB Block

1. AUDIO block

The AUDIO signal input entered from M1008 to M1010 is controlled and selected by I2C bus control of IC5001 (MM1311BD: SW).
The selected AUDIO signal is output from the AB connector to the AUDIO AMP module via IC5002 (BA4558: buffer).

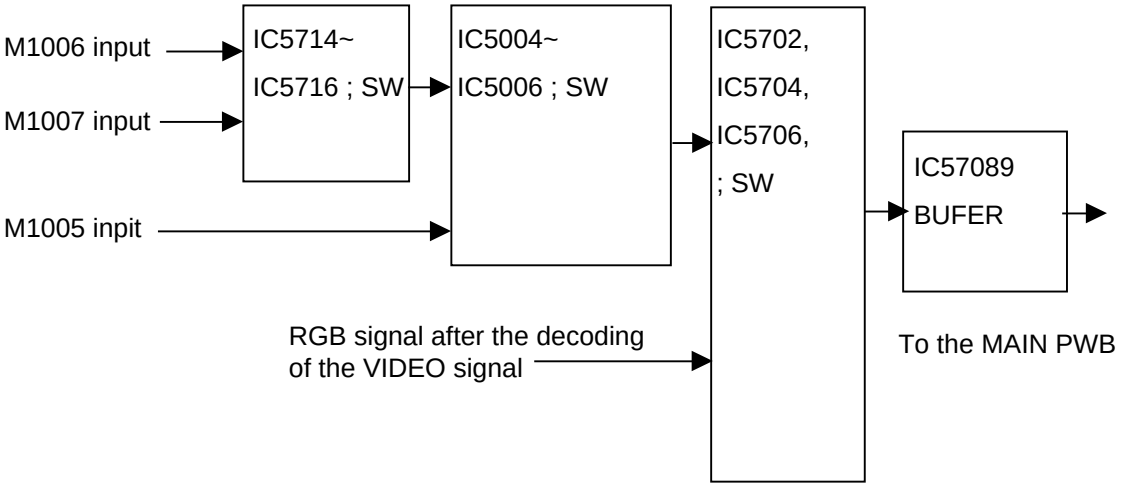
2. PC block

The video signals (RGB signals) from M1006 and M1007 are selected at IC5703, IC5705, and IC5707, and then output to the MAIN PWB via IC5708 (AD8023: buffer) and the PC connector.



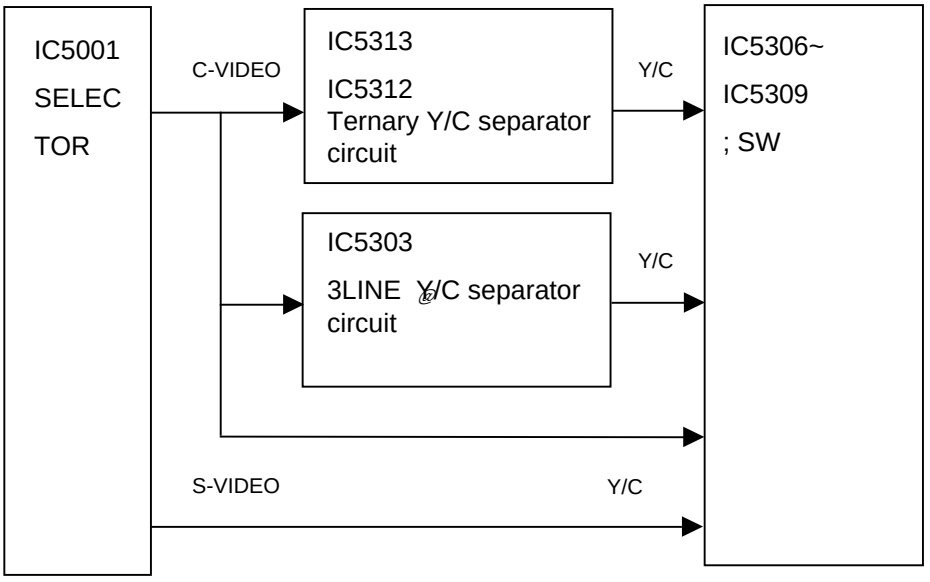
3. HD block

The video signals (Y, Pb, Pr signals) from M1006 and M1007 are selected at IC5714 to IC5716. The selected signals are changed over with the signals from M1005 at IC5004 to 5006.
The selected video signals (Y, Pb, Pr signals) are further changed over with the signals on the VIDEO input side at IC5702, 5704, and 5706. The resultant outputs are sent to the MAIN PWB via IC5709 (AD8023; buffer) and the YU connector.



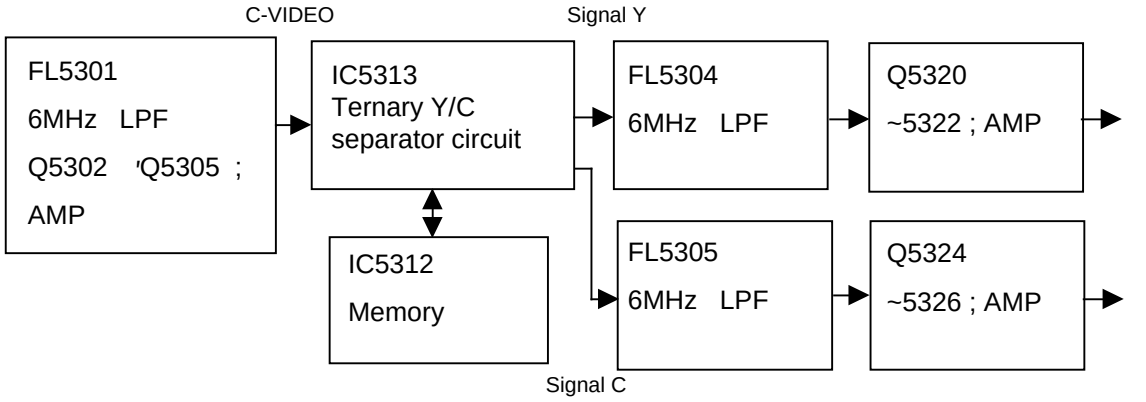
4. VIDEO block

The external VIDEO signal input is entered from M1001 to M1003, and selected at IC5001 (MM1311BD: SW). The composite signals of the IC5001 output are applied to the ternary Y/C separator circuit and the 3-line Y/C separator circuit. The Y/C signal input separated at each Y/C separator circuit is entered in IC5306 to 5309. At the same time, the composite signals are also entered in IC5306 to 5309 directly.
The Y/C signal output of IC5001 is directly entered in IC5306 to 5309.
When the input signal is of 3.58 NTSC, IC5306 to 5309 operate so that only the output of the ternary Y/C separator circuit is turned on.
If the input signal is of PAL/PAL_M,/PAL_N, IC5306 to 5309 operate so that only the output of the 3-line Y/C separator circuit is turned on.
When the input signal is of SECAM, IC5306 to 5309 operate so that the VIDEO composite signal is immediately turned on.
When the VIDEO mode is for VIDEO3 (S input), there is no dependence on the color system and the circuits operate so that the Y/C signal output of IC5001 is always turned on.



(1) Ternary Y/C separation (For NTSC)

The VIDEO signal output of Q5018 is processed for band limitation at FL5301. It is then processed for the level and Characteristic F compensation at the AMP (Q5302 to Q5305) in the latter stage. After this compensation, the signal input is entered from Q5328 to Pin 88 of IC5313, with the potential maintained at 1.0Vp-p.
The same signal is processed for sync separation at Q5317 to 5319. This sync signal input is then applied to Pin 76 of IC5313.
In IC5313, ternary Y/C separation is effected through an interface with IC5312, and the Y signal is output from Pin 84 of IC5313, and the C signal from Pin 83.
The Y signal is processed for band limitation at FL5304, and the AMP/F characteristic compensation is carried out at Q5320 to Q5322. The resultant signal input is entered in the SW circuit of IC5307.
The C signal is processed for band limitation at FL5305, and the AMP/F characteristic compensation is carried out at Q5324 to Q5326. The resultant signal input is entered in the SW circuit of IC5309.

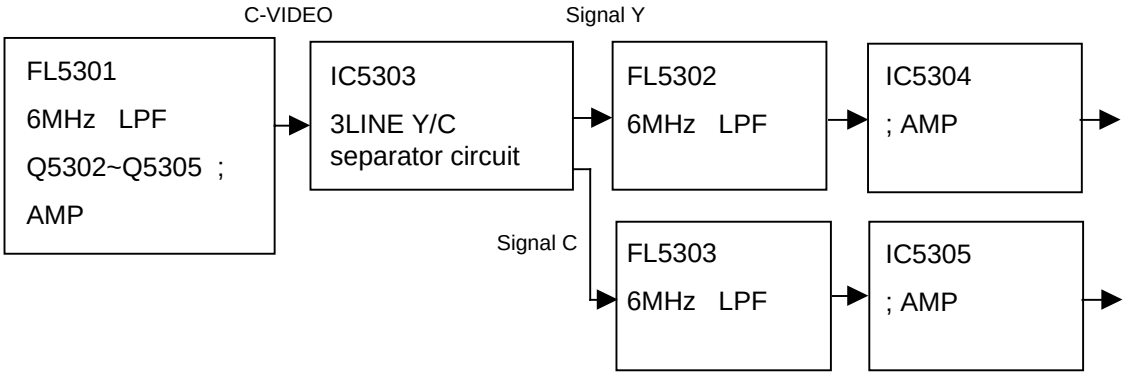


(2) 3-line Y/C separation

The VIDEO signal output of Q5018 is processed for band limitation at FL5301. It is then processed for the level and Characteristic F compensation at the AMP (Q5302 to Q5305) in the latter stage. After this compensation, the signal input is entered from Q5304 to Pin 3 of IC5303, with the potential maintained at 1.3Vp-p.

In IC5303, 3-line Y/C separation is effected, and the Y signal is output from Pin 25, and the C signal from Pin 23.

The Y and C signals are processed for band limitation at FL5302 and 5303, and they are double-amplified at IC5304 and IC5305. The resultant signal input is entered in the SW circuit of IC5307 and IC5309.

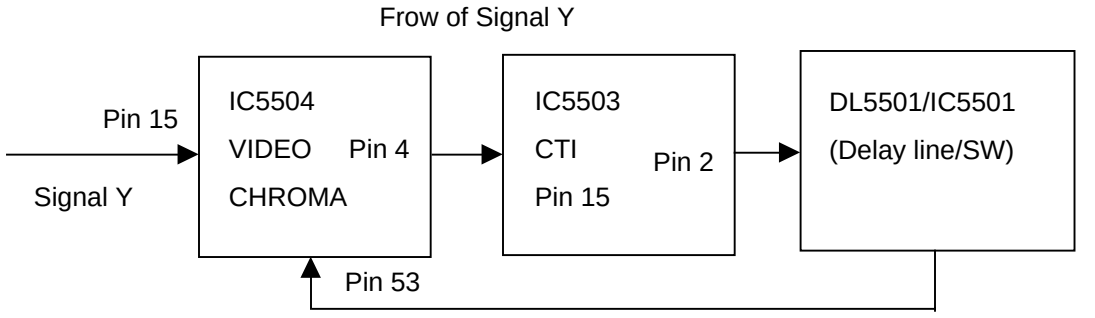


The outputs of IC5306 and IC5307 (Signal Y) are changed over with the DVD signal at IC5507 (TC7W66; SW) of the next stage. The output signal input is directly entered in Pin 17 of IC5504 as a sync signal. Compensation for Character F and peaking are effected at Q5512 to Q5515, and the input is entered in IC5504 (PAL/NTSC process).

The outputs of IC5308 and IC5309 (Signal C) are entered in IC5504 (PAL/NTSC process) and IC5510 (SECAM decoding).

(3) PAL/NTSC decoding

After passing through the built-in delay line of IC5504, the Y signal is then output from Pin 4. This signal is applied to Pin 15 of IC5503 (CTI) and double-amplified there. The resultant output is then generated from Pin 2. The output signal of Pin 2 passes through DL5501 and IC5501, and is then returned to Pin 53 of IC5504. It is further led to the internal RGB matrix through the pedestal clamp, black expander, DC reproduction, sharpness circuit, etc.



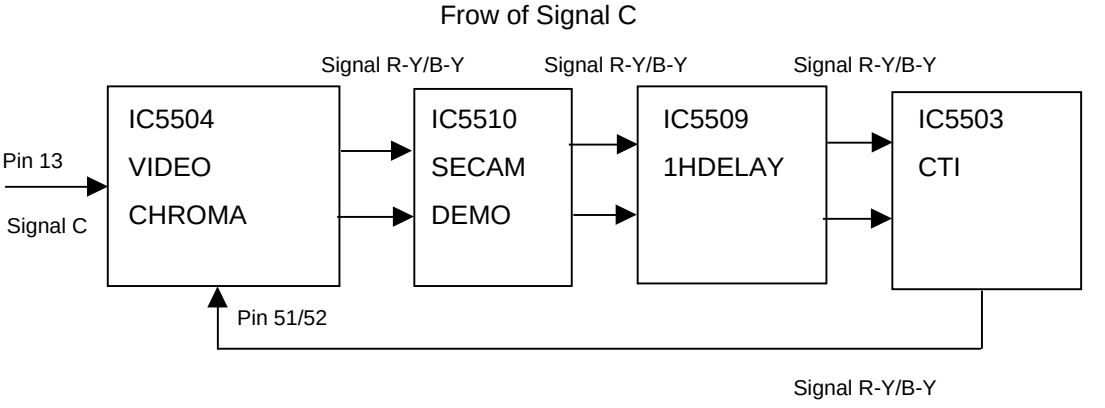
The C signal is processed for system discrimination. When it is defined for the PAL or NTSC, it is then processed through the APC circuit, ACC circuit, carrier reproduction, and the phase detection circuit to make up the R-Y/B-Y signals. The signal output is once generated from Pin 5 and Pin 6, and then entered in Pins 12/13 of IC5510 (SECAM decoding). After passing through the internal switch, the outputs are generated from Pins 10 and 11, and sequentially entered in the next stage.

[In regard to information for system discrimination, the control signal output is generated from Pins 3 and 7 of IC5504, in order to control IC5510 (SECAM decoding) and IC5508 (1H DELAY).]

In IC5508 (1H DELAY), the signal is amplified and its output is generated from Pins 29 and 30. This output is applied to Pins 7 and 8 of IC5503 (CTI).

Internal color processing is conducted in IC5504, and the resultant output is fed to the RGB matrix.

At the RGB matrix stage, this chrominance signal and the foregoing brightness signal are used to generate the analog RGB signal at the RGB matrix stage.



(4) SECAM decoding

When a color signal of SECAM is received, IC5510 (SECAM decoding) receives the control signal from Pin 3 of IC5504 (PAL/NTSC).

Inside the IC5510 (SECAM decoding), the chroma signal input of Pin 24 is processed for band limitation at the bell filter and is then amplified at the limiter circuit. Since then, FM decoding and de-emphasis are carried out. After the signal has been switched with the foregoing control signal, the chrominance output is generated from Pin 10 and Pin 11.

When this signal input is entered in Pins 26/27 of IC5508 (1H DELAY), operation of interpolation is conducted at the intervals of one hour (1H) and the output is generated from Pins 29/30. This output is entered in Pins 7 and 8 of IC5503 (CTI).

In IC5503, profile compensation for the color signals is effected. When the output is generated from Pins 11 and 12, it is then returned to Pins 51 and 52 of IC5504.

(5) 1H DELAY

Information about the color system of received signals is entered from Pin 7 of IC5504 to Pin 24 and Pin 25 of IC5508. According to this information, presence of operation in the internal circuits is examined and AMP gain changeover is carried out.

System	Voltages at Pin 24 and Pin 25 of IC5508
NTSC	0V
PAL	8.3V
SECAM	4.6V

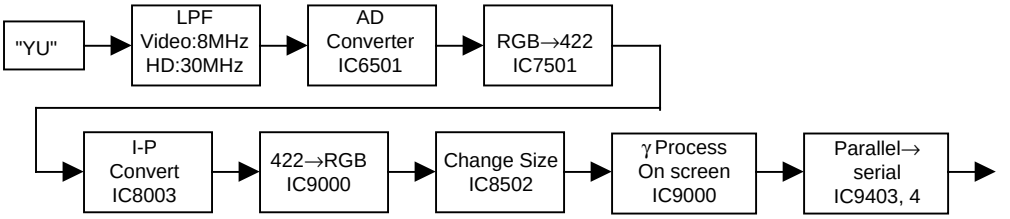
■ MAIN PWB Block

1. Video signal processor block

In the MAIN PWB, each video signal selected at the VIDEO PWB is converted into a digital signal for the purpose of various signal processing such as enlargement, contraction, and so on. The processed signal output is sent to the plasma display module.

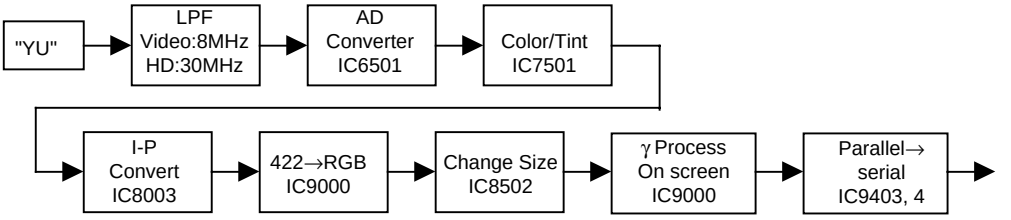
The contents of signal flow control and IC processing for analog signal inputs are different from those for digital signal inputs (RGB3). In addition, for the respective analog signal inputs, the flow of signals can differ according to the type of an input signal.

(1) Flow of video signals, video (for RGB inputs), HDTV (for RGB inputs) signals



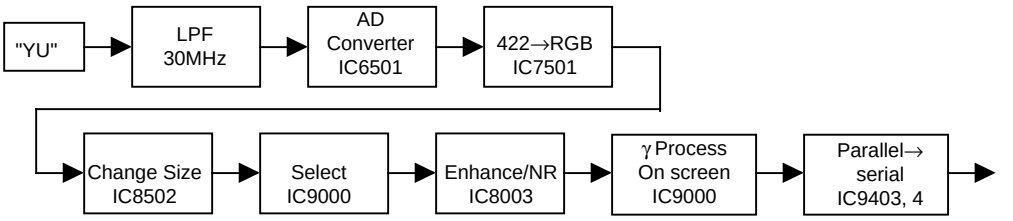
The RGB signal input entered from the YU connector is converted into a digital signal at the AD converter, IC6501. (Processing of RGB x 8 bits x 2 phases = 48 lines) IC7501 is used to convert an RGB signal into a chrominance (422) signal. In IC8003, a horizontal interlace signal of 15 kHz (34 kHz) is converted into a progressive signal of 31 kHz (67 kHz). IC8502 is in charge of screen size conversion for normal size, full size, digital zoom, etc. The processed signal inputs are entered in IC9000 again. In this IC9000, γ processing, gradation processing, and white balance processing are carried out for digital video signals. In addition, the synthesis of ON-screen signals is carried out there. In IC9003 and IC9004, 48-bit parallel signals are processed for conversion into LVDS serial signals and the output is sent to the plasma display module (“AD” connector).

(2) Flow of DVD and HDTV (chrominance input) signals



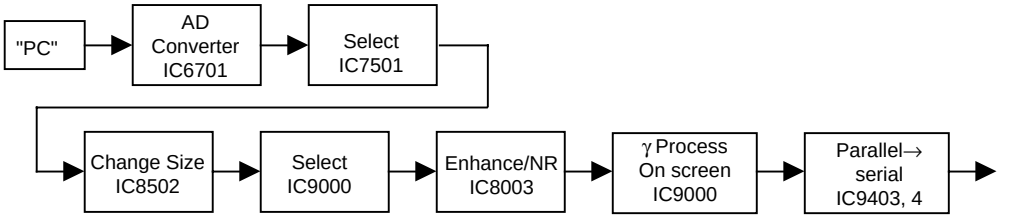
The chrominance signal input entered from the YU connector is converted into a digital signal at the AD converter, IC6501. (Processing of YUV x 8 bits x 2 phases = 48 lines) IC7501 is used for the processing of color depth and tone. In IC8003, a horizontal interlace signal of 15 kHz (33 kHz) is converted into a progressive signal of 31 kHz (67 kHz). In IC9000, the chrominance signal is converted into the RGB signal. IC8502 is in charge of screen size conversion for normal size, full size, digital zoom, etc. The processed signal inputs are entered in IC9000 again. In this IC9000, γ processing, gradation processing, and white balance processing are carried out for digital video signals. In addition, the synthesis of ON-screen signals is carried out there. In IC9003 and IC9004, 48-bit parallel signals are processed for conversion into LVDS serial signals and the output is sent to the plasma display module (“AD” connector).

(3) Flow of 480P, 720P (chrominance input), and 480P, 720P (RGB input) signals



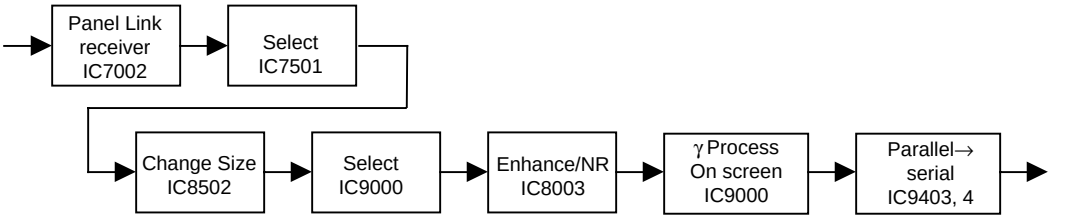
The chrominance (or RGB) signal input entered from the YU connector is converted into a digital signal at the AD converter, IC6501. (Processing of YUV or RGB x 8 bits x 2 phases = 48 lines) IC7501 is used for the processing of color depth and tone for the chrominance (422) signal and the resultant signal is converted into an RGB signal. The RGB signal is once put into chrominance conversion for the processing of color depth and tone. Since then, the signal is again converted into an RGB signal. IC8502 is in charge of screen size conversion for normal size, full size, digital zoom, etc. IC9000 sends out an output signal of IC8502 to IC8003. This IC8003 is in charge of enhancer processing and NR processing. The processed signal input is entered in IC9000 again. In this IC9000, γ processing, gradation processing, and white balance processing are carried out for digital video signals. In addition, the synthesis of ON-screen signals is also carried out there. In IC9003 and IC9004, 48-bit parallel signals are processed for conversion into LVDS serial signals and the output is sent to the plasma display module (“AD” connector).

(4) Flow of RGB1/2 (analog RGB) signals



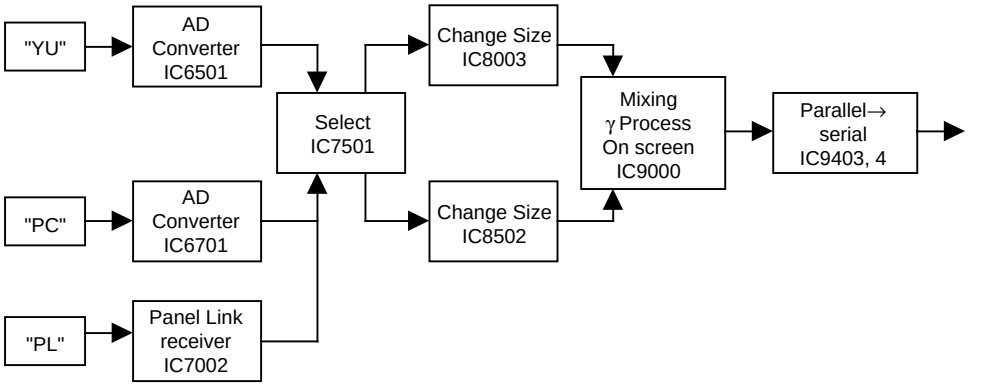
The RGB signal input entered from the PC connector is converted into a digital signal at the AD converter, IC6701. (Processing of RGB x 8 bits x 2 phases = 48 lines) IC7501 sends out an output signal of IC6701 to IC8502. IC8502 is in charge of screen size conversion for normal size, full size, digital zoom, etc. IC9000 sends out an output signal of IC8502 to IC8003. This IC8003 is in charge of enhancer processing and NR processing. The processed signal input is entered in IC9000 again. In this IC9000, γ processing, gradation processing, and white balance processing are carried out for digital video signals. In addition, the synthesis of ON-screen signals is also carried out there. In IC9003 and IC9004, 48-bit parallel signals are processed for conversion into LVDS serial signals and the output is sent to the plasma display module (“AD” connector).

(5) Flow of digital signal inputs (RGB3)



When the RGB3 input is entered, the digital RGB signal input from the PL1 connector is of the serial data and it is converted into the parallel data at the panel link receiver, IC7002. (Processing of RGB x 8 bits x 2 phases = 48 lines) IC7501 sends out an output signal of IC7002 to IC8502. This IC8502 is in charge of screen size conversion for normal size, full size, digital zoom, etc. IC9000 sends out an output signal of IC8502 to IC8003. This IC8003 is in charge of enhancer processing and NR processing. The processed signal input is entered in IC9000 again. In this IC9000, γ processing, gradation processing, and white balance processing are carried out for digital video signals. In addition, the synthesis of ON-screen signals is also carried out there. In IC9003 and IC9004, 48-bit parallel signals are processed for conversion into LVDS serial signals and the output is sent to the plasma display module (“AD” connector).

(6) Flow of dual screen display signals



The chrominance (or RGB) signal input entered from the YU connector is converted into a digital signal at the AD converter, IC6501. The RGB signal input entered from the PC connector is converted into a digital signal at the AD converter, IC6701. In IC7501, the output signal from IC6501 is adjusted to obtain adequate color depth and tone, and the output is sent to IC8003. In IC8003 and IC8502, screen size conversion is carried out for the dual screen display. IC9000 sends out an output signal of IC8502 to IC8003. This IC8003 is in charge of enhancer processing and NR processing. The processed signal input is entered in IC9000 again. In this IC9000, processing of dual screen display is conducted through the synthesis of output signals from IC8003 and IC8502. In addition, γ processing, gradation processing, and white balance processing are carried out for digital video signals. The synthesis of ON-screen signals is also carried out there. In IC9003 and IC9004, 48-bit parallel signals are processed for conversion into LVDS serial signals and the output is sent to the plasma display module (“AD” connector).

(7) Analog filter block

Before the digital conversion at the AD converter, the video signals pass through the low pass filter (LPF). Signals of motion pictures for video, HDTV, etc., pass through an LPF of 8 MHz or 30 MHz. Each switching IC (IC6005, IC6006, IC6007) is selected according to the type of signals and the output is entered in the AD converter, IC6501. The PC signal is led through a 50MHz LPF, or otherwise, it is selected for each input signal by each switching IC (IC6008, IC6009, IC6010, IC6011, IC6012, IC6013). The resultant input is entered in the AD converter, IC6701. The signal intended to select a signal is output from the I/O extension IC, IC6003. IC6003 is controlled by the I2C bus SCL2 and SDA2 from the microcomputer IC9501.

(8) AD converter (IC6501, IC6701) block

IC6501 and IC6701 are the ICs intended for the conversion of analog RGB signals into 8-bit digital signals. (However, there are 48 output lines in total, each RGB color 8 bits x 2.) In addition to the functions of AD converter, this type of IC is also provided with the various functions of analog amplifier and PLL/VCO. Each function is controlled by the I2C bus SCL6 and SDA6 from IC9501.

IC6501 accepts signal inputs of motion pictures such as video signals, DVD, HDTV, etc. IC6701 picks up RGB signal inputs of still pictures from PC, etc.

With the aid of the analog AMP incorporated in the IC, various adjustments are carried out, such as contrast adjustment, brightness adjustment, and white balance adjustment in the factory service mode.

In addition to video signals, the IC receives inputs of horizontal and vertical sync signals. Based on these sync signals, sampling of video signals is conducted by the use of the sampling clock produced in the built-in VCO. The sampling frequency differs according to each signal input entered. The clamp signal (Pin 113) is fed from IC7501.

(9) Panel link block

During the entry of RGB3 input, the digital RGB signal input from the PL1 connector is of serial data, and hence the signal is converted into parallel data at the panel link receiver, IC7002.

While the RGB3 input is not displayed, the microcomputer IC9501 turns the potential of the PD0 terminal (Pin 9) to be at the “L” level to set up a high impedance for the outputs of video signals, clock signals, sync signals, and DE (data enable). If a condition of no signal occurs during the entry of RGB3 input, the SCTD output terminal (Pin 8) is turned to be at the “L” level and this causes the PDO terminal to be at the “L” level, and a condition of high impedance is secured for the outputs. The PDO terminal gains an AND input of the SCDT output and microcomputer output in IC7003.

In IC7004, the Plug & Play data for the panel link (for RGB3 input only) are stored. The power supply and control for IC7004 are maintained from the connected equipment (personal computer, etc.) through the PL connector.

(10) Gate array (Pre G/A IC7501) block

For video signal processing, IC7501 is provided mainly with the four functions specified below. These functions are controlled by bus SIK2, SID2, and CSYUMA from the microcomputer IC9501.

① The video signal from the AD converter IC6501/IC6701 or IC7002 is selected according to the type of the input signal, and the output is sent to IC8502 and IC8003.

② The RGB signal input from IC6501 is converted into a chrominance signal of 4:4:4 or 4:2:2. The chrominance signal is converted into an RGB signal.

③ For the chrominance signal that passes through the IC inside, processing is carried out in regard to the color depth and tone.

④ The peak brightness and the mean brightness of the video signal are measured.

(11) I-P conversion and profile emphasis processing, RGB chrominance conversion (IC8003) block

In IC8003, the horizontal 15kHz interlace signals like video signals, DVD signals, etc., are converted into 31kHz progressive signals, and the 33kHz interlace signals of the HDTV system are converted into 67kHz progressive signals. (I-P conversion) In the case of other input signals, processing of profile emphasis and noise reduction is performed. In the case of dual screen processing, processing of enlargement and contraction is carried out. To perform processing of I-P conversion and that of enlargement and contraction, a RAM (IC8004) is used.

IC8004 is a control IC for IC8003. The method of image display for I-P conversion and profile emphasis processing is controlled by I2C bus (SDA1, SCL1) from the microcomputer IC9501.

X8000 is a clock signal source for IC8003 system operation (10 MHz). IC6550 operates when the potential of the system reset terminal XRST is at the [H] level. IC8001, IC8002, and IC8006 function as the power source to drive IC8003. They generate outputs of 1.4V, 1.9V, and 2.5V, respectively.

(12) Definition conversion processing block (IC8502)

Using the SDRAM (consisting of IC8503 and IC8504), IC8502 performs the conversion of the XGA signal to a level equivalent to VGA, the modification of the screen size for normal, full, etc., zoom operation, and the movement of the screen position. This IC8502 also performs color temperature regulation according to the user menu.

For memory control, a clock signal of 100MHz is produced at X8501. This signal is supplied to IC8502 and each SDRAM.

The clock signals and the horizontal and vertical sync signals to be entered in IC8502 are classified into two categories. One is the signal (input side) synchronized with the input signal and the other is the signal (output side) synchronized with the signal to be supplied to the plasma display module. Like the video signals, the clock and sync signals are fed from IC7501 and IC9000, respectively.

(13) ON-screen signal generator block

IC9401 is generating ON-screen signals. The contents of display are controlled by the SBD, SBK, and CSOSD signals sent from the microcomputer IC9501. The SBD, SBK, and CSOSD signals are put into the conversion of 5V $\rightarrow$ 3V through IC9405 and the input is entered in IC9401. The clock, horizontal sync, and vertical sync signals are sent from the IC9000 block.

(14) Gate array block (Post G/A IC9000)

For video signal processing, IC9000 is provided mainly with the four functions specified below. These functions are controlled by bus SIK2, SID2, and CSYUMA from the microcomputer IC9501 and by the signals of signal reset and video mute.

① The video signal output from IC8003 is sent to IC8502. The video signal from IC8502 is output to IC8003. This output is ON/OFF controlled by the microcomputer.

② The video signal from IC8003/IC8502 is selected. In the case of dual screen processing, synthesis processing is carried out and the output is sent to IC9403 and IC9404.

③ γ processing is conducted for video signals. The γ curve is set up by the microcomputer.

④ IC9401 (ON-screen IC) is controlled. The synthesis of ON-screen signals into video signals is carried out.

(15) Plasma display module output block

In IC9003 and IC9004, the 48-bit parallel video signal output from IC9000 is processed for conversion into the LVDS serial signal. The resultant output is sent to the plasma display module (“AD” connector).

2. Sync signal processor block

(1) AD converter block (IC6501, IC6701)

In the AD converter of IC6501 and IC6701, a sampling clock signal (clock on input side) is generated on the basis of the horizontal sync input (Pin 111) from the YU connector and the PC connector (Pin 10). Based on this clock signal at Pin 98 (Pin 99 for IC6701), a clock signal output at half the frequency is generated from Pin 101. The phase comparison output (pulses synchronized with the input horizontal sync signal) is generated from Pin 103 and fed to the latter stages. The oscillation frequency for clock signals differs according to the input signal. Phase comparison is effected when the potential at Pin 106 is at the “L” level. This phase comparison pin is controlled by the phase comparison stop signal output from IC7501.

(2) Panel link block (IC7002)

During the entry of RGB3 input, the signals of clock, horizontal and vertical sync, and video period discrimination are output.

All these signals are entered in IC7501. Under the control from IC7501, clock signals are fed to other ICs.

(3) Gate array block (Pre G/A IC7501)

IC7501 is used as a timing controller intended to generate a variety of timing pulses based on the clock and horizontal sync signals from IC6701 (AD converter) and the vertical sync signal input entered from the YU connector and the PC connector (Pin 12).

The clock signals and various pulses are fed to IC6501, IC6701, IC8003, and IC8502. According to the signal type and the input mode, the output is generated through pulse changeover for IC8003 and IC8502 in conformity to the video signal output. (Refer to 1. Video signal processor block.)

IC7501 operates with the system clock signal (CLKS_PRE signal) sent from IC9000.

(4) Module side (output side) clock generator block

The clock signal on output side is generated at X9000 (76MHz). This clock signal is supplied to each IC and the plasma display module.

(5) Gate array block (Post G/A IC9000)

IC9000 is used as a timing controller intended to generate a variety of timing pulses based on the clock and horizontal sync signals from IC7501 (Pre G/A) and the clock signal from X9000.

The clock signals and various pulses are fed to IC8003, IC8502, IC9401, IC9403, and IC9404 on input side. According to the signal type and the input mode, the output is generated through pulse changeover for IC8003 and IC8502 in conformity to the video signal output. (Refer to 1. Video signal processor block.)

3. System control block

IC9501 is used as a microcomputer (μ-COM) for system control. In this IC9501, various controls are carried out, such as input signal changeover, setting in the A/D converter block, adjustment of the timing and video chroma block for the output signals from the timing controller, selection of the hue and color depth level for the HD decoder and the method of digital signal processing, various controls of the plasma display module, diagnostic judgment for troubleshooting inside the set, and so on.

Pin 34 of the microcomputer IC9501 is used as a reset terminal. It is connected to the reset IC (IC9505). This terminal generally works at 5V.

The contents of control are described below. For the matters not described here, please refer to the relevant explanations given to each individual circuit block.

(1) Input signal discrimination

The microcomputer performs the discrimination of input signal type based on the horizontal sync and vertical sync signals (Pin 7 and Pin 9 of the YU connector and the PC connector) and the information (at Pins 1, 2, 4, and 5 of the BU connector) sent from the VIDEO PWB through the I2C bus. Based on the result of the above-mentioned discrimination, the microcomputer performs the control of various blocks. During the entry of VIDEO3 input (for an input at Terminal S), the detection of S2 (automatic discrimination of the Terminal S system) is carried out.

With the voltage at Pin 3, the screen size (screen mode) is automatically modified.

Voltage at Pin 3	Other than the right	1.4~2.4V	3.5~5.0
Result of discrimination	4:3 (general)	4:3 (letter box)	16:9 (squeeze)
Screen size	By user's selection	Zoom	Full

During the entry of RGB3 input, the presence (if any) of the input signal is identified according to the status of the SCDT terminal (Pin 100, at "H" in ordinary operation) and operation for power management is conducted.

(2) Auto-picture function

In IC7501, the screen position data are computed according to the input video signal when the auto-picture feature is turned ON for the RGB input. During the entry of RGB3 input, the screen position data are computed based on the DE signal sent from IC7002. The microcomputer picks up the screen position data from IC7501, and sets up the screen position in IC7501 and IC8502 based on the obtained data.

(3) Last memory function

The input mode, power ON/OFF status, setting values of various user controls, factory servicing values, and such data are stored in an external EEPROM (IC9504). During the entry of VIDEO input, however, data of color, tint, and UCOL are stored in IC1011 of the VIDEO PWB. In the SECAM mode, data of R-Y, B-Y, and BELL are also stored in this IC1011.

(4) Error detector block

The microcomputer is in charge of fan stoppage, plasma display module alarming, and temperature sensor detection.

① Detection of fan stop

Two fans are loaded on the set main body. If a stop signal ([H]) from either fan is entered in IC9805 and even a single fan unit stops as a result, the “L” signal is sent to the microcomputer IC9501. When either fan stops, the relevant LED blinks in green and the power supply assumes a standby condition. The function of fan stop detection is disabled when Pin 2 and Pin 3 of S9802 are short-circuited with a jumper wire or the like.

② Panel crack detection

If there is any abnormality in the plasma display module (signal system), an alarm signal is sent from Pin 37 of the “AD” connector to Pin 100 of the microcomputer. When this terminal is at the “L” level, the LEDs repeat reciprocal lighting in red and green, in order to indicate a condition of power supply in standby mode. To reset alarming, the input changeover key is kept pressed at the set main body and the mains POWER of the main body is turned “ON.” In this case, it is necessary to keep pressing the input changeover key at the main unit for more than 2 seconds.

③ Temperature error detection

When the temperature sensor of the power unit senses any abnormality or when Pin 8 of the “PN” connector is turned to be at the “L” level, the LED flashes in red and a condition of power standby is assumed.

(5) Temperature sensor block

The information about the internal temperature in the set is transmitted from the temperature sensor boards (SEND PWB, SENT PWB) to the microcomputer via the I2C bus SCL5 and SDA5 of the T1 connector. Based on this information, the microcomputer controls the output voltage of the regulator IC9802 and IC9803 via IC9805. In this fashion, fan revolutions are increased and decreased.

(6) Remote control block

This system is applicable to remote controls. An infrared remote control light receiver block RV2101 is mounted on the LED PWB. Its signal input is entered in IC9808 through the “LD” connector. The 232C PWB is provided with the wired remote control input terminals and an input from the “RA” connector is entered in IC9808. In IC9808, a signal of infrared remote control is generally selected and its input is fed to Pin 7 of the microcomputer IC9501. When a wired remote control is connected, the potential at Pin 2 of IC9808 is turned at the “L” level and the signal of wired remote control is selected so that its input is entered in the microcomputer.

(7) Control lock block

When S2001 is turned on (pressed condition) inside the 232C PWB, Pin 19 of the microcomputer IC9501 is turned “H” and all keys other than the POWER key of the set main body are disabled.

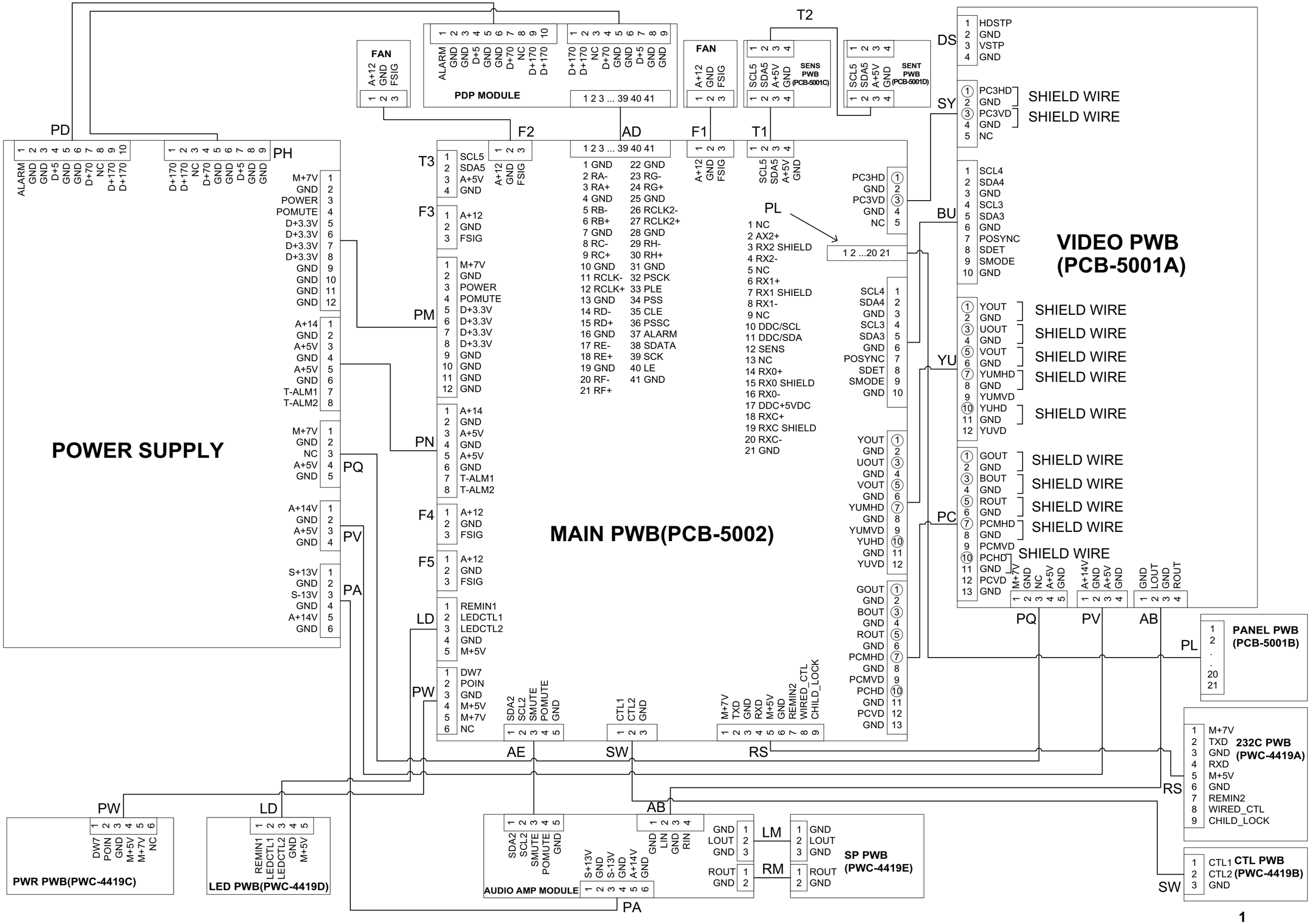
(8) PDP module control block

With the PDP module, information about the screen position and input signals is controlled by the microcomputer through the bus SDATA, SCK, and LE. Power save control for the PDP module is effected through Pins 32, 33, 34, 35, and 36 of the AD connector. Pin 34 is used for the average brightness data input from the PDP module.

(9) Voice control block

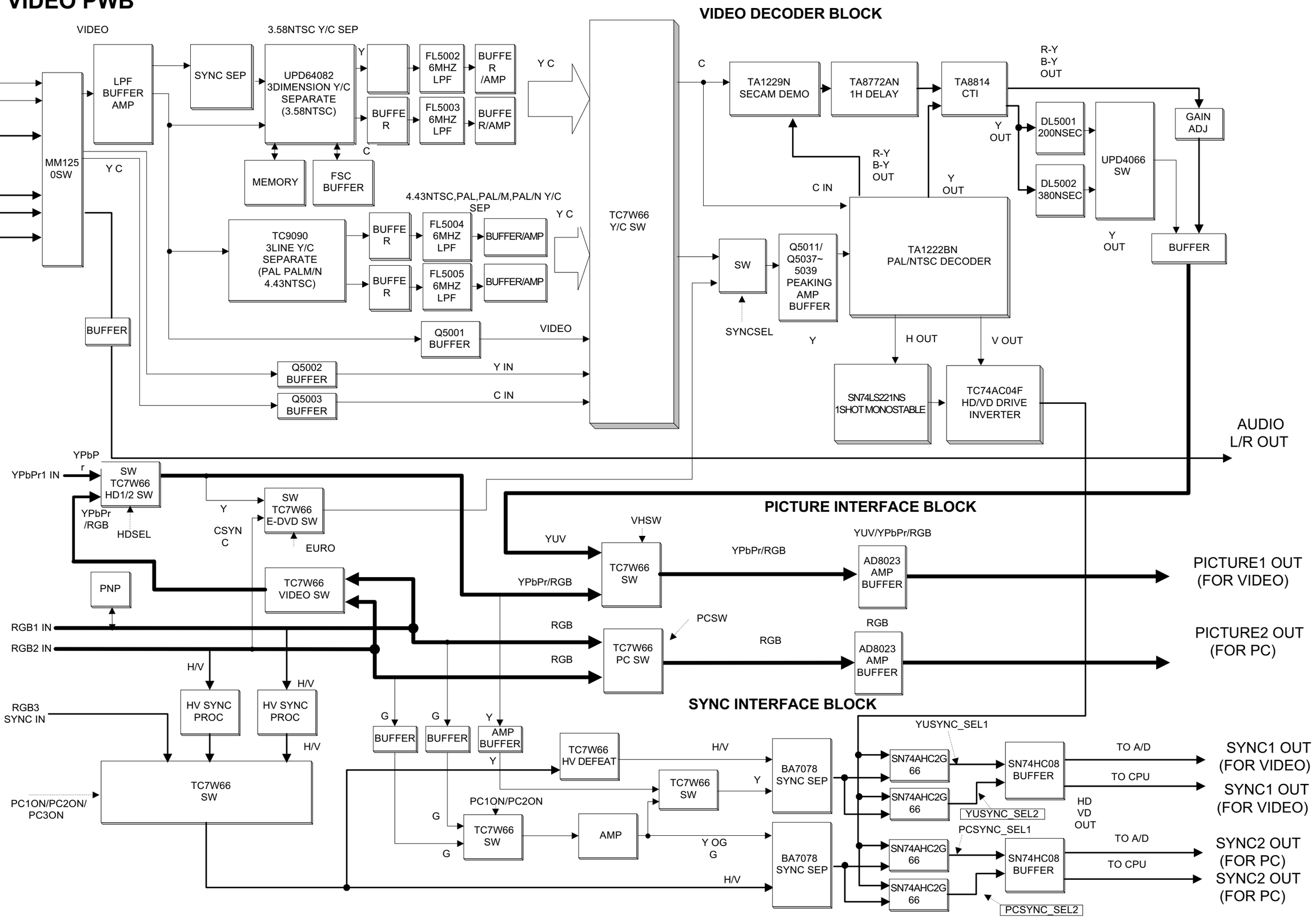
The AUDIO unit controls the sound volume, balance, and the sound quality through IC9505 with the aid of the bus SDA2AE and SCL2AE. Transmission of the voice output is suspended when Pin 3 of the AE connector (SMUTE terminal) is at the “H” level or when Pin 4 of the AE connector (POMUTE terminal) is at the “L” level.

CONNECTION DIAGRAM

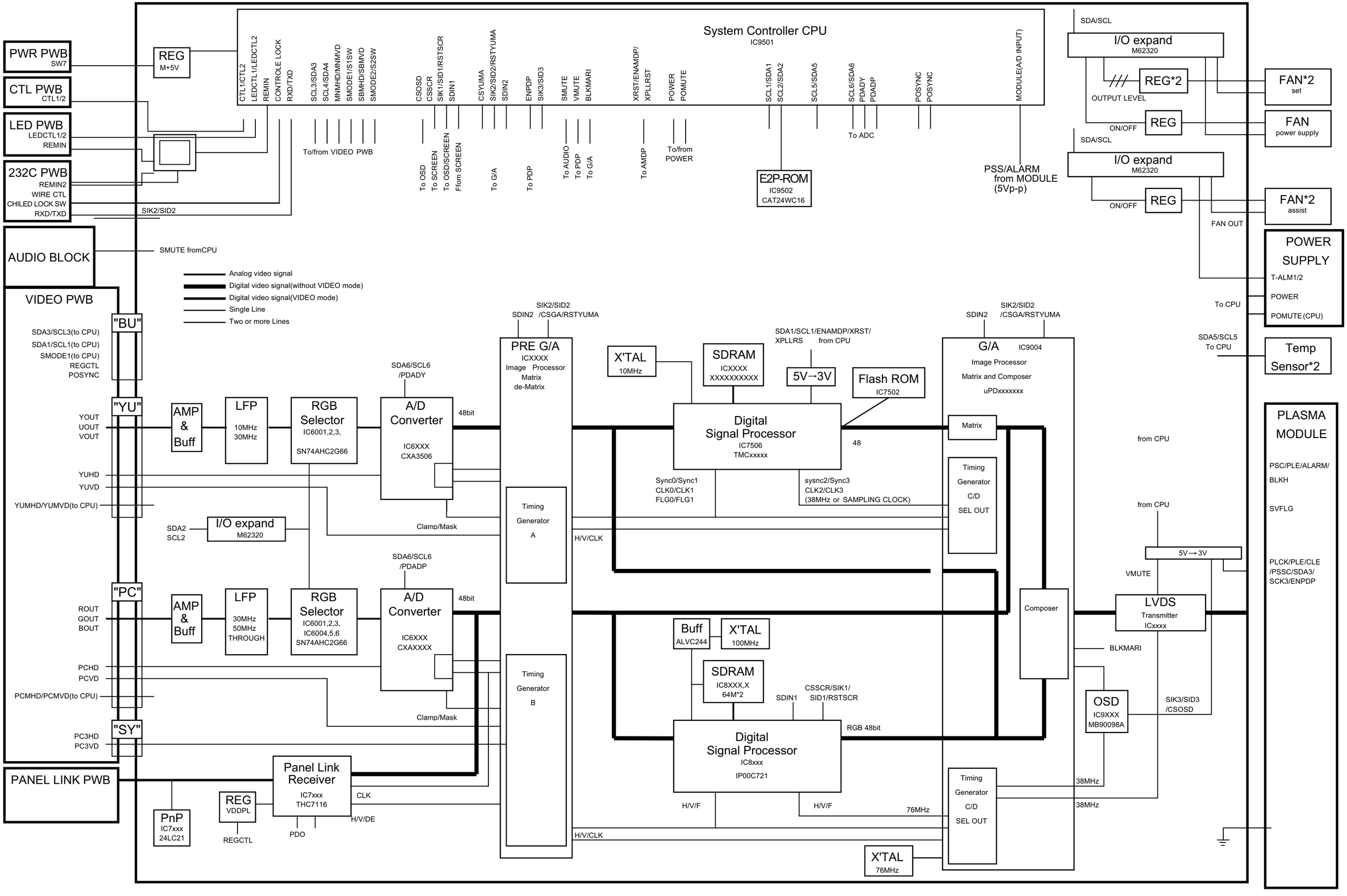


BLOCK DIAGRAM

▪ VIDEO PWB



▪ MAIN PWB


PWR PWB
SW7
REG
M+5V
CTL PWB
CTL1/2
LED PWB
LEDCTL1/2
REMIN
232C PWB
REMIN2
WIRE CTL
CHILED LOCK SW
RXD/TXD
SIK2/SID2
AUDIO BLOCK
SMUTE fromCPU
System Controller CPU
IC9501
CTL1/CTL2
LEDCTL1/LEDCTL2
REMIN
CONTROLE LOCK
RXD/TXD
SCL3/SDA3
SCL4/SDA4
MNMHD/MNMVD
SMODE1/S1SW
SBMHD/SBMVD
SMODE2/S2SW
To/from VIDEO PWB
CSOSD
CSSCR
SIK1/SID1/RSTSCR
SDIN1
To OSD
To SCREEN
To OSD/SCREEN
Ffom SCREEN
CSYUMA
SIK2/SID2/RSTYUMA
SDIN2
To G/A
ENPDP
SIK3/SID3
To PDP
SMUTE
VMUTE
BLKMARI
To AUDIO
To PDP
To G/A
XRST/ENAMDP/
XPLLRST
To AMDP
POWER
POMUTE
To/from
POWER
SCL1/SDA1
SCL2/SDA2
E2P-ROM
IC9502
CAT24WC16
SCL5/SDA5
SCL6/SDA6
PDADY
PDADP
To ADC
POSYNC
POSYNC
MODULE(A/D INPUT)
PSS/ALARM
from MODULE
(5Vp-p)
SDA/SCL
I/O expand
M62320
REG*2
OUTPUT LEVEL
ON/OFF
REG
FAN*2
set
FAN
power supply
SDA/SCL
I/O expand
M62320
ON/OFF
REG
FAN*2
assist
FAN OUT
POWER
SUPPLY
T-ALM1/2
POWER
POMUTE(CPU)
To CPU
SDA5/SCL5
To CPU
Temp
Sensor*2
PLASMA
MODULE
PSC/PLE/ALARM/
BLKH
SVFLG
PLCK/PLE/CLE
/PSSC/SDA3/
SCK3/ENPDP
Analog video signal
Digital video signal(without VIDEO mode)
Digital video signal(VIDEO mode)
Single Line
Two or more Lines
VIDEO PWB
"BU"
SDA3/SCL3(to CPU)
SDA1/SCL1(to CPU)
SMODE1(to CPU)
REGCTL
POSYNC
"YU"
YOUT
UOUT
VOUT
AMP
&
Buff
LFP
10MHz
30MHz
RGB
Selector
IC6001,2,3,
SN74AHC2G66
A/D
Converter
IC6XXX
CXA3506
48bit
SDA6/SCL6
/PDADY
SIK2/SID2
SDIN2 /CSGA/RSTYUMA
PRE G/A
ICXXXX
Image Processor
Matrix
de-Matrix
X'TAL
10MHz
SDRAM
ICXXXX
XXXXXXXXXX
SDA1/SCL1/ENAMDP/XRST/
XPLLRS from CPU
5V→3V
Flash ROM
IC7502
Digital
Signal Processor
IC7506
TMCxxxxx
48
Sync0/Sync1
CLK0/CLK1
FLG0/FLG1
sysnc2/Sync3
CLK2/CLK3
(38MHz or SAMPLING CLOCK)
SIK2/SID2
SDIN2 /CSGA/RSTYUMA
G/A IC9004
Image Processor
Matrix and Composer
uPDxxxxxx
Matrix
Timing
Generator
C/D
SEL OUT
from CPU
YHD
YVD
YUMHD/YUMVD(to CPU)
SDA2
SCL2
I/O expand
M62320
Clamp/Mask
Timing
Generator
A
H/V/CLK
"PC"
ROUT
GOUT
BOUT
AMP
&
Buff
LFP
30MHz
50MHz
THROUGH
RGB
Selector
IC6001,2,3,
IC6004,5,6
SN74AHC2G66
A/D
Converter
IC6XXX
CXAXXXX
48bit
SDA6/SCL6
/PDADP
PCHD
PCVD
PCMHD/PCMVD(to CPU)
Clamp/Mask
Timing
Generator
B
Buff
ALVC244
X'TAL
100MHz
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IC8XXX,X
64M*2
CSSCR/SIK1/
SID1/RSTSCR
SDIN1
Digital
Signal Processor
IC8xxx
IP00C721
RGB 48bit
H/V/F
H/V/F
76MHz
Timing
Generator
C/D
SEL OUT
H/V/CLK
X'TAL
76MHz
Composer
from CPU
5V→3V
VMUTE
LVDS
Transmitter
ICxxxx
BLKMARI
OSD
IC9XXX
MB90098A
SIK3/SID3
/CSOSD
38MHz
38MHz
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PC3HD
PC3VD
PANEL LINK PWB
Panel Link
Receiver
IC7xxx
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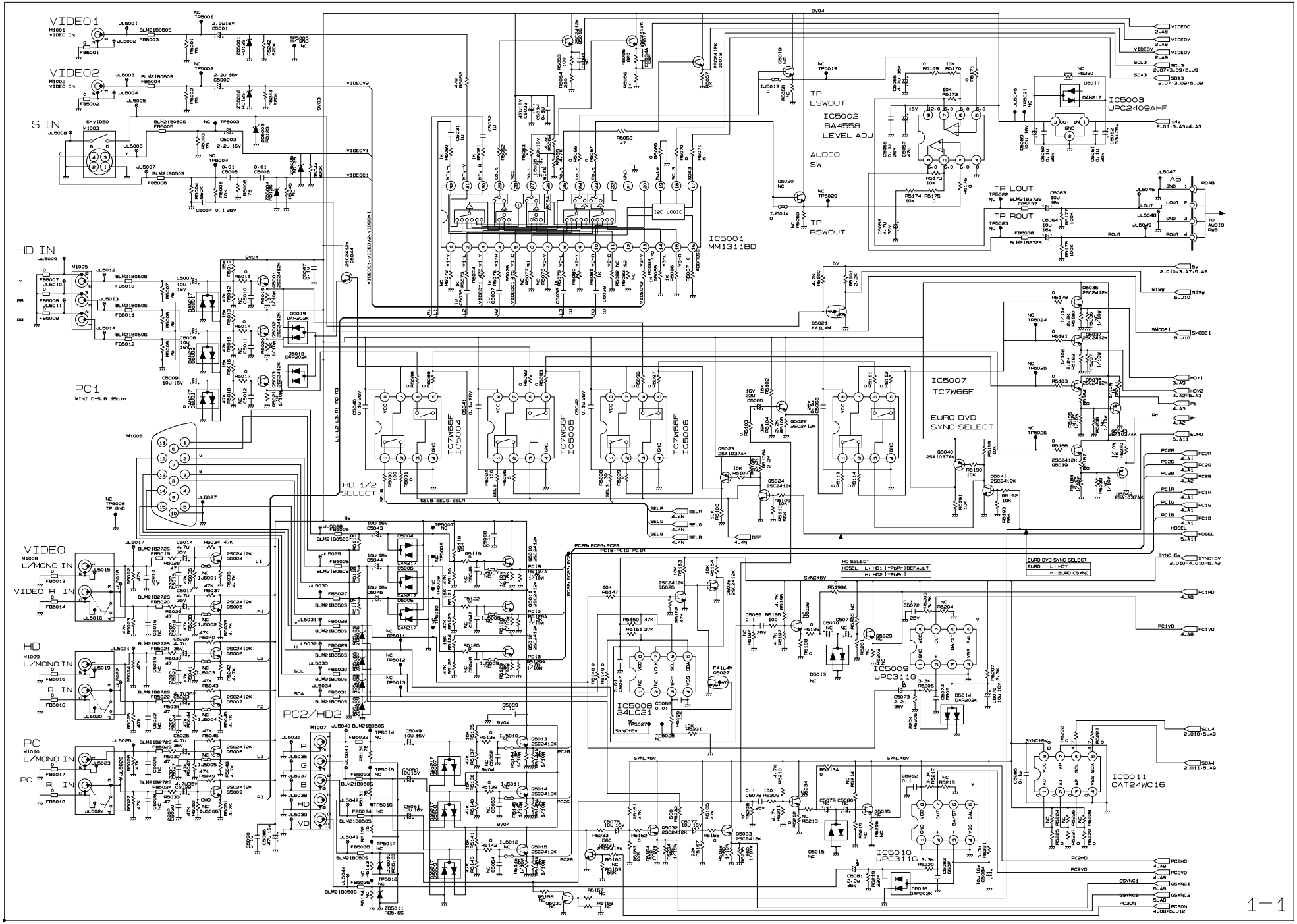
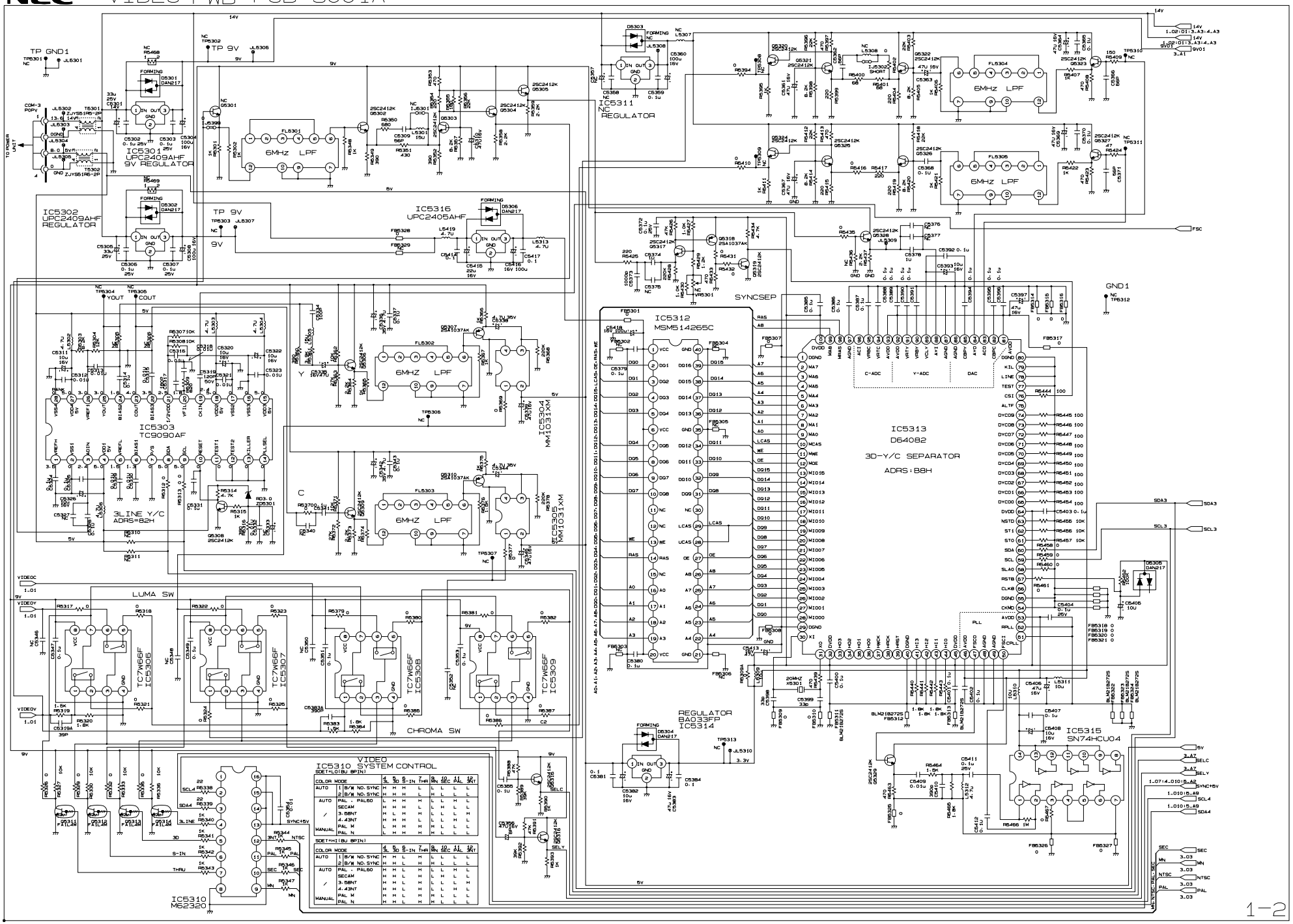
H/V/DE
PDO
REG
VDDPL
REGCTL
PnP
IC7xxx
24LC21

NEC VIDEO PWB PCB-5001A

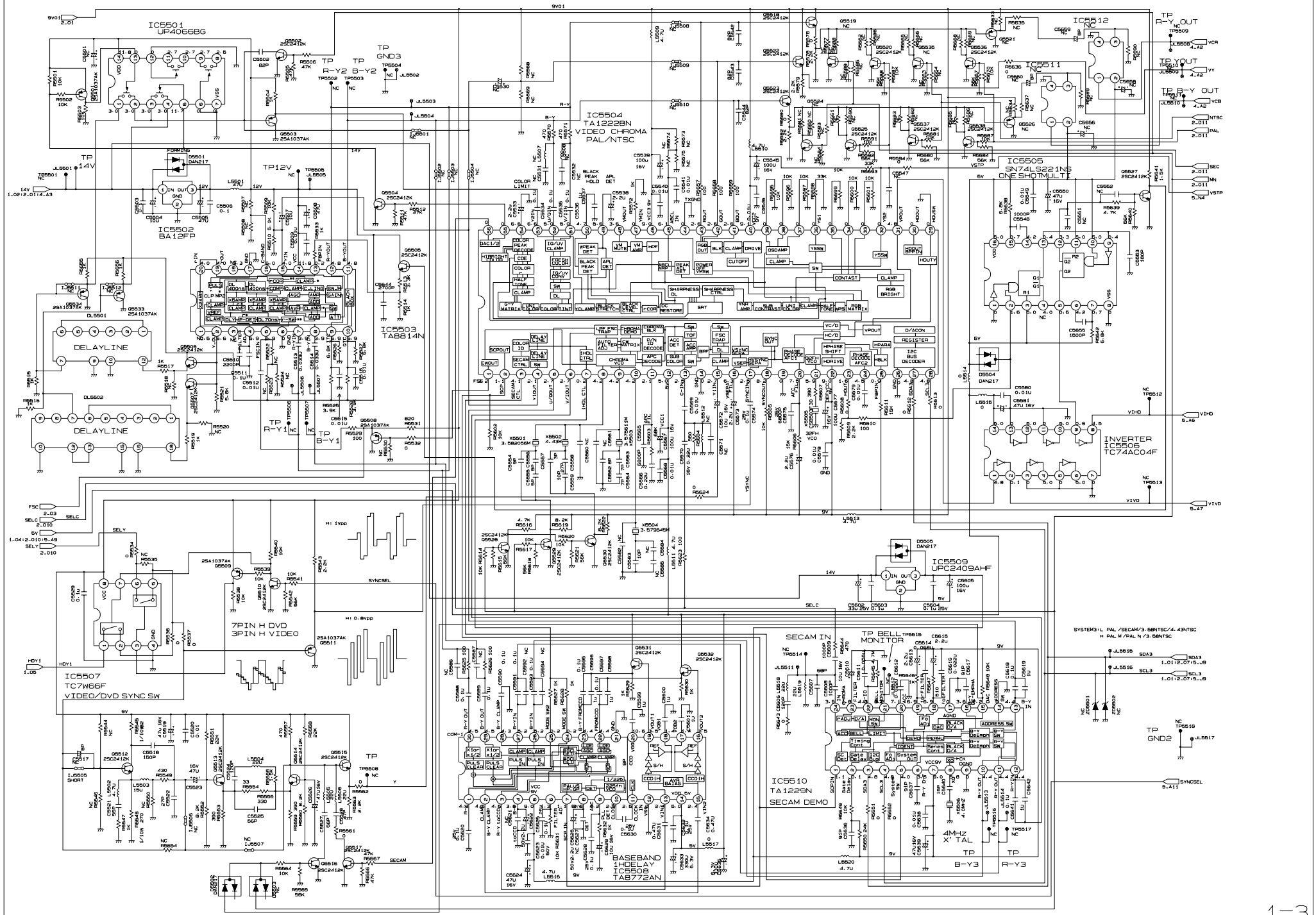


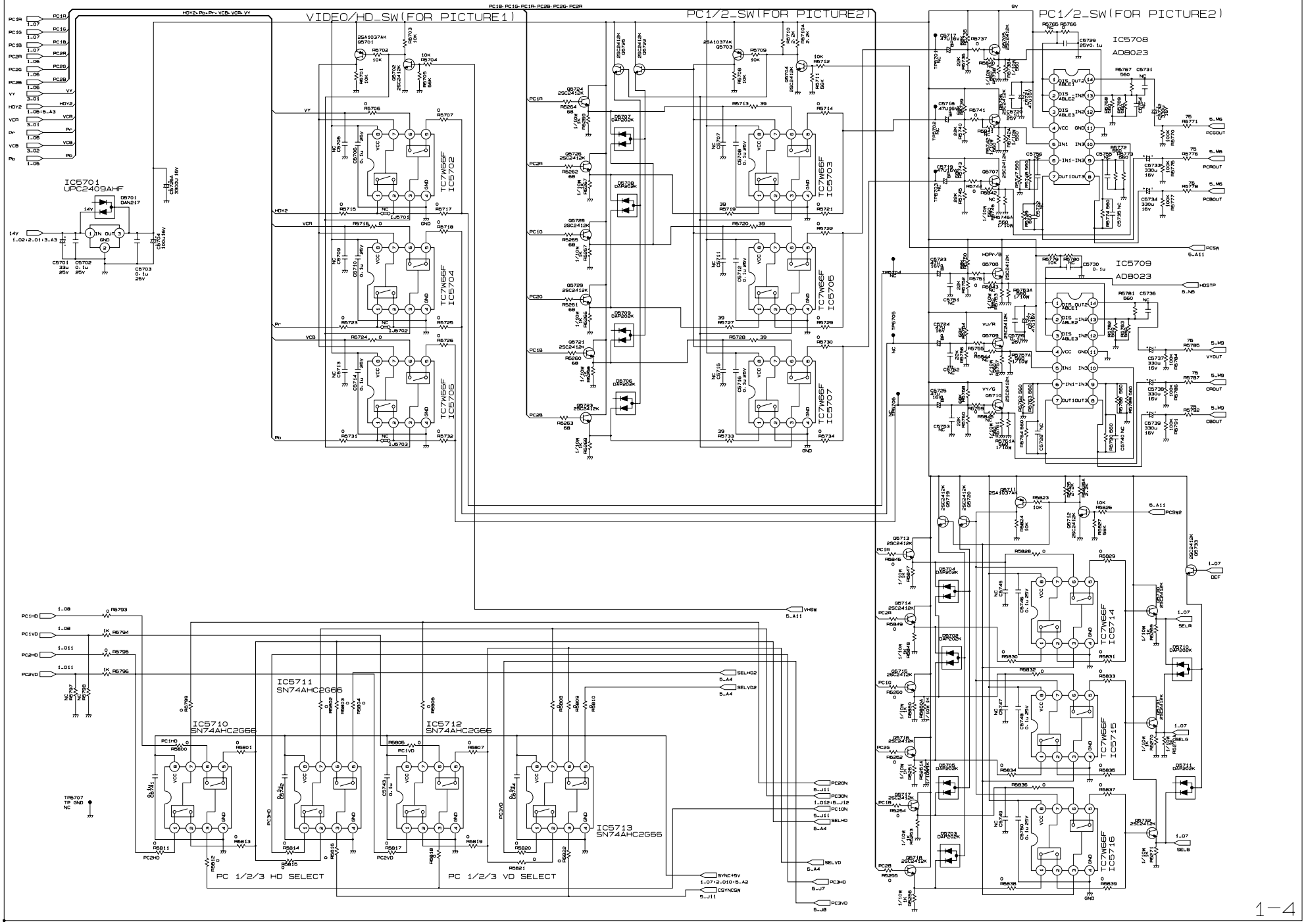
1-1

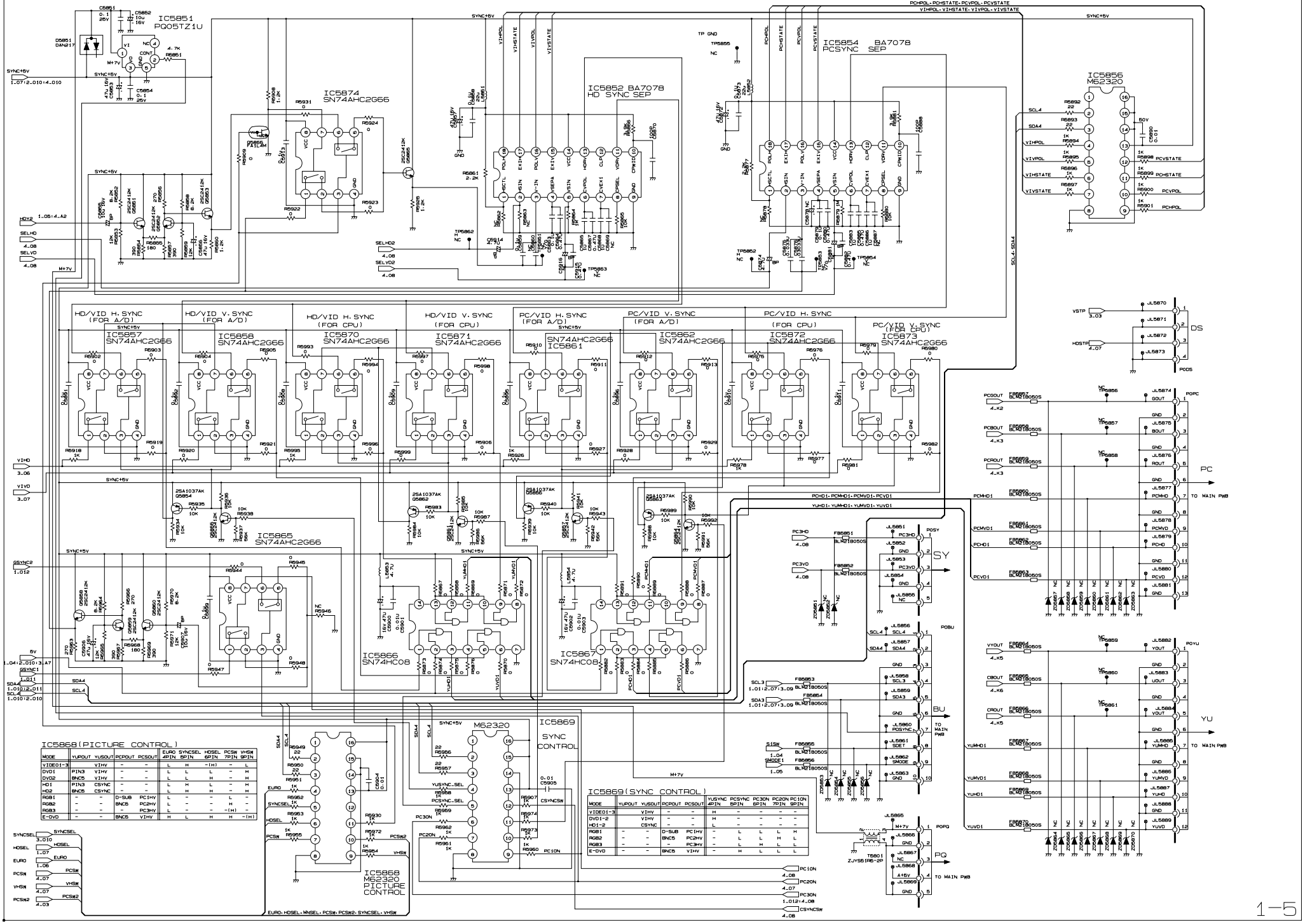
NEC VIDEO PWB PCB-5001A



1—2


IC5501
UP4066BG
IC5502
BA12FP
IC5503
TA8814N
IC5504
TA1222BN
VIDEO CHROMA
PAL/NTSC
IC5505
SN74LS221NS
ONE SHOTMULTI
IC5506
TC74AC04F
INVERTER
IC5507
TC7W66F
VIDEO/DVD SYNC SW
IC5508
TA8772AN
BASEBAND
IDELAY
IC5509
UPC2409AHF
IC5510
TA1229N
SECAM DEMO
IC5511
IC5512
DELAYLINE
DELAYLINE
7PIN H DVD
3PIN H VIDEO
SECAM IN
TP BELL
MONITOR
4MHZ
X'TAL
TP R-Y OUT
TP Y OUT
TP B-Y OUT
TP GND3
TP R-Y2 B-Y2
TP 14V
TP12V
TP R-Y1
TP B-Y1
TP GND2
TP B-Y3
TP R-Y3
SYSTEM:L PAL /SECAM/3.58NTSC/4.43NTSC
H PAL M/PAL N/3.58NTSC


VIDEO/HD_SW(FOR PICTURE1)
PC1/2_SW(FOR PICTURE2)
PC1/2_SW(FOR PICTURE2)
IC5701
UPC2409AHF
IC5702
IC5703
IC5704
IC5705
IC5706
IC5707
IC5708
AD8023
IC5709
AD8023
IC5710
SN74AHC2G66
IC5711
SN74AHC2G66
IC5712
SN74AHC2G66
IC5713
SN74AHC2G66
IC5714
IC5715
IC5716
PC 1/2/3 HD SELECT
PC 1/2/3 VD SELECT



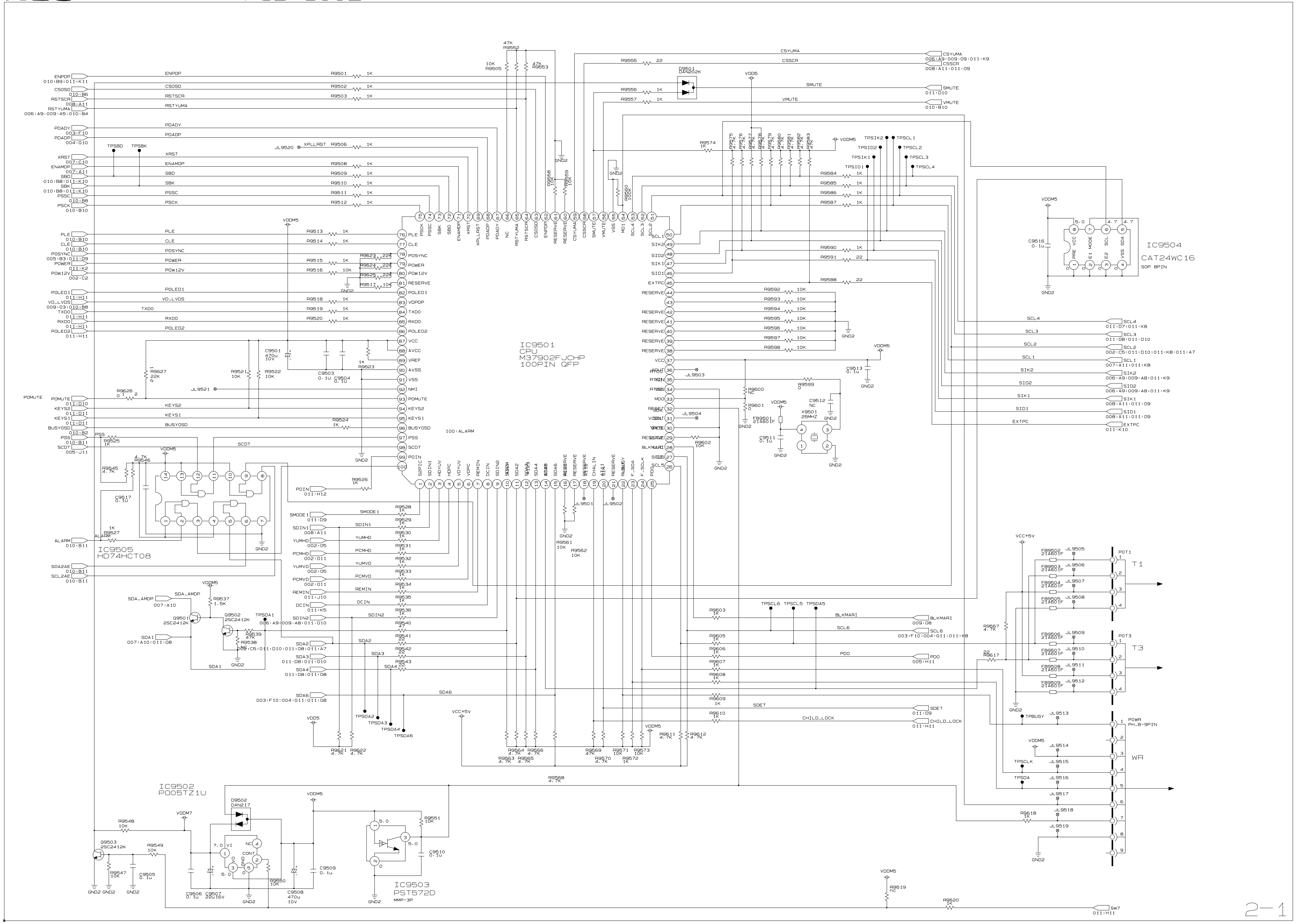
IC5868(PICTURE CONTROL)

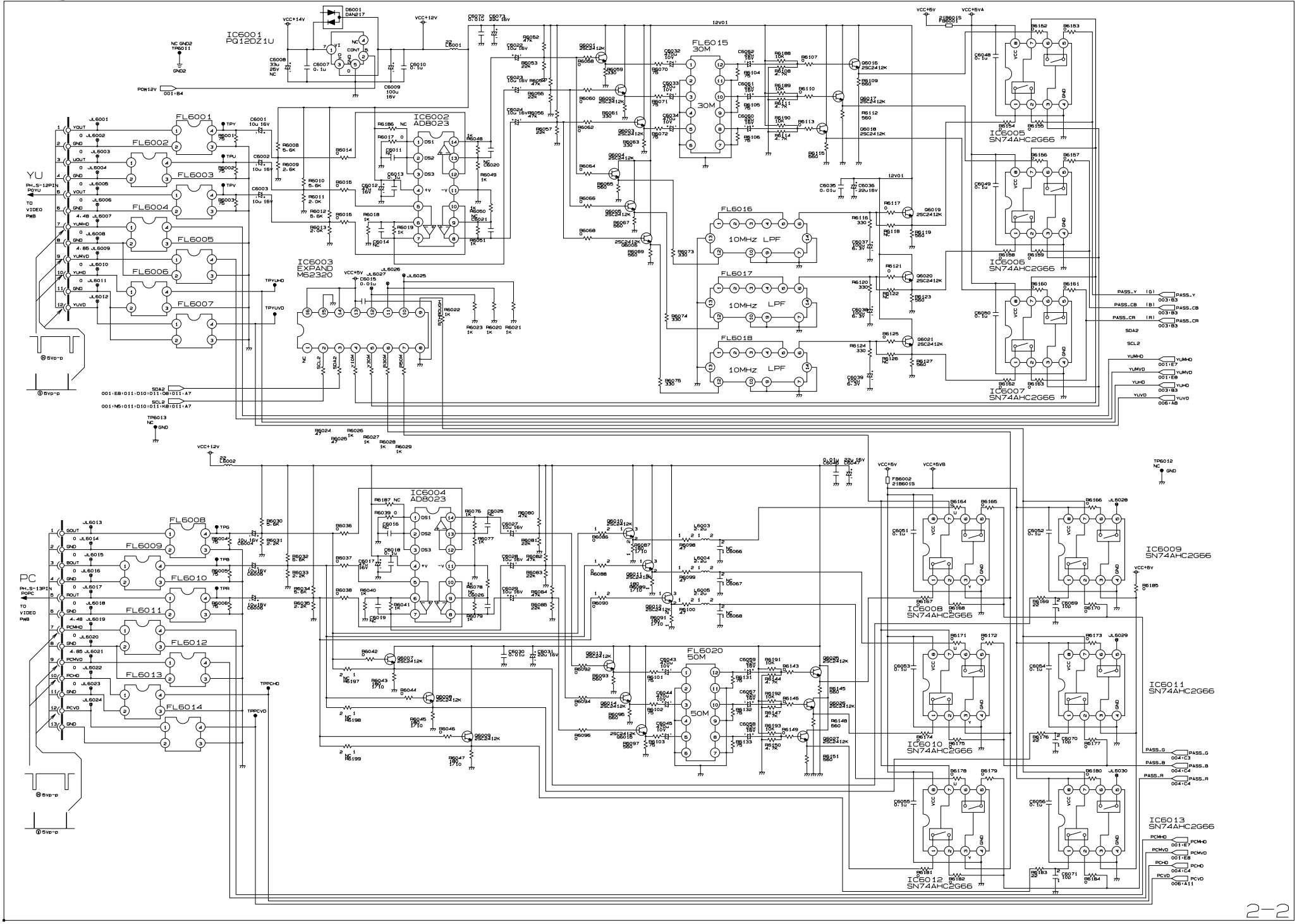
MODE	YUPOUT	YUSOUT	PCPOUT	PCSOUT	EURO 4PIN	SYNCSEL 8PIN	HDSEL 6PIN	PCSW 7PIN	VHSW 9PIN
VIDEO1-3		VIHV	-	-	L	H	-(H)	-	L
DVD1	PIN3	VIHV	-	-	L	L	L	-	H
DVD2	BNC5	VIHV	-	-	L	L	H	-	H
HD1	PIN3	CSYNC	-	-	L	H	L	-	H
HD2	BNC5	CSYNC	-	-	L	H	H	-	H
RGB1	-	-	D-SUB	PC1HV	L	-	-	L	-
RGB2	-	-	BNC5	PC2HV	L	-	-	H	-
RGB3	-	-	-	PC3HV	L	-	-	-(H)	-
E-DVD	-	-	BNC5	VIHV	H	L	H	H	-(H)

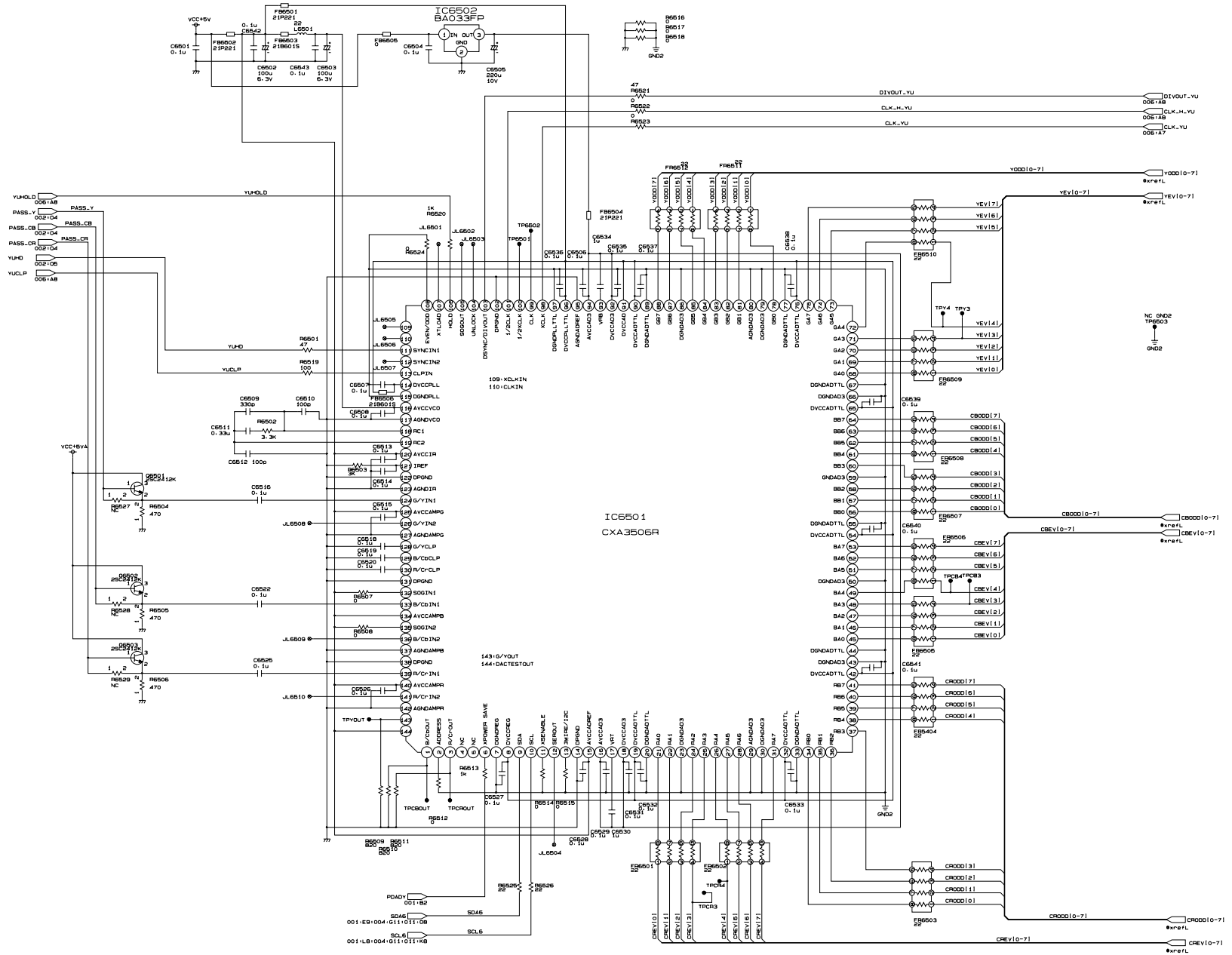
IC5869(SYNC CONTROL)

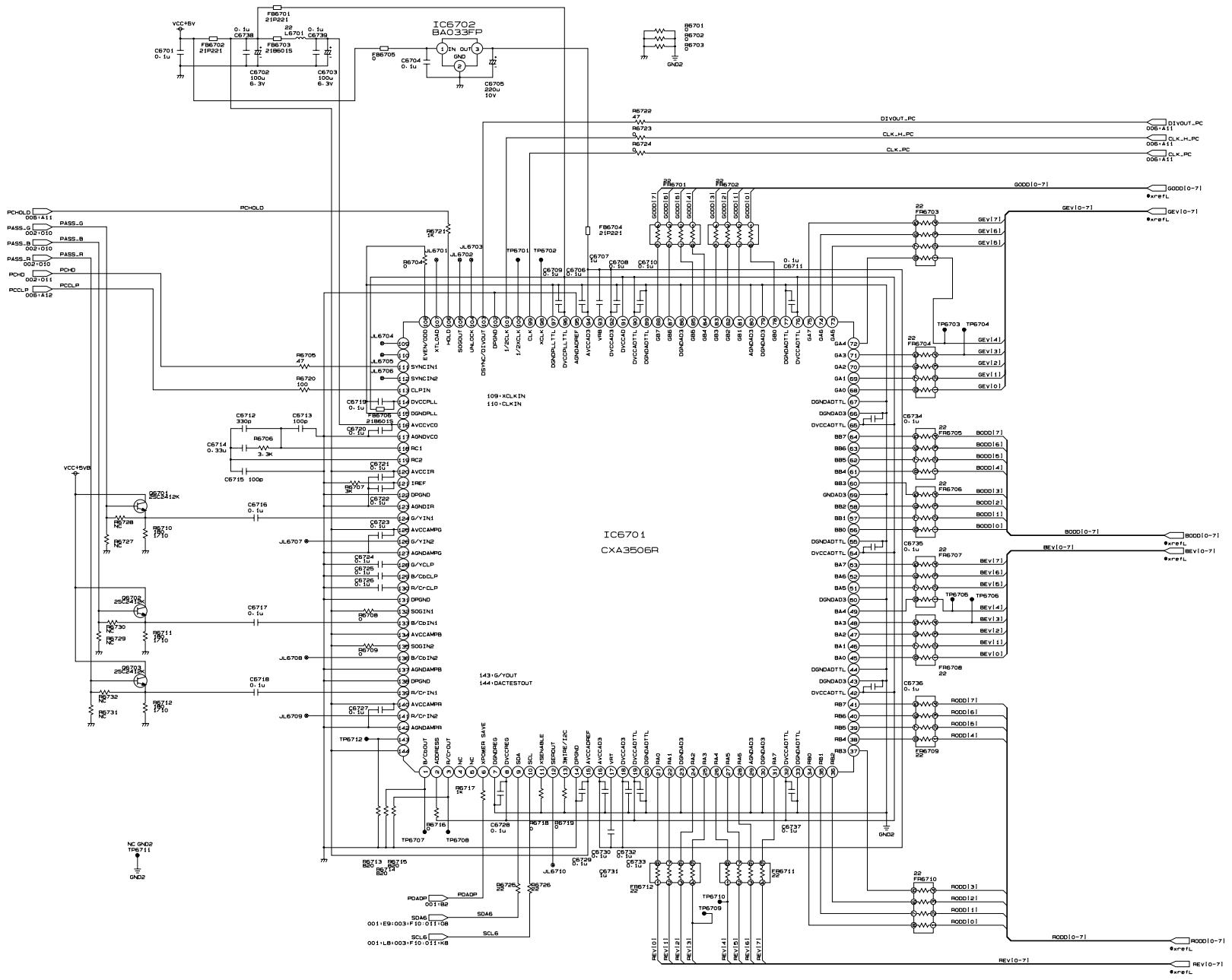
MODE	YUPOUT	YUSOUT	PCPOUT	PCSOUT	YUSYNC 4PIN	PCSYNC 6PIN	PC3ON 7PIN	PC2ON 8PIN	PC1ON 9PIN
VIDEO1-3		VIHV	-	-	H	-	-	-	-
DVD1-2		VIHV	-	-	H	-	-	-	-
HD1-2		CSYNC	-	-	L	-	-	-	-
RGB1	-	-	D-SUB	PC1HV	-	L	L	L	H
RGB2	-	-	BNC5	PC2HV	-	L	L	H	L
RGB3	-	-	-	PC3HV	-	L	H	L	L
E-DVD	-	-	BNC5	VIHV	-	H	L	L	L

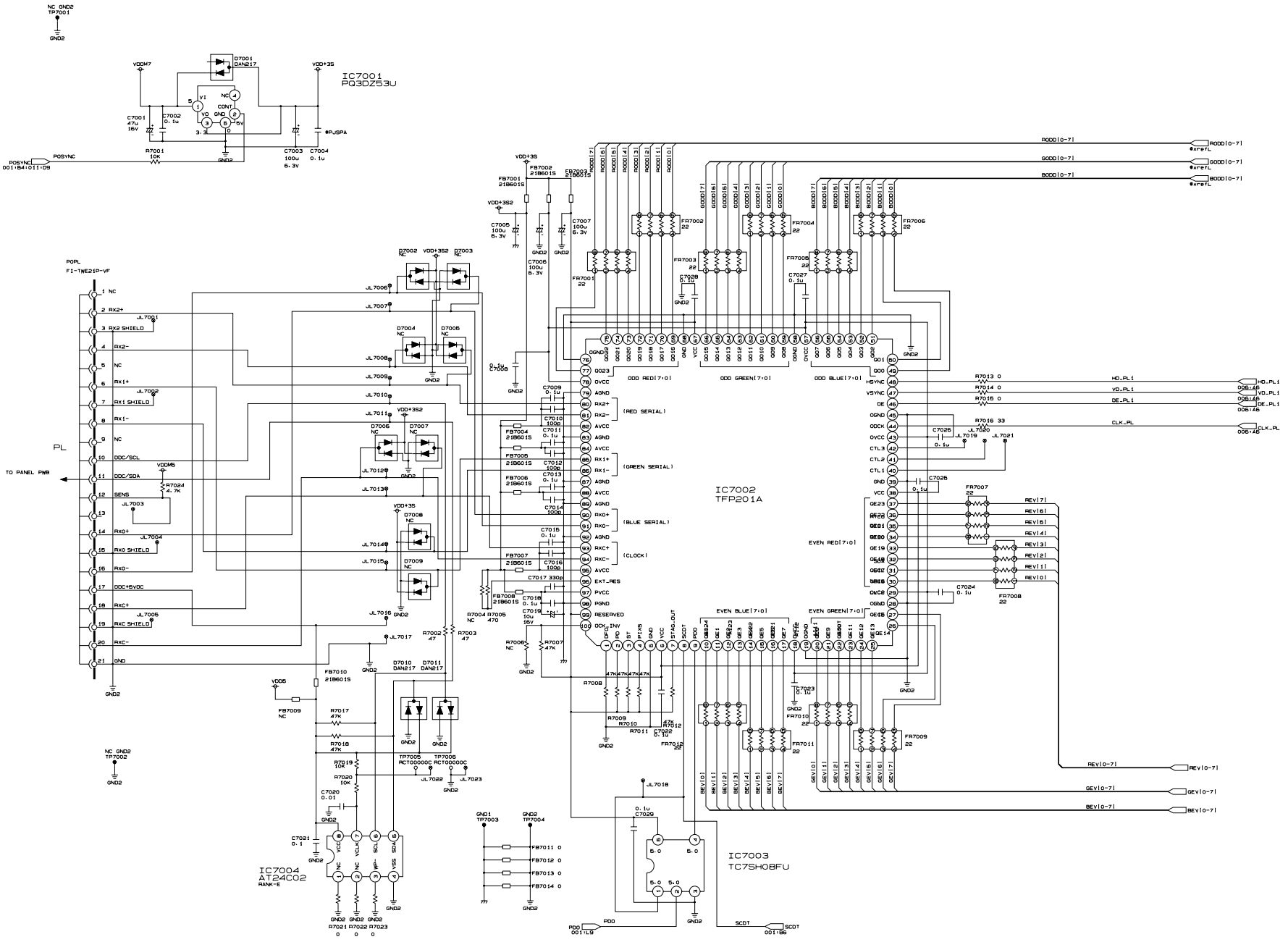
NEC MAIN PWB PCB-5002

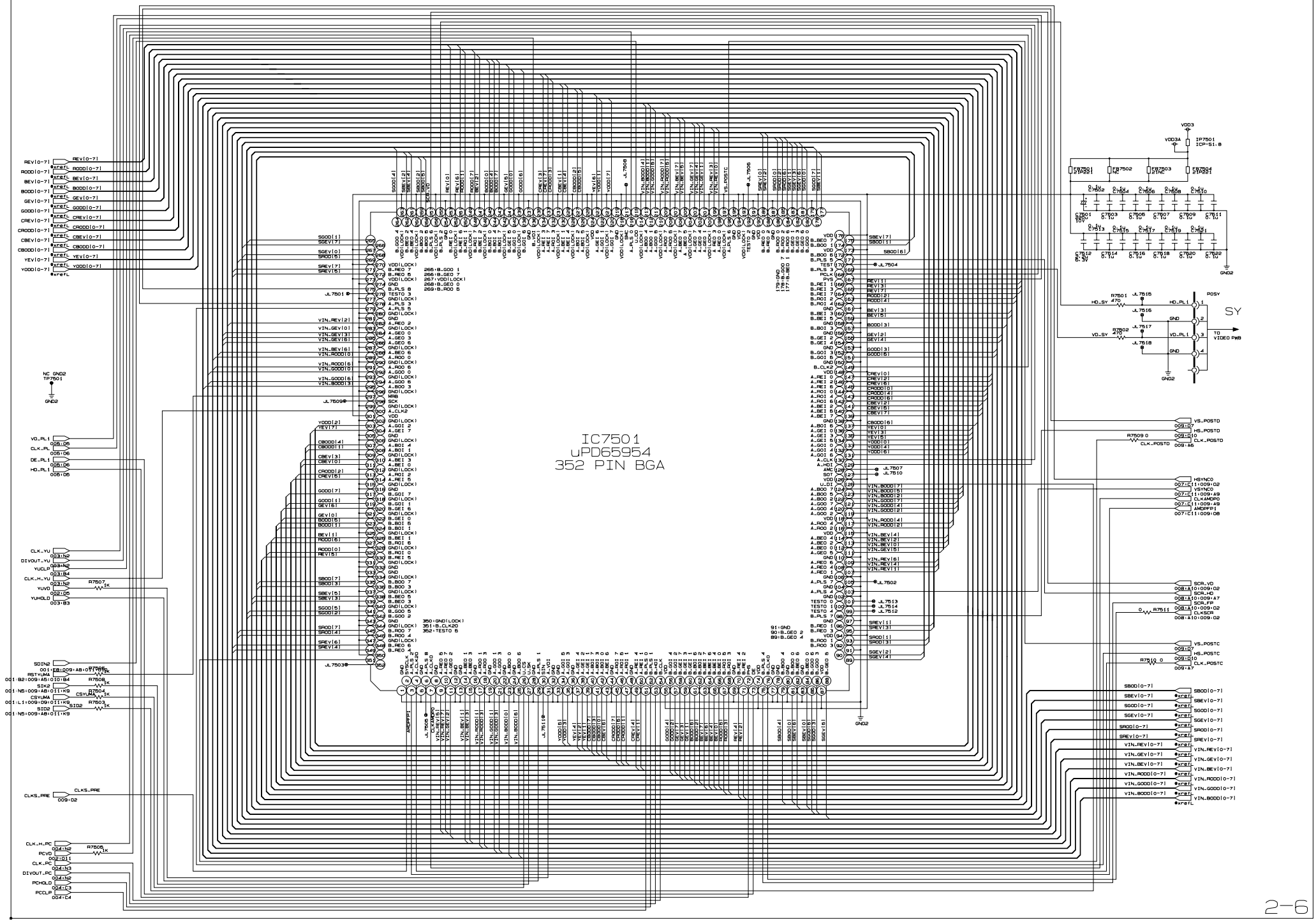


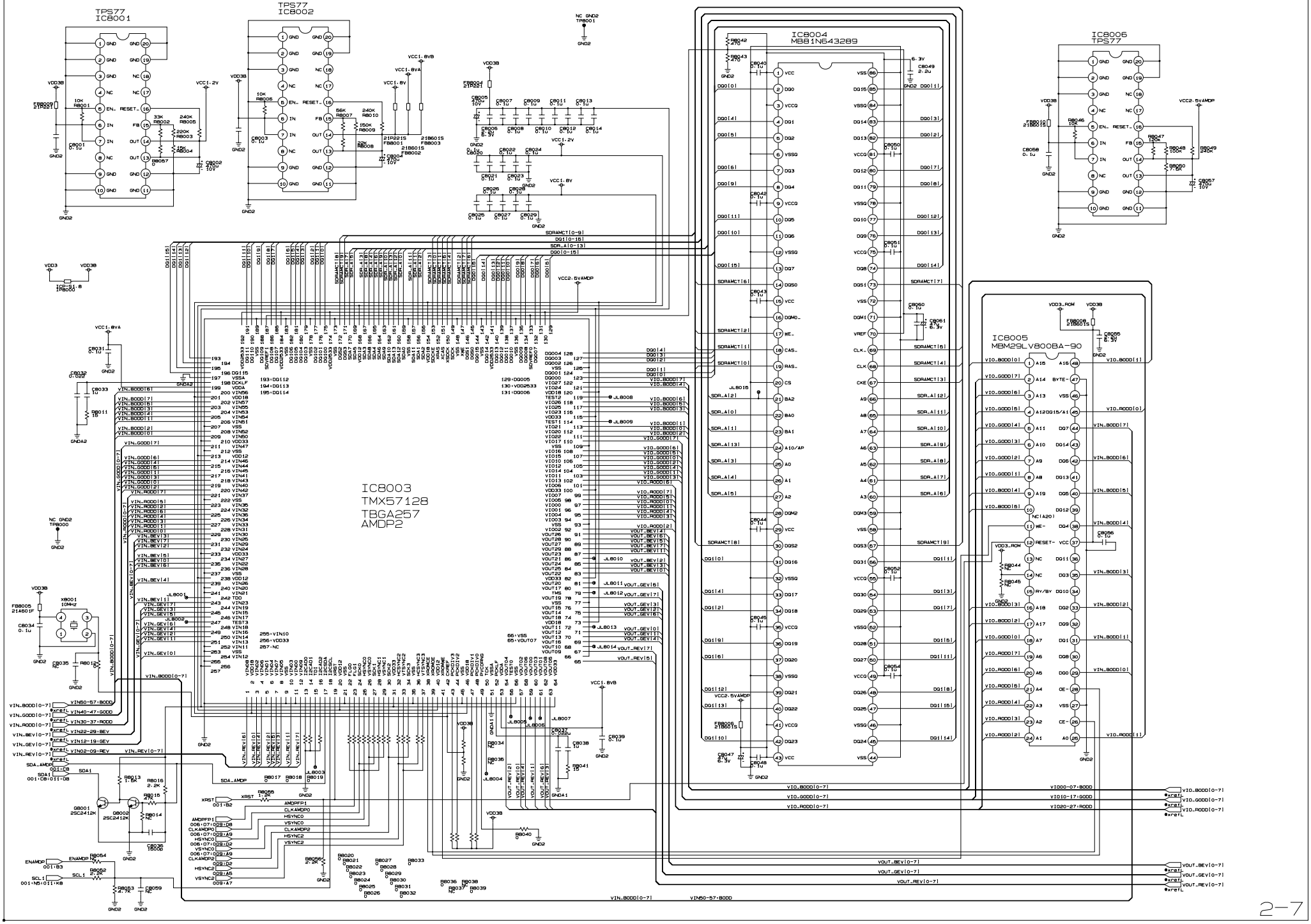

IC6001
PQ12DZ1U
IC6002
AD8023
IC6003
EXPAND
M62320
IC6004
AD8023
FL6015
30M
FL6016
10MHz LPF
FL6017
10MHz LPF
FL6018
10MHz LPF
FL6020
50M
IC6005
SN74AHC2G66
IC6006
SN74AHC2G66
IC6007
SN74AHC2G66
IC6008
SN74AHC2G66
IC6009
SN74AHC2G66
IC6010
SN74AHC2G66
IC6011
SN74AHC2G66
IC6012
SN74AHC2G66
IC6013
SN74AHC2G66
YU
PC
TO VIDEO PWB

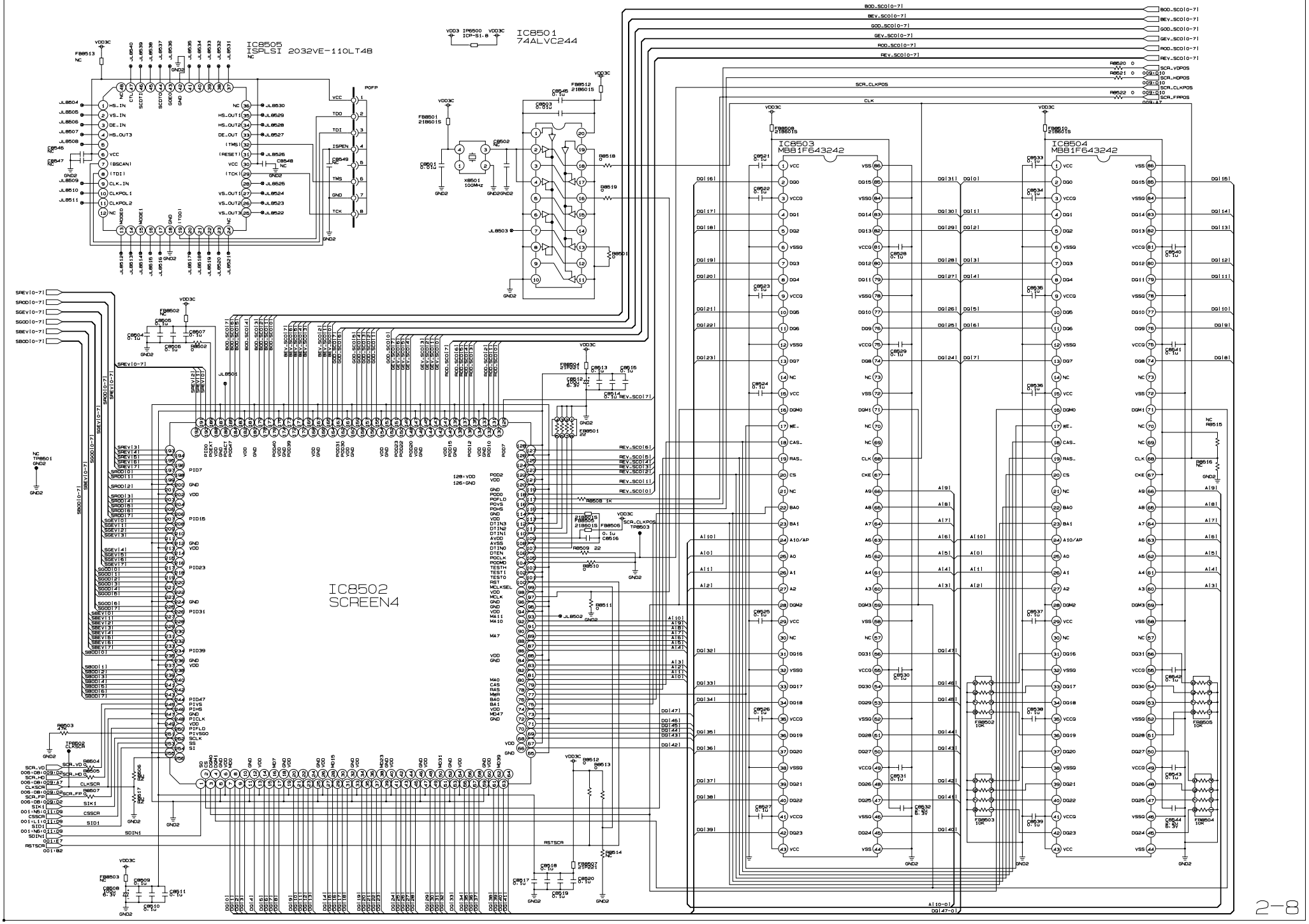

IC6502
BA033FP
IC6501
CXA3506R
VCC+5V
GND2
DIVOUT_YU
CLK-H_YU
CLK-YU
YUHOLD
PASS_Y
PASS_CB
PASS_CR
YUHD
YUCLP
YDD[0-7]
YEV[0-7]
CBOD[0-7]
CBEV[0-7]
CROD[0-7]
CREV[0-7]
SDA6
SCL6
PDADY
TPVOUT
TPCBOUT
TPCROUT
109:XCLKIN
110:CLKIN
143:G/YOUT
144:DACTESTOUT

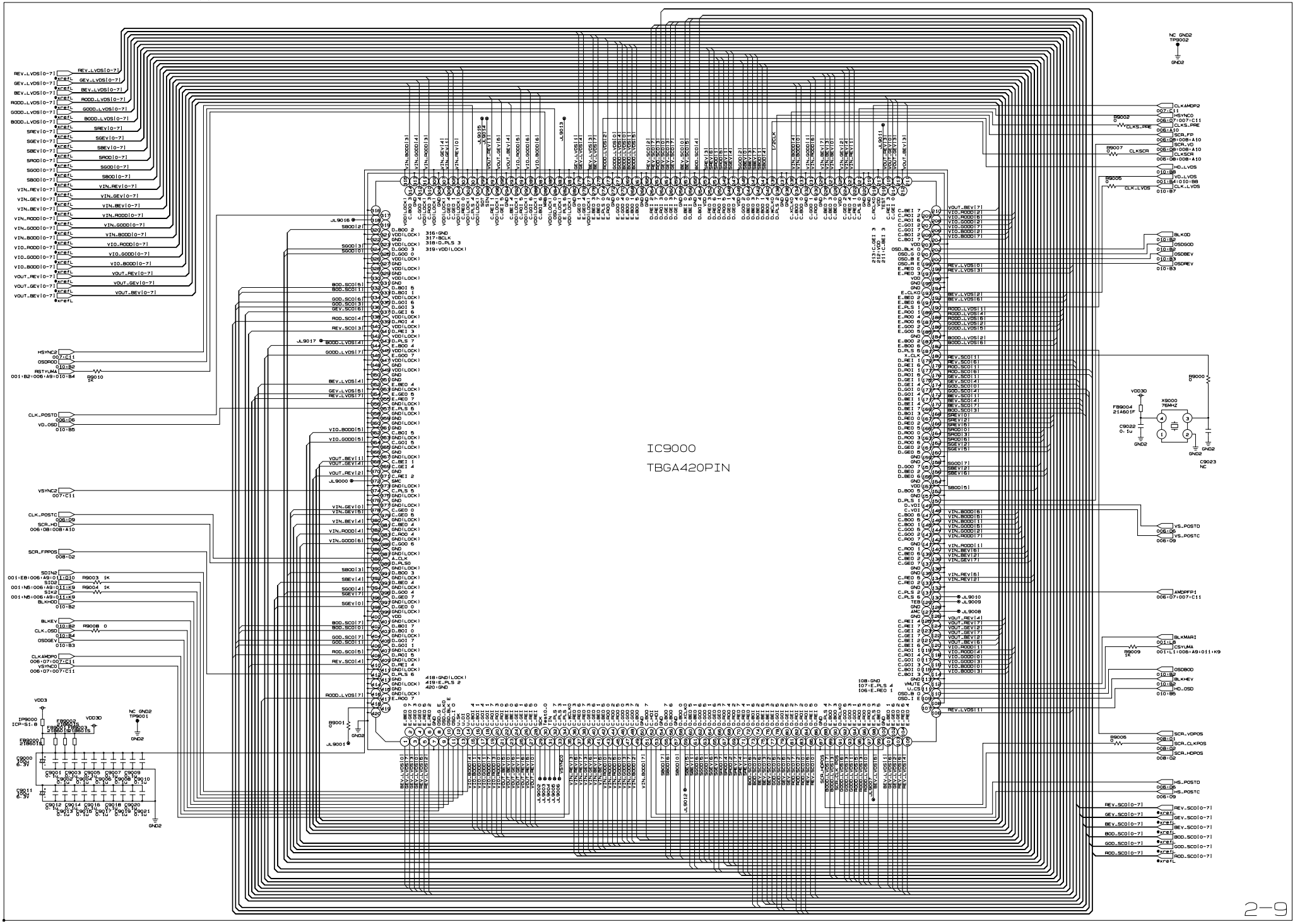

IC6702
BA033FP
IC6701
CXA3506R
VCC+5V
VCC+5VB
GND2
NC GND2
PCHOLD
PASS_G
PASS_B
PASS_R
PCHO
PCCLP
DIVOUT_PC
CLK_H_PC
CLK_PC
GOOD[0-7]
GEV[0-7]
BOOD[0-7]
BEV[0-7]
ROOD[0-7]
REV[0-7]
PDADP
SDA6
SCL6
109:XCLKIN
110:CLKIN
143:G/YOUT
144:DACTESTOUT

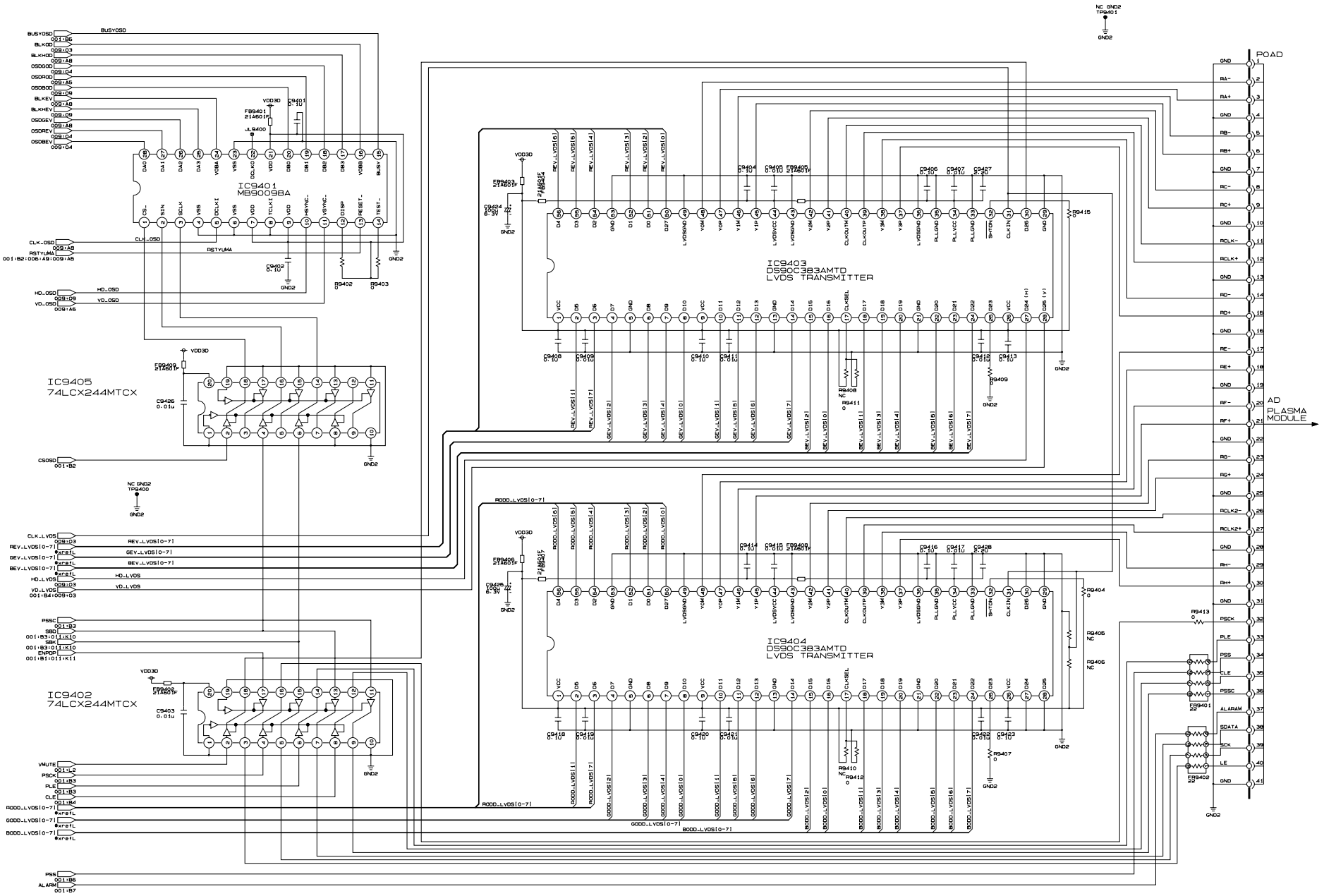

IC7001
PQ3DZ53U
IC7002
TFP201A
IC7003
TC7SH08FU
IC7004
AT24C02
PL
TO PANEL PWB
ODD RED[7:0]
ODD GREEN[7:0]
ODD BLUE[7:0]
EVEN RED[7:0]
EVEN GREEN[7:0]
EVEN BLUE[7:0]
(RED SERIAL)
(GREEN SERIAL)
(BLUE SERIAL)
(CLOCK)
RODD[0-7]
GODD[0-7]
BODD[0-7]
REVE[0-7]
GEVE[0-7]
BEVE[0-7]
HD_PL
VD_PL
DE_PL
CLK_PL
POSYNC
SCDT
PDO

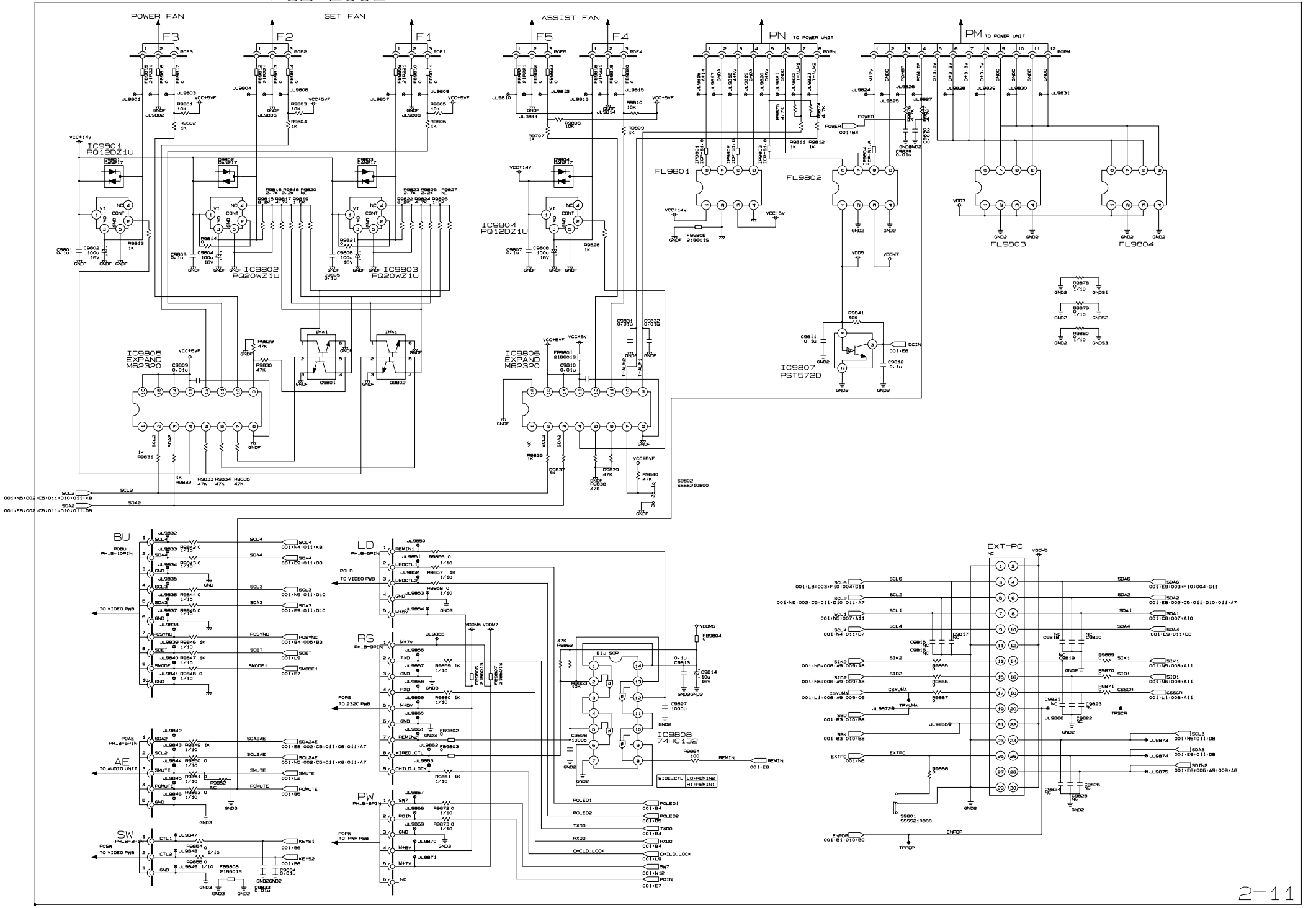

IC7501
uPD65954
352 PIN BGA

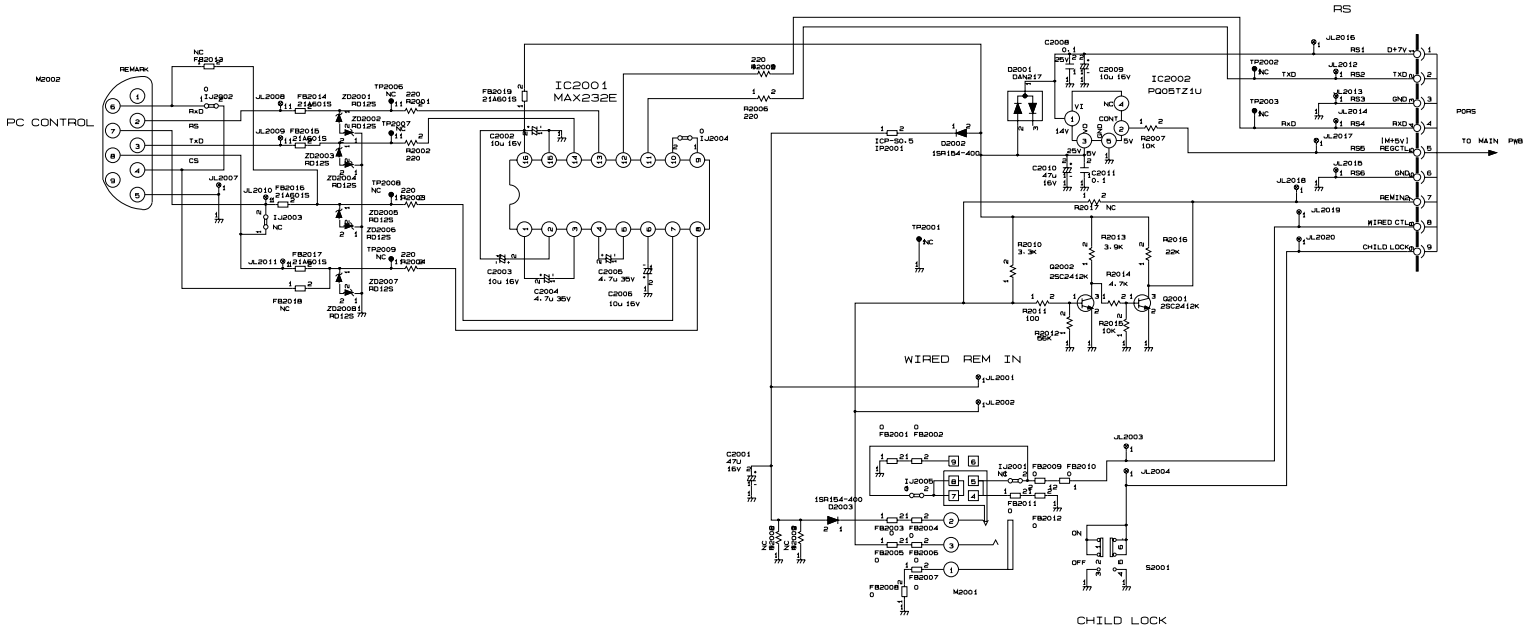

IC8001
TPS77
IC8002
TPS77
IC8004
MB81N643289
IC8006
TPS77
IC8005
MBM29LV800BA-90
IC8003
TMX57128
TBGA257
AMDP2

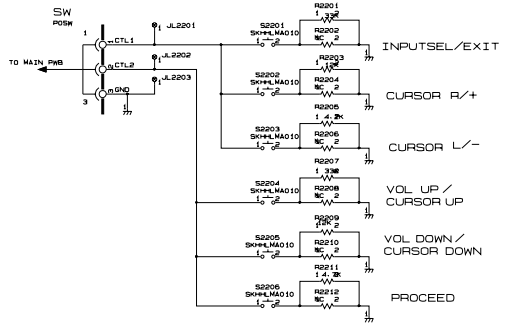

IC8505
ISPLSI 2032VE-110LT48
IC8501
74ALVC244
IC8503
MB81F643242
IC8504
MB81F643242
IC8502
SCREEN4

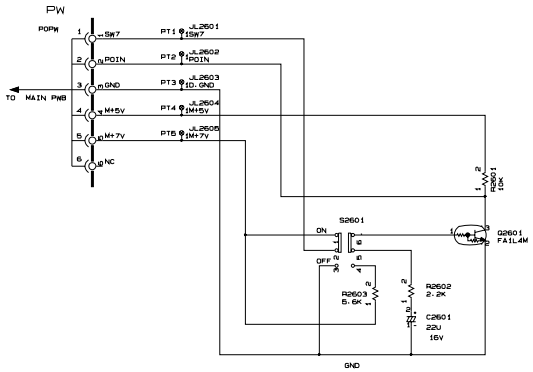

IC9000
TBGA420PIN

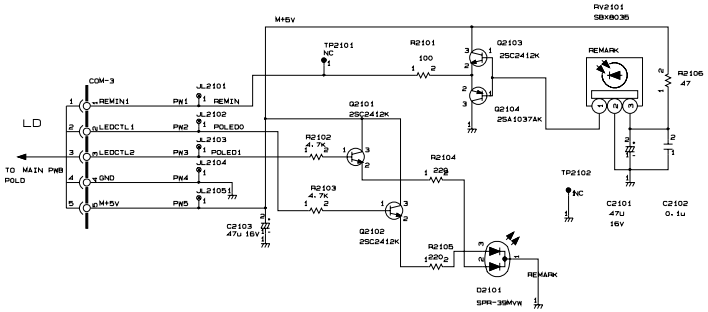

IC9401
MB90098A
IC9402
74LCX244MTCX
IC9403
DS90C383AMTD
LVDS TRANSMITTER
IC9404
DS90C383AMTD
LVDS TRANSMITTER
IC9405
74LCX244MTCX
POAD
AD
PLASMA
MODULE
BUSYOSD
CLK_OSD
HD_OSD
VD_OSD
CSOSD
REV_LVDS[0-7]
GEV_LVDS[0-7]
BEV_LVDS[0-7]
HD_LVDS
VD_LVDS
PSSC
SBC
ENPDP
VMUTE
PSCK
PLE
CLE
RODD_LVDS[0-7]
GODD_LVDS[0-7]
BODD_LVDS[0-7]
PSS
ALARM
SDATA
SCK
LE
GND2
VDD3D

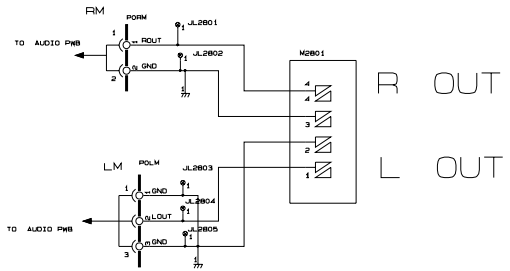

POWER FAN
SET FAN
ASSIST FAN
F3
F2
F1
F5
F4
PN TO POWER UNIT
PM TO POWER UNIT
IC9801 PQ12DZ1U
IC9802 PQ20WZ1U
IC9803 PQ20WZ1U
IC9804 PQ12DZ1U
FL9801
FL9802
FL9803
FL9804
IC9805 EXPAND M62320
IC9806 EXPAND M62320
IC9807 PST572D
BU
LD
RS
PW
SW
AE
EXT-PC
IC9808 74HC132
SCL2
SDA2
POLD
PORS
POPW
POSW
POAE
TO VIDEO PWB
TO AUDIO UNIT
TO 232C PWB
TO PWR PWB

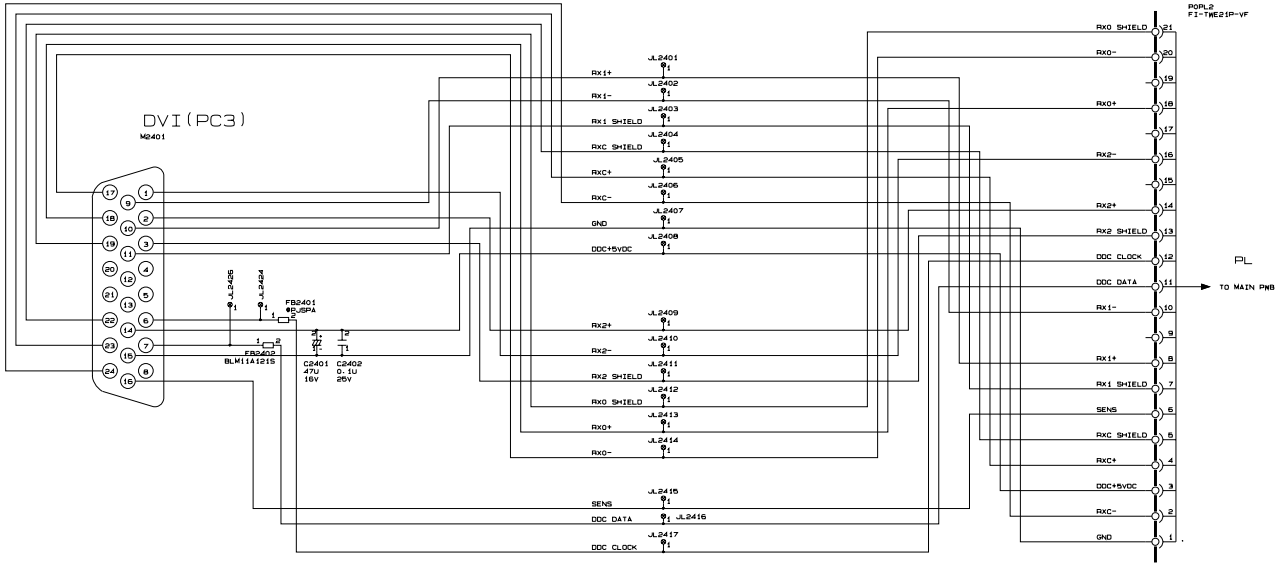

PC CONTROL
IC2001
MAX232E
IC2002
PQ05TZ1U
RS
WIRED REM IN
CHILD LOCK
TO MAIN PWB

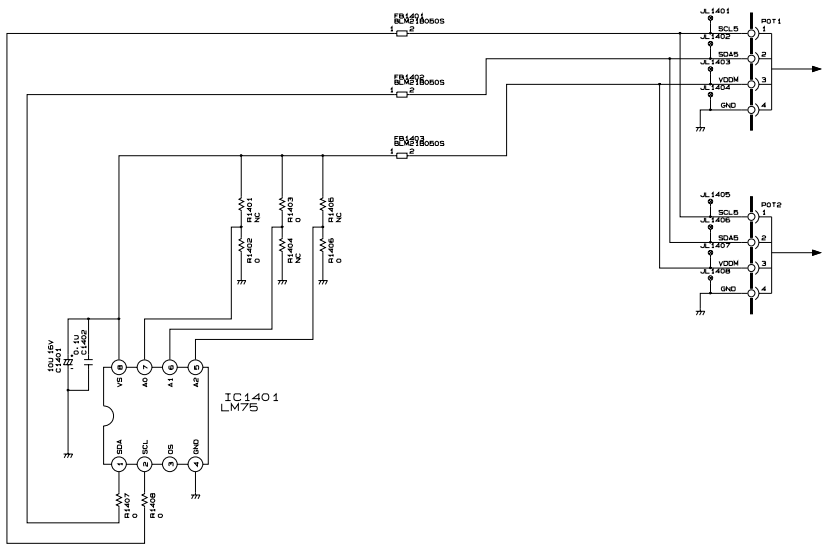

SW
POSW
TO MAIN PWB
CTL1
CTL2
GND
JL2201
JL2202
JL2203
S2201
S2202
S2203
S2204
S2205
S2206
SKHHLMA010
R2201
R2202
R2203
R2204
R2205
R2206
R2207
R2208
R2209
R2210
R2211
R2212
INPUTSEL/EXIT
CURSOR R/+
CURSOR L/−
VOL UP/
CURSOR UP
VOL DOWN/
CURSOR DOWN
PROCEED

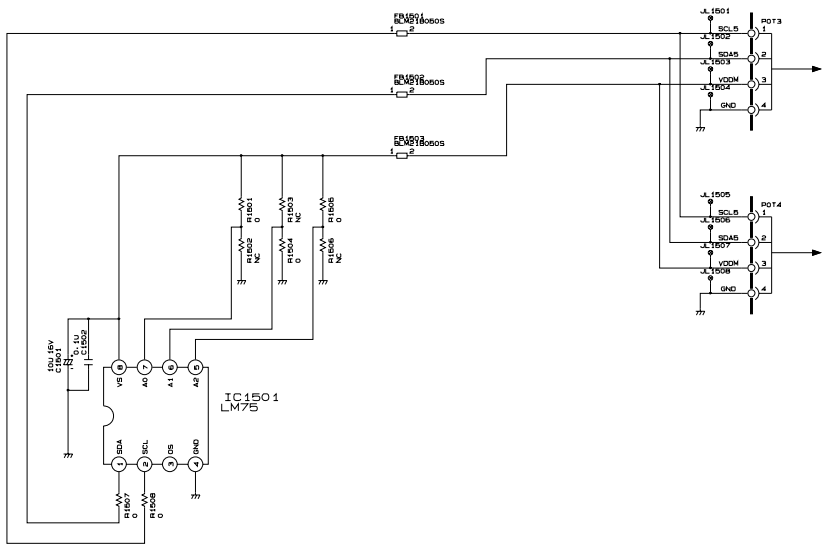

PW
POPW
SW7
POIN
GND
M+5V
M+7V
NC
TO MAIN PWB
JL2601
1SW7
JL2602
1POIN
JL2603
1D.GND
JL2604
1M+5V
JL2605
1M+7V
PT1
PT2
PT3
PT4
PT5
R2601
15K
S2601
ON
OFF
Q2601
FA1L4M
R2603
5.6K
R2602
2.2K
C2601
22U
16V
GND


M+5V
RV2101
SBX8035
TP2101
NC
R2101
100
Q2103
2SC2412K
REMARK
R2106
47
COM-3
JL2101
REMIN
REMIN1
PW1
LD
JL2102
POLED0
LEDCTL1
PW2
Q2101
2SC2412K
Q2104
2SA1037AK
JL2103
POLED1
LEDCTL2
PW3
R2102
4.7K
JL2104
GND
PW4
TO MAIN PWB
POLD
R2104
220
TP2102
NC
JL2105
M+5V
PW5
R2103
4.7K
C2101
47U
16V
C2102
0.1u
C2103
47U 16V
Q2102
2SC2412K
R2105
220
REMARK
D2101
SPR-39MVW


RM
PORM
JL2801
TO AUDIO PWB
ROUT
JL2802
GND
W2801
R OUT
LM
POLM
JL2803
GND
JL2804
LOUT
JL2805
GND
L OUT
TO AUDIO PWB


DVI(PC3)
M2401
JL2401
JL2402
JL2403
JL2404
JL2405
JL2406
JL2407
JL2408
JL2409
JL2410
JL2411
JL2412
JL2413
JL2414
JL2415
JL2416
JL2417
JL2425
JL2424
FB2401
BLM11A121S
FB2402
BLM11A121S
C2401
47U
16V
C2402
0.1U
25V
RX1+
RX1-
RX1 SHIELD
RXC SHIELD
RXC+
RXC-
GND
DDC+5VDC
RX2+
RX2-
RX2 SHIELD
RX0 SHIELD
RX0+
RX0-
SENS
DDC DATA
DDC CLOCK
POPL2
F1-TWE21P-VF
RX0 SHIELD
RX0-
RX0+
RX2-
RX2+
RX2 SHIELD
DDC CLOCK
DDC DATA
RX1-
RX1+
RX1 SHIELD
SENS
RXC SHIELD
RXC+
DDC+5VDC
RXC-
GND
PL
TO MAIN PWB


FB1401
BLM21B050S
FB1402
BLM21B050S
FB1403
BLM21B050S
JL1401
SCL5
JL1402
SDA5
JL1403
VDDM
JL1404
GND
POT1
JL1405
SCL5
JL1406
SDA5
JL1407
VDDM
JL1408
GND
POT2
R1401 NC
R1402 0
R1403 0
R1404 NC
R1405 NC
R1406 0
R1407 0
R1408 0
10U 16V
C1401
0.1U
C1402
IC1401
LM75
VS
A0
A1
A2
SDA
SCL
OS
GND


FB1504
BLM21B050S
FB1505
BLM21B050S
FB1503
BLM21B050S
JL1501
JL1502
JL1503
JL1504
SCL5
SDA5
VDDM
GND
POT3
JL1505
JL1506
JL1507
JL1508
POT4
R1501 0
R1502 NC
R1503 NC
R1504 0
R1505 0
R1506 NC
C1501 10U 16V
C1502 0.1U
IC1501
LM75
VS
A0
A1
A2
SDA
SCL
OS
GND
R1507 0
R1508 0