SERVICE MANUAL

17" HIGH - RESOLUTION
COLOR DISPLAY MONITOR
MODEL TFS6705

≡ VC-7

MITSUBISHI ELECTRIC CORPORATION

APR. 1992

1. SPECIFICATION

1.1 FEATURES

(1) HIGH RESOLUTION IMAGE

1280 x 1024 pixel resolution image in non-interlace mode comes out. Flicker free image is enabled by non-interlace operation.

(2) AUTO TRACKING FUNCTION

Input signals which have 30 KHz~64 KHz as horizontal scanning freq., and 50 Hz~130 Hz as vertical scanning freq. can be displayed correctly in the screen of this monitor by the auto tracking function without any adjustment.

Display image size and position of 4 different signal sources are memorized by user and that of 6 different signal sources are presetted at factory.

(3) EASY RE-ADJUSTMENT

Adjustment points of display image size and position are easily accessed through the front lid of the standard plastic cabinet, and push buttons.

(4) WIDE - BAND - VIDEO AMPLIFIER

Wide-band-analog video amplifier can display the fine-grained picture with unlimitted colour.

NOTE:

In case of horizontal freq. around 62 - 64 KHz and vertical refresh rate of 74 - 76 Hz, should be applied as resolution 1024 x 768.

1.2 RATING / SPECIFICATION

(1) AC Power Voltage: 90-132 and 180-264VAC
(2) AC Power Frequency: 50/60 Hz
(3) Power Consumption: 130 W (nominal)
(4) Input Signal
  (a) Video Signal: Analog RGB 0.7 Vp-p (typ) (Positive bright)
  (b) Sync Signal:
    Composite sync on Green video 0.3Vp-p (typ)
    Composite sync 1.5 Vp-p - 5.0 Vp-p (Negative)
    Separate sync 1.5 Vp-p - 5.0Vp-p
    (HD/ VD) (Negative / Positive)
(5) Interface
  (a) Video Signal: Shrink D-SUB 15p & 13W3 Connector
  (b) Input Impedance: 75ohm for video signal
    1Kohm for Sync. Signal
(6) Scanning Frequency:
    Horizontal 30KHz - 64KHz
    Vertical 50Hz - 130 Hz
(7) Warm Up Time: More than 30 minutes
(8) Effective Display Area: 300(W) x 225(H) mm
(9) Brightness: 100 nits (typ) with B22 phosphor
(10) Operater Controls:
    Power SW (Front panel)
    Degauss SW (Front panel)
    Contrast control (Front panel)
    Bright control (Front panel)
    Horizontal width control
    Horizontal position control
    Vertical height control
    Vertical position control
    H-static convergence control
    V-static convergence control
(11) Service Controls (Front lid):
    R, G, B Video gain controls
    PCC-AMP
    PCC-PHASE
    KEY-BALANCE
    PIN-BALANCE
    Horizontal width control
    Horizontal position control
    Vertical height control
    Vertical position control
    H-static convergence control
    V-static convergence control
(12) Video Amplifier:
    50Hz - 100 MHz±3dB
    Tr / Tf 6 nsec (typ)
(13) Retrace Time: Horizontal 4.0 μsec
  (Recommended) Vertical 600 μsec
(14) Linearity: 7 % (max)
(15) Raster Distortion: 2.0 % (max)
(16) Raster Size Regulation: 0.5 % (max)
(17) Misconvergence:
  * Center 0.35mm (max)
  (within 225 mm diameter circle)
  * Other Area 0.45mm (max)
(18) High Voltage: 27.0 KV (typ)
(19) Temperature: 0~40 ℃ (with standard cabinet)
(20) Outline Size: 410(W) x 406.5(H) x 440(D) mm (Incl. T/S)
(21) Weight: Approx. 22 kg (Incl. T/S)

2. CIRCUIT DESCRIPTION

2.1 GENERAL

This display monitor is composed of eight blocks as shown in BLOCK DIAGRM (Schematics).

(a) Power supply and deflection block(PCB-MAIN)
(b) Control block (PCB-CONTROL)
(c) Deflection block (PCB-DEFL-SUB)
(d) Video block (PCB-VIDEO)
(e) Sync block (PCB-SYNC-SUB)
(f) Power supply block (PCB-POWER-SUB)
(g) HV-REG block (PCB-HV-SUB)
(h) Distortion block (PCB-SINE)

Every blocks will be explained in detail in following chapters. In this chapter, the auto-tracking function will be explained generally.
Input sync signals whose horizontal scanning frequency of 30KHz-64KHz and vertical scanning frequency of 50Hz-130Hz can be automatically locked on without adjusting H-HOLD/V-HOLD. This automatic lock on function is performed by the circuits in PCB-CONTROL.

To maintain optimum operation of circuits over wide frequency range, some elements in circuits are switched according to horizontal frequency of input sync signal. The circuit in PCB-CONTROL judges the frequency of input sync signal, and generates changing signals.
PCB-CONTROL also maintains the other control signals to adjust picture sizes, positions, etc. electronically.

2.2 POWER SUPPLY BLOCK

2.2.1 GENERAL

(1) Dual input voltage 100~200 VAC and 220~240VAC (automatically) are supported.
(2) The output lines of this power supply are shown in Table 2-1 with their main loads.
(3) The power supply works as switced mode operation with RCC (Ringing Choke Converter) configuration. Output voltages are regulated by 3 of primary circuit feed back signal through photo coupler (IC902). The switching frequency is corresponding to load currents.
The 60V-140V line is regulated by the DC chopper method from168V line whose switching frequency is corresponding to H-Sync input.

OUTPUT LINE	MAIN LOAD
6.3 V	CRT Heater
24 V	H / V Deflection IC, H - Drive
27 V	V - Deflection
5 V	CPU
12 V	Video Circuit
80 V	Video Circuit
168 V	Video Circuit, HV Circuit
60~140 V	H - Deflection
- 12 V	DAC Pre-Amp. for S - PCC Circuit for B, G, B - Gain

Table 2-1

2.2.2 RECTIFY AND FILTER CIRCUIT

(1) The AC input voltage is rectified by the diode bridge D901.
The rectified voltage is filtered by charging C911 and C912.
(2) The thermistor RT901 & RT902 are equipped to suppress the inrush current when switch on.
A triac Q901 shunts RT901 to eliminate the power loss of RT901 when the control circuit starts to oscillate.

2.2.3 DEGAUSS CIRCUIT

(1) This monitor is provided the auto and manual degauss function.
(2) The auto-degauss circuit is operated as follows after started up the micro computer. The degauss signal from micro computer via 4 pin of connector J904, then it turns on Q951, and then RY901 operates degauss circuit during approx. 5 sec so that the degauss current could flow to the degauss coil via RP901.
(3) The manual degauss circuit works during approx. 5 sec which is controlled by the degauss signal from micro computer (when pushing the degauss switch (SW110)).
(4) A varistor RV901 works to keep approximately the same degauss current in both case of 220-240VAC and 100-120 VAC line input.

2.2.4 PRIMARY CIRCUIT

(1) Main DC power supply of this monitor consists of RCC (Ringing Choke Converter).

When the power switch is turned on, triggering current is fed through R906, R907, R908 and R909 to flow the collector current of Q1 in IC901 which is a main-switching transistor. An error amp. IC956 detects an output voltage and makes a feed back to primary circuit via photo-coupler IC902.

(2) When Q901 switch off, the energy which is stored in primary winding T901 transfers to secondary circuit. When all stored energy is discharged, the voltage of each coil is reversed and Q1 (main switch transistor in IC901) switches on. The base current of Q1 is supplied by the discharge of C916.

(3) Photo-coupler IC902 controls the reversed charge current of C918 and changes the turn on thresh time by which on time of Q1 is controlled.

(4) R915 is a resistor to detect over-current.

2.2.5 SECONDARY CIRCUIT

(1) In this paragraph chopper circuit which is applied for auto-scanning circuit will be explained.

(2) Chopper circuit mainly consists of L955, IC955 and Q952.
The output voltage +B is regulated by Q952 on PCB-MAIN in terms of PWM control to change the horizontal display size. The output from 12 pin of IC955 is pulse wave whose on-duty is followed by feed-back signal to pin 8 of IC955 from the emitter of Q520 in order to change +B.
The increase or decrease command of H-size comming from MPU goes to DAC on PCB-DEFL-SUB and then into pin 9 of IC955 as a H-size signal. A pin 9 of IC955 is connected to pin 8 of IC955 internally through PNP transistor like Fig. 1-1 so that a signal to pin 9 of IC955 could change feed-back signal from emitter of Q520 seemingly and change H-size finally.

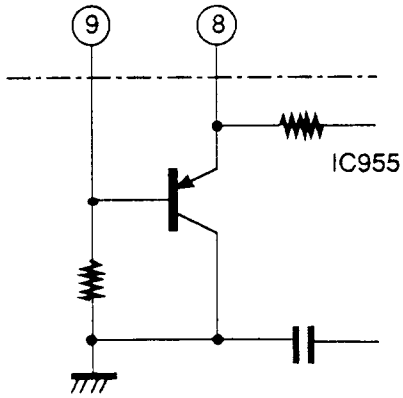


Fig. 1-1

2.3 CONTROL BLOCK

2.3.1 GENERAL

The CONTROL BLOCK is on PCB-CONTROL. Fig.2-1 shows the block diagram of PCB-CONTROL.

(1) PCB-CONTROL has one CPU IC101, one non-volatile memory IC102, and other control ICs.
The input signal for PCB control are fed from tact switches on PCB-CONTROL, horizontal and vertical sync signals, sync polality detecting signals from PCB-SYNC-SUB.
The FAN rotation detect signals are also provided to PCB-CONTROL.

(2) Based on above signals, IC101 reads out data like as screen size, screen position etc., which are stored in IC102, and stores into RAM on IC101. IC101 provides the horizontal deflection control signals like as AFC constant and Cs changing which are stored in ROM on IC101.
Each outputs of IC101 are as follows;

P00: For changing horizontal linearity control
P01,P02: For changing AFC time constant
P03～P06: For changing Cs compensate

(3) The D/A conversion data is sent from P70, P71 PORT and P30～P33 PORT of IC101 to IC452 (DAC on PCB-DEFL-SUB), IC304 (DAC on PCB-SYNC-SUB), IC302 (DAC on PCB-SYNC-SUB). The clock(P32,P71), serial data output (P31, 70) and load (P33,P30) strobe pin make up the three-wire interfaces. The DC voltages from IC452, IC304, IC302 are used to control screen size, position, brightness, etc.

(4) IC102 is EEPROM which are written control data like screen size, position, brightness, etc. IC103 is provided to reset at power on, program run away watching, and +5V power source voltage watching.

(5) SW101～110 on PCB-CONTROL are corresponding to each buttons on front panel as follows.

(6) IC107,108,109 on PCB-CONTROL are not used whose patterns are prepared just for future function.

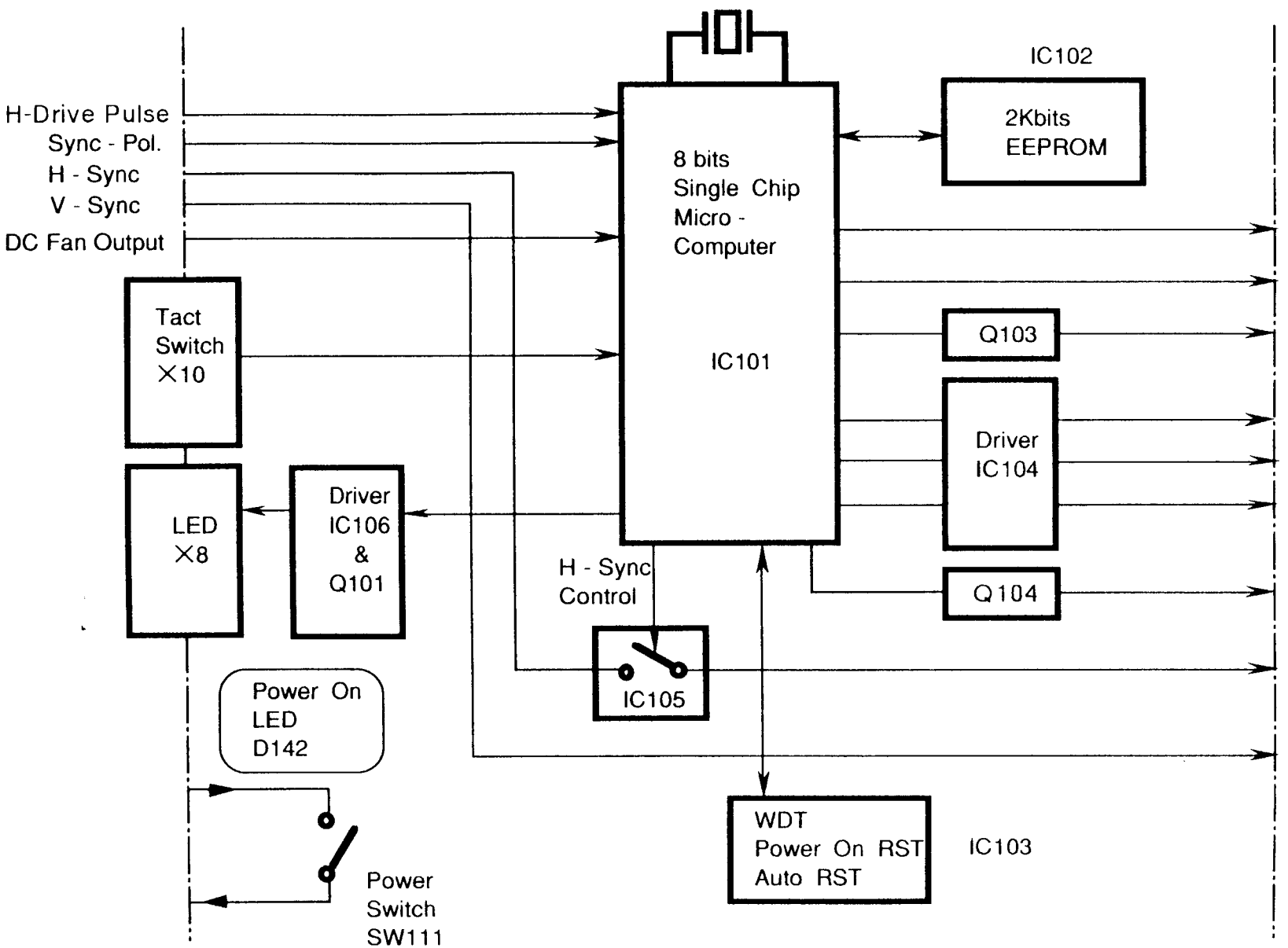
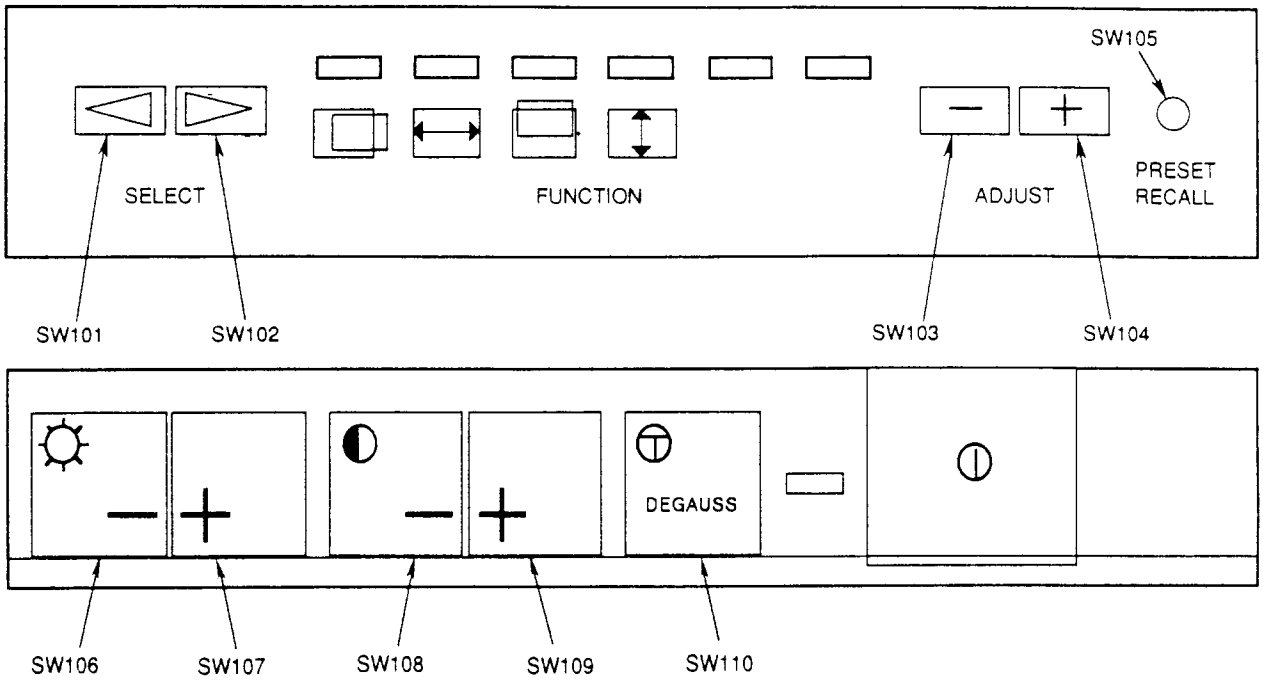


Fig. 2-1 Control Block



2.3.2 CONTROL FUNCTION

(1) Maximum timing number: 12 timings
(6 timings: for preset, 4 timings: for user, 2 timings: reserved)
There are 6 timings preset at factory which are shown in Fig. 2-2. And there are 4 additional timings available for user.

(2) To detect a timing, one of following conditions are necessary at least.
※ | fH' - fH | > 3 KHz
(internal check uses 2 KHz in program)
※ | fv' - fv | > 5 Hz
(internal check uses 4 Hz in program)
※ different polarity of H-SYNC
※ different polarity of V-SYNC

(3) In following cases, the output of H-SYNC signal in chassis are set off to protect deflection circuit.
(a) Out of horizontal frequency range from 28.3KHz ±1 KHz~66 KHz±1KHz and / or out of vertical frequency range 45Hz±2Hz ~135Hz±2Hz.
(b) No H or V sync signal.
(c) Unstable sync signal that Δ f v exceeds 4Hz and / or Δ f H exceeds 1.5KHz often.

(4) Each 12 timings has one common data for R, G, B- BIAS and GAIN, DBF-H, DBF-V, CONTRAST, BRIGHT.

(5) Select buttons function
(a) Operation mode ----- shift to right / left
(b) Service mode ------ change lit-on pattern followed by adjustment items of Fig. 2-3
(c) Factory mode -------- ditto

(6) When +/- buttons of bright are pushed at the same time, the brightness becomes a middle level of brightness set at factory.

(7) RECALL FUNCTION
When pushing the recall button on front panel in case of operate mode and service mode, the all factory adjustment items as shown in Fig. 2-3 that may have been overwritten by the user are restored.

(8) FAN WATCHING
When the revolutions per minute of FAN becomes less than 1006 rpm (normally 3300 rpm), the monitor stops to operate in order to protect the electrical components inside. So a pin 10 of J102 becomes high and enables Q953 to shunt.
Then the current limitter of IC901 works.

2.3.3 Adjustment Mode

There are 3 adjustment modes in this monitor.
(a) Operate mode
(b) Service mode
(c) Factory mode

(a) Operate mode
The operate mode is opened for the general end user operation and is available to adjust the raster size, position, brightness and contrast by the adjustment buttons on the front panel.

The adjusted picture conditions are automatically memorized into EEPROM (During pushing the adjust button, picure conditions change in terms that datas on CPU RAM and DAC output datas are changed. All CPU RAM datas are written into EEPROM just after the adjust button is released.).

(b) Service mode

The service mode has additional following items from the operate mode.

(1) R,G,B-GAIN
(2) PCC-AMP,PHASE
(3) KEY BALANCE
(4) PIN BALANCE

The meanings of above (2), (3), (4) are as follows.

To enable Service mode, perform the following.

1) Power off the monitor.
2) Push and hold both the plus (+) and minus (-) adjustment buttons while switching the monitor power on.
   After the power is on, release both buttons.
3) The adjustment function indicators blink for approximately 10 seconds.
   During this time, push and release both the (+) and (-) buttons one more time. When the indicators stop blinking, they should indicate the V-SIZE function as shown in Fig.2-3.

NOTE:

If the adjustment function indicators do not blink, or if both adjustment buttons were not pushed while the indicators were blinking, or if some other button was pushed, or the indicators do not show the display service status, the service mode is not enabled. In this case, repeat steps 1) through 3).

4) Use the Adjustment Function Select Buttons to select the desired Adjustment Function Indicator Code as shown in Figure 2-3.
5) Use the Adjustment Control Buttons to perform the adjustments as required for optimum raster geometry or R, G, B-Gains.
6) All adjustments are automatically memorized. To exit the service mode, turn off the monitor.

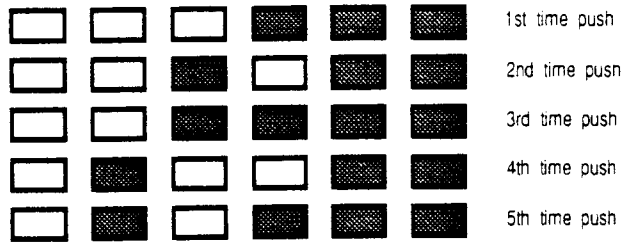
(c) Factory mode

The factory mode has some additional items from service mode, which are different adjust - ment items by the way to enable factory mode.

To enable factory mode by front panel

(c*-1) Power on while pushing and holding both + button of contrast and - button of brightness.
(c*-2) Both contrast LED and bright LED blink for approximately 10 seconds.
(c*-3) ITEM LED is lit on as follows.

(c*-4) Push select button 5 times

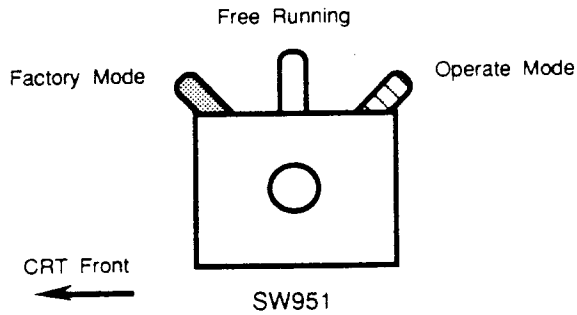


Indication of LED

(c*-5) Push both + and - buttons of adjust at the same time.
(c*-6) Use the Adjustment Control Buttons to perform the adjustments as required for .
(c*-7) To release factory mode, turn off the monitor.

To enable factory mode by switch inside the cabinet.

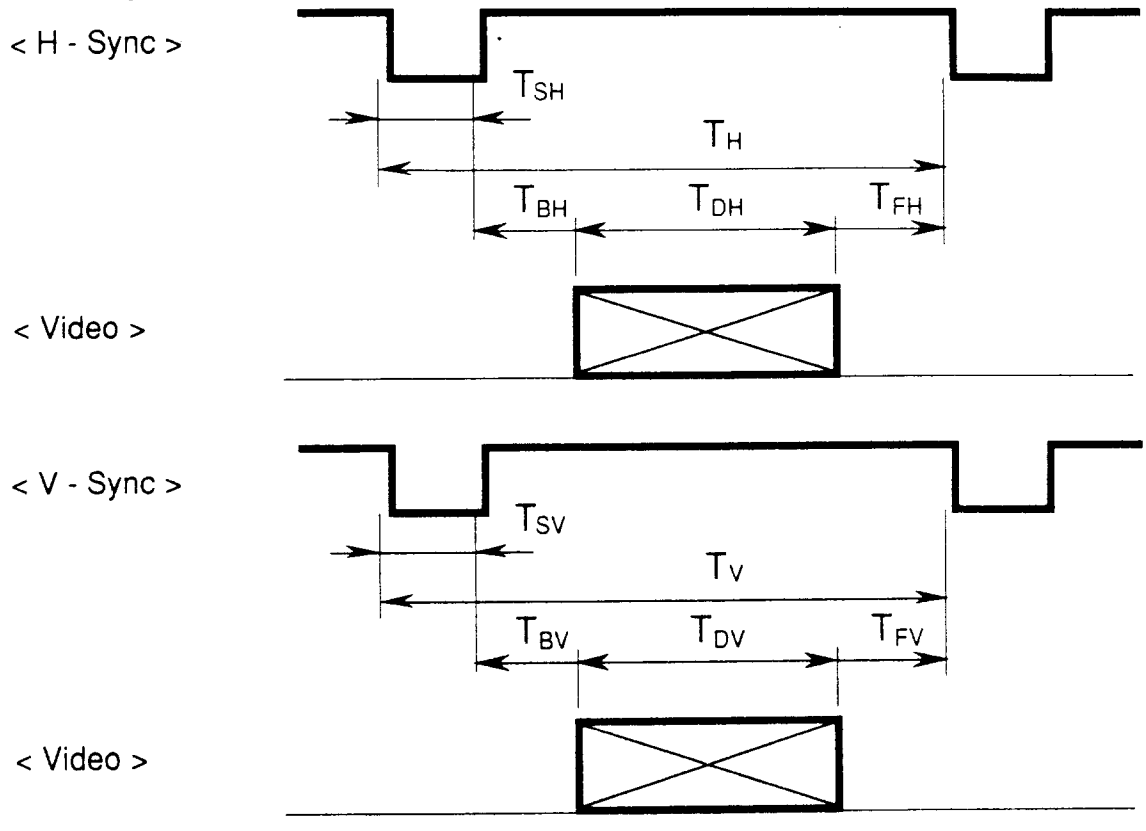
(c**-1) Power off.
(c**-2) Power on after setting SW951 to the factory mode side as shown below.



SW951

Adjusted Items additional to items of service mode
the way of (c*) ------ R, G, B-BIAS by the way of (c*)
the way of (c**) ----- DBF-H, DBF-V, R, G, B-BIAS

Fig. 2-2 Preset Timing Datas at Factory



	IBM PS / 2			APPLE MAC II	f_H = 48.36KHz f_V = 60.00Hz	f_H = 56.48KHz f_V = 70.07Hz
	640×480	640×400	640×350			
T_H	31.778	←	←	28.570	20.676	17.710
T_{SH}	3.813	←	←	2.120	2.092	1.810
T_{FH}	0.636	←	←	2.120	0.360	0.330
T_{BH}	1.907	←	←	3.170	2.462	1.920
T_{DH}	25.422	←	←	21.160	15.754	13.650
T_V	16.683	14.268	←	15.000	16.667	14.272
T_{SV}	0.064	←	←	0.086	0.124	0.106
T_{FV}	0.318	←	1.176	0.084	0.063	0.094
T_{BV}	1.048	1.112	1.906	1.114	0.600	0.513
T_{DV}	15.253	12.711	11.122	13.714	15.880	13.599
H - Sync	−	−	+	Comp. Sync	−	−
V - Sync	−	+	−	Comp. Sync	−	−

Fig. 2-3 Indication Table for LED

Indication of LED	ITEM	Service Mode	Factory Mode(1)	Factory Mode(2)
	V-STAT	○	○	○
	H-STAT	○	○	○
	V-SIZE	○	○	○
	V-POSI	○	○	○
	H-SIZE	○	○	○
	H-Phase	○	○	○
	Not Used	○	○	○
	PCC-Amp	○	○	○
	PCC-Phase	○	○	○
	Key Balance	○	○	○
	Pin Balance	○	○	○
	G-Gain	○	○	○
	B-Gain	○	○	○
	R-Gain	○	○	○
	G-Bias		○	○
	B-Bias		○	○
	R-Bias		○	○
	DBF-V			○
	DBF-H			○

2.4 DEFLECTION BLOCK

Deflection block consists of horizontal, vertical, high voltage circuits, and horizontal and vertical deflections are fundamentaly operated by changing DC control voltages.

2.4.1 HORIZONTAL DEFLECTION CIRCUIT

(1) All DC control voltage are fed from PCB-DEFL-SUB.
Positive H-sync signal is fed from PCB-SYNC-SUB and DC voltage in accordance with that frequency is given in pin 5 of J5A5 on PCB-MAIN to oscillate horizontal frequency.
If H-oscilation frequency is high, relative DC voltage of 5 pin of J5A5 is higher, then the charge current to add to time constant circuit consisting of R504 and C506 increase to shorten charge time. So the oscillation frequency goes to higher.
When no sync signal is connected, free running frequency is about 47KHz.

(2) The output of 26 pin of IC501 on PCB-MAIN works as a drive voltage for H-deflection, and High Voltage circuits.
The principle of horizontal deflection is shown in Fig. 2-4. Q591 works as a horizontal output, and D508, D509 and D510 work as dumper diodes. Q511, Q512, Q513, Q514 and Q510 are switched on as follows in accordance with the horizontal frequency to compensate the horizontal linearity.

~33.5KHz	Q511~Q513 are on.
33.5~37.1KHz	Q512 and Q513 are on.
37.1~40.5KHz	Q512 and Q514 are on.
40.5~44.0KHz	Q513 and Q514 are on.
44.0~49.3KHz	Q513 is on.
54.5~61.5KHz	Q514 is on.
61.5KHz~	All is off.

(3) In Fig.2-4, the horizontal output Tr Q591 is turned on by the drive pulse from IC501 via Q506 and Q508. During Q591 is turned on, the deflection current IDY increase from 0 to positive max Ip in accordance with the equation as follows.

$Ip = (VDY \times Ton) / LDY.$

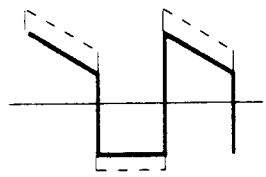
*(LDY : parallel value of HOT and DY)

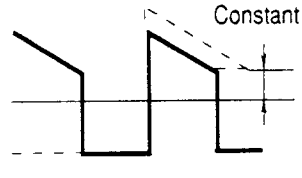
When the drive pulse goes to negative polarity, Q591 is turned off, and IDY begins to flow to charge C519 and C520 until Vcp reaches maximum value " $\pi / 2 \times (Ts / Tr) \times Vcc$ ".

(4) The source voltage of Q501 is varied from approx. 60V to 140V to regulate the horizontal width regardless of horizontal frequency.
This is performed to maintain the DC voltage of the cathode of D518 which is proportional to collector pulse voltage of Q591.
The DC voltage across C533 is fed to 8 pin of IC955. If DC voltage across C533 is higher, +B voltage of Drain of Q952 becomes lower in procedure stated in 2.2.5 (2).

(5) Q502~Q505 consist of regulator to optimize the driving condition of H-deflection output Tr Q591.
The output voltage of Q504 is controlled by 2 modes.
(5-1) If the H-WIDTH control voltage from 9 pin of J5A5 on PCB-MAIN decreases (Horizontal width increases), then output voltage of Q504 increases to supply enough driving power for Q591.
Refer to Fig. 2-5.
(5-2) On the other hand, when the 1 pin voltage of J5A4 on PCB-MAIN decreases according to the lower horizontal frequency, the base voltage of Q502 also decreases, so the output voltage of Q504 increases to optimize the base current of Q591. Refer to Fig. 2-7.
By the manner stated (5-1), (5-2), Q591 is driven enough, and power loss is minimized.

Base Current of Q591





Collector Current of Q591

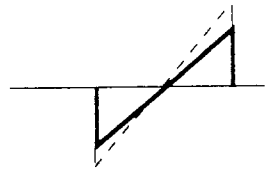


Fig. 2-5

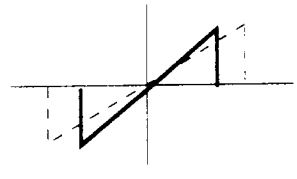


Fig. 2-6

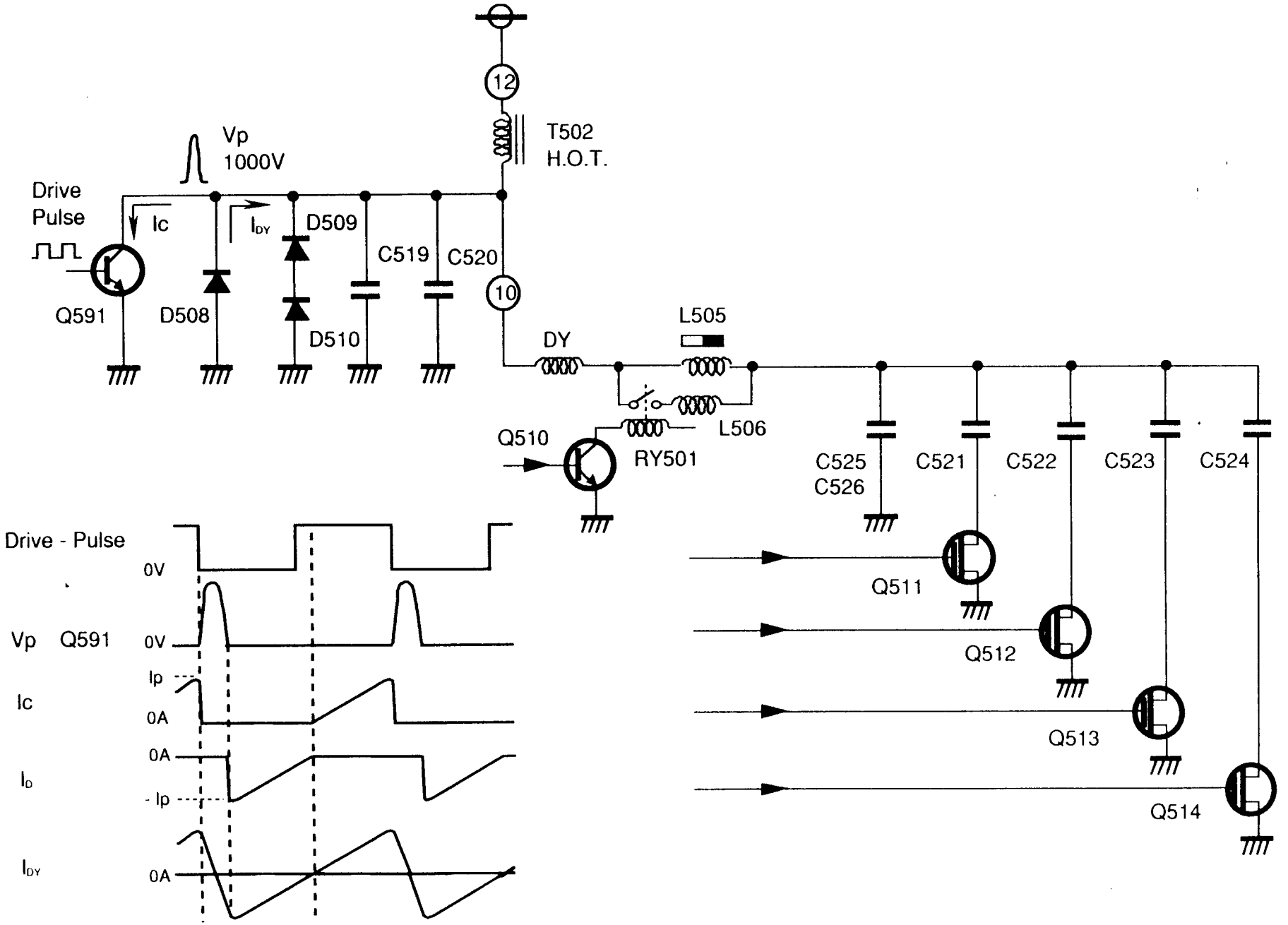


Fig. 2-4 Priciple of Horizontal Deflection

(6) The 6 and 7 pin of J502 on PCB-MAIN are control signals to change AFC components R506~R509. The combination of these are as follows.

~40.5KHz	C545/R508
40.5~49.3KHz	C549/R507
49.3~59.7KHz	C543/R506
59.7KHz~	C546/R509

(7) In case of more than 44.0KHz, RY501 is on to add L506 in parallel with L505 to keep good H-linearity condition on the screen.

2.4.2 HIGH VOLTAGE CIRCUIT

(1) HIGH VOLT. SUPPLY & CONTROL CIRCUIT

The drive pulse, which is the same frequency as the horizontal deflection, is connected to the base of Q603 via the emitter follower Q601 and Q602. The flyback transformer steps up collector pulse generated by Q603 to the high voltage when Q603 turned off. The maximum Vcp of Q603, which depends on the horizontal frequency normally, is kept the same value independent on horizontal frequency by T601 (1/2) and D605 in spite of the fixed +B and resonance capacitor. During Q603 is on, C608 is changed to reversed +B voltage. Because the impedance between 10 and 9 pin of T601 (1/2) and between 6 and 8 pin of T601 (1/2) are the same. When Q603 turns off, the current through the coil between 6 and 8 pin of T601 (1/2) starts to charge into C608 oppositely until collector pulse of Q603 becomes 2 times as +B voltage and D605 goes to on. To get enough collector pulse for this operation, Q605 turns off at more than 38.8KHz of horizontal frequency to change capacity of resonance capacitor. The high voltage should be stabilized by T601 (2/2) which is controlled by Q607 (shunt regulator) and Q801. The proportional high voltage is fed to pin R of Q607. If the high voltage increases, the output voltage of pin K of Q607 decreases. The DC level of pulse made by a coil between pin 2 and pin 3 of T601 (1/2) decreases. It raises up the threshhold level of gate voltage of Q801 relatively. It makes the high voltage decrease to the correct value. If the high voltage decreases, stabilized circuit works opposite direction of increase as above mentioned. The high voltage is set to 27.0KV by VR601 at factory.

(2) HIGH VOLTAGE SAFETY CIRCUIT

Safety circuits described below are equipped to prevent abnormal increase of the high voltage that may cause a X-radiation of harmful level. No modification should be applied to the high voltage supply and safety circuits.

The safety circuit works as the over voltage protector for a high voltage. Excessive high voltage is detected by R610 which is fed to Hold-Down circuit. The voltage across the capacitor C612 which is proportional to the high voltage is fed to Hold-Down circuit through R611, VR602 and R612. When high voltage reaches 29.0KV, the voltage across D806 is over 6.0V and then IC801 goes to turn on, and Drain of Q611 is connected to the secondary ground via Q606. When this happens, horizontal oscillation signal can no longer drive Q601, Q602 and Q603, so high voltage goes down. Once Hold-Down circuit operates, hold-down status is held till power is off. Additionally, in case of T601 generates too high voltage across C803, D807 becomes on to enable high voltage protection circuit.

2.4.3 VERTICAL DEFLECTION CIRCUIT

The vertical deflection is performed by one IC and some attached components. The oscillating frequency is fixed by R406 and C406.

The vertical size is controlled by changing the output current from 9 pin of IC501. The vertical linearity is adjusted by changing charge current into C404 and C405. IC450 (analog switch) on the PCB-DEFL-SUB can achieve this.

2.4.4 SIDE DISTORTION CORRECTION

The deflection current is modulated to parabolic and sinuous waveform by Q501 and T502 on the PCB-MAIN to compensate the side pincushion distortion. The gate of Q501 is controlled by PWM method from a signal of 8 pin of J5A5 on the PCB-MAIN leading to 8 pin of J7A2 on the PCB-DEFL-SUB which is the pulse output from Q718 and Q719 on the PCB-DEFL-SUB. This pulse is generated as follows. The signals to correct the sea gull shape distortion comming from 9 pin of J7V1 (sine wave), to corrct the Side-PCC distortion comming from 3 pin of IC708(parabolic wave) and PCC-Phase distortion comming from 2 pin of IC708 (V-saw wave) are combined at 5 pin of IC707 and amplified.

This output signal is compared with H-saw signal at 5 pin and 6 pin of IC703 in order to generate pulse signals whose width is varied according to the distortion corrections. The H-saw signal is

made by charging current into C730 and synchronized by trigger from 7 pin of J7A2 to Q725. The voltage (p-p) of H-saw wave is kept approx. 6V by feed-back into 5 pin of IC704 via D721.

2.4.5 DYNAMIC BEAM FOCUS

In order to get best focus condition on the entire screen, the dynamic modulated focus voltage is supplied to FOCUS (D) connector in addition to static focus voltage. This modulated voltage is comming from 1 pin of J706 after amplification by Q731 and Q714. The modulated signal is combined with horizontal and vertical parabolic waves at R7J1 and R7J2. The source of these parabolic waves are outputs of 18 pin and 11 pin of IC705.

2.4.6 H & V STATIC CONVERGENCE

1pin (RCV) of J702 is the output voltage to change horizontal static convergence, which depends on the output from 18 pin of IC452 (DAC) operated by the front button. A pin (V-STATIC) of J701 is the output current to change the vertical static convergence, which depends on VR701 (V-STA-ADJ) adjusted at the factory and output from 17 pin of IC452.

2.5 VIDEO BLOCK

2.5.1 VIDEO AMPLIFIER

(1) The circuits of video amplifier are in PCB-VIDEO.

(2) There are three video amps for RGB inputs which have identical circuit configulation. For simplification, the green-channel amp. will be explained in this chapter.

(3) This amplifier is composed of the pre-amplifier section and the main-amplifier section. The video signal (0.7Vp-p STD) is amplified to approx. 2 V p-p in the pre-amplifier section and is amplified again to approx. 35 Vp-p during the main-amplifier section.

(4) The input signal is fed to 22 pin of IC201 via C2G0. The gain of IC201 is controlled by the DC voltage of 21 pin. The higher voltage of 4 pin makes the gain of IC201 larger. This IC also provides the function of the black level clamp. The clamp pulse which is added at the back-porch duration of video signal is fed to 15 pin. The voltage level of 14 pin is fixed, which is a control of brightness for RGB signal.

(5) The output signal of IC201 is connected to the main-amplifier (IC203) via emitter follower Q2G0.

(6) The main-amplifier (IC203) is composed of the amplifier and the push-pull emitter follower. The amplifier circuit composed of IC203 is the complimentary push-pull circuit which has an infinite open loop gain.

(7) To display a pure white image on screen, both the DC level and the amplitude of video output signal should be adjusted as the 3 guns character -istics of CRT's are not identical. The DC level of cathod can be adjusted by the DAC of IC202, pin 11 (R-BIAS), pin 4 (G-BIAS) and pin 18 (B-BIAS).

2.5.2 SYNC SEPARATION CIRCUIT

(1) This monitor can be synchronized under following conditions.
  (a) Composite sync signal on green video
  (b) Composite sync signal (negative going)
  (c) Horizontal sync./ vertical sync signals (positive or negative going)

(2) The sync separation circuit provides following functions.
  (a) Seperating the composite sync signal from the green video signal
  (b) Amplifing the composite sync signal level to TTL level
  (c) Separating the horizontal and vertical sync signal from the composite sync signal

(3) This sync separation circuit is controlled by IC301 on PCB-SYNC-SUB. The horizontal sync signal is input to 6 pin of IC301. And the output of horizontal sync is fed from 14pin of IC301 to 6 pin of IC101 on PCB-CONTROL. Vertical sync signal is input to 8 pin of IC301. And the output of vertical sync is fed from 13 pin of IC301 to 17 pin of IC101 on PCB-CONTROL. Clamp pulse is fed from 17 pin of IC301 to 15 pin of IC201 on PCB-VIDEO. IC301 is located on PCB-SYNC-SUB.

2.5.3 ABL CIRCUIT

(1) This circuit is for limiting the beam current of CRT, and is in PCB-SYNC-SUB.

(2) The brightness of CRT is determined by the beam current. The beam current is detected by R810 (PCB-HV-SUB). When the beam current exceeds the limit value (approx. 600 μA), the voltage across R334 causes Q301 turn on, the voltage of 16 pin of IC201 on PCB-VIDEO which controls the gain of pre-amplifier, goes down to lower level.
It means that the circuit suppresses the output of pre-amplifiers for limiting the brightness of CRT.

(3) When the voltage across R810 drops until Q301 turn on and Q302 is supplied its base current and then the collector voltage of Q302 decreases. As the result, the gain control voltage of pre-

(b) PCB-DEFL-SUB:
VR550 (F_H-BIAS), VR551 (F_H-GAIN),
VR701 (V-STATIC)
(c) VIDEO UNIT: VR701 (H-STATIC)

3.2.3 +B ADJUSTMENT

(1) Connect a voltmeter to TP+B on PCB-MAIN.
(2) Adjust VR951 on PCB-MAIN to get 168V±0.3V.

3.2.4 HIGH VOLTAGE ADJUSTMENT

Adjust high voltage to 27.0KV±0.3KV by VR601 (HV-ADJ) on PCB-MAIN.

3.2.5 H-DRIVE ADJUSTMENT

(1) Input MAC-II timing signal as shown in Fig.2-2.
(2) Select the indication of H-SIZE pattern of LED by select button in the front panel.
(3) Adjust the horizontal raster size to get a max. width by adjust button in the front panel.
(4) Input 64KHz timing signal as shown in Fig.2-2.
(5) Adjust the horizontal width to 300mm±4mm by VR504 (H-SIZE) on the PCB-MAIN.
(6) Connect a digital voltmeter to TP-H-DRIVE on the PCB-MAIN.
(7) Adjust VR501 to get a minimum indication.

3.3 INTERNAL ADJUSTMENT

3.3.1 H-FREE RUNNING FREQUENCY ADJUST.

(1) Grasp red lead wire from PCB-MAIN to horizontal deflection yoke by frequency counter probe.
(2) Set SW951 on PCB-POWER-SUB at center position to have free running condition.
(3) Input sync. signal whose frequency is 40 KHz, then adjust VR550 (fH bias) on PCB-DEFL-SUB to oscillate free-running frequency at 40 KHz ± 0.2KHz.
(4) Input sync. signal whose frequency is 64 KHz, then adjust VR551 on PCB-DEFL-SUB to oscilate free-running frequency at 64KHz± 0.2KHz.
(5) Repeat (3) and (4).

3.3.2 +B ADJUSTMENT

(1) Input only sync signal of horizontal frequency 31.5KHz.
(2) Turn VR951 until TP+B reaches 168±0.3V.

3.3.3 HIGH VOLTAGE ADJUSTMENT

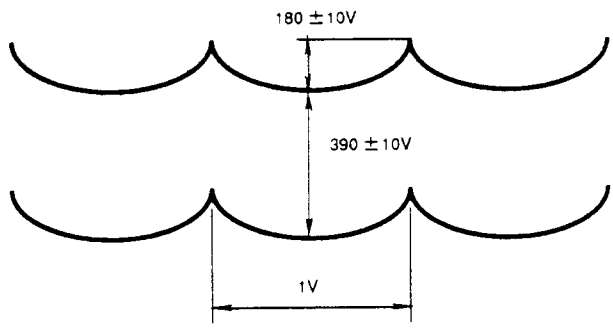
(1) Input only sync signal. (fH = 31.5KHz)
(2) Connect HV meter between anode of CRT and chassis (ground).
(3) Turn the screen potentiometer of FBT to fully CCW.
(4) Turn the HV-ADJ (VR601) to CW until HV-meter indicates 30.0KV ±0.3 KV.
(5) Turn the HV-LIMIT (VR602) until HV-LIMIT circuit works. (confirm 0(zero) V of high voltage.)
(6) Turn off the power SW, and turn the HV-ADJ (VR601) to CCW.
(7) Turn on the power SW, and turn HV-ADJ (VR601) slowly to CW to check HV-LIMITER works at 30.0KV±0.3 KV. Turn off power SW, and turn HV-ADJ (VR601) to CCW.
(8) Fix VR602 with glue.
(9) Turn on the power SW, and set HV-ADJ (VR601) to 27.0 KV±0.2 KV.
(10) Check if HV-LIMITER does not work after SW off and on.
(11) Fix VR601 with glue.

*CAUTION

HV-ADJ (VR601) and HV-LIMIT (VR602) are sealed and no field serviceable parts to avoid exposure of X-ray. Please contact to qualified personnel of MITSUBISHI, if need to re-adjust.

3.3.4 SUB-FOCUS ADJUSTMENT

(1) Input sync signal of fH = 57KHz and fV =70Hz.
(2) Connect a probe of the osciloscope to pin 1 of J706 on PCB-DEFL-SUB.
(3) Select DBF-H pattern of LED on front panel.
(4) Use adjust button on front panel to get 390V± 10V amplitude of horizontal parabolic wave.
(5) Select DBF-V patten of LED on front panel.
(6) Use adjust button on front panel to get 180V± 10V amplitude of vertical parabolic wave.

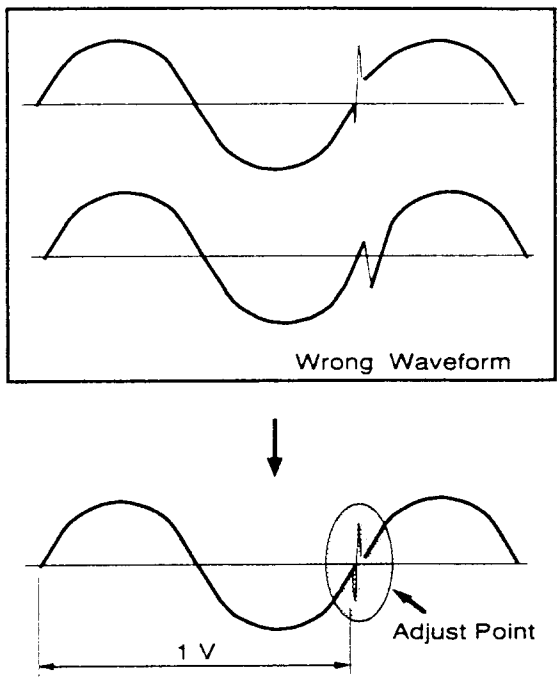


3.3.5 PCC DISTORTION SINE WAVE ADJUST.

(1) Input 56KHz timing signal as shown in Fig. 2-2.

(2) Connect a probe of the oscilloscope to TP-SINE on the PCB-SINE.

(3) Adjust VR7V1 on the PCB-SINE to have following waveform.



3.3.6 SWITCH SET

Set SW951 on the PCB-POWER-SUB to the factory mode position as stated in chapter 2.3.3.

3.3.7 SCREEN IMAGE ADJUSTMENT

All screen images should be adjusted with the 6 timing datas in Fig. 2-2 at factory mode.

3.3.8 HORIZONTAL RASTER POSITION

(1) Turn VR503 (G1-ADJ) on PCB-MAIN until dim back-rater appears.

(2) Set SW501 & VR502 to get raster position nearly at the center of CRT.

3.3.9 CRT CUT-OFF ADJUSTMENT (fH = 57KHz)

(1) Input only sync signal (fH = 57KHz).

(2) Set contrast to maximum position by contrast buttons on front panel.

(3) Push + button of bright to get a max. brightness.

(4) Set R, G, B-Bias to minimum position (- button of bright) after selecting R, G, B-Bias pattern by select button in the front panel.

(5) Turn the SCREEN VR on FBT to get a dim raster.

(6) Adjust 2 bias control except 1 bias control potentiometer which is the brightest at adjustment (5) item, to get a white raster.

(7) Set the VR503 (G1-ADJ) to get a dim raster (about 0.4 nit).

3.3.10 BRIGHTNESS & WHITE BALANCE ADJUSTMENT (fH = 57KHz)

(1) Set contrast control to maximum position by contrast button on the front panel (LED blinks).

(2) Set brightness control to maximum position by brightness button on the front panel (LED blinks).

(3) Input green video signal whose size is about 80x80 mm square at CRT center position.

(4) Adjust G-Gain to 73 nits.

(5) Input R, B video signal together with G, then adjust only R-gain, B-gain controls to get color coordination X=0.283±0.02, Y=0.297±0.02.

(6) Make sure that brightness is more than 100 nits at the full white pattern.

3.3.11 FOCUS ADJUSTMENT

(1) Receive white ASII (H) characters pattern on the entire screen.

(2) Adjust the FOCUS and DFOCUS VR on FBT to get best focus on the entire screen.

(3) After adjustment, the marking paint should be used to mark the final condition.

3.3.12 CONVERGENCE ADJUSTMENT

(1) Receive a cross hatch test pattern.

(2) Select the indication of V-STAT as shown Fig. 2-3 by select button in the front panel.

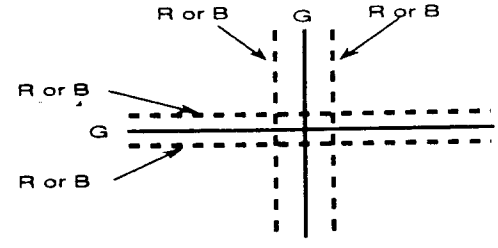
(3) Push the both "+" and "-" buttons in the front panel at the same time to get center position of vertical convergence.

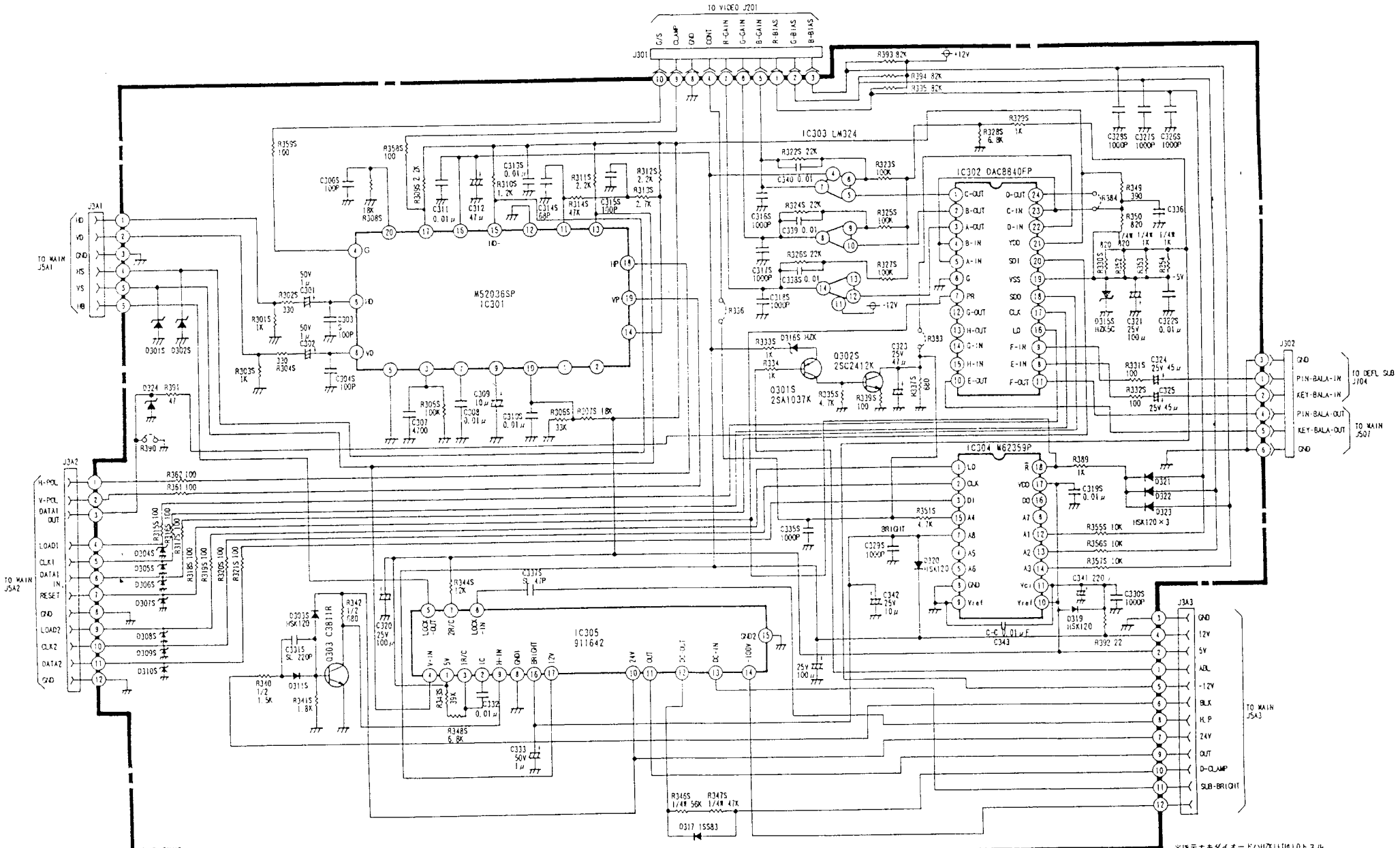
(4) Adjust VR701 on the PCB-DEFL-SUB to make both horizontal red and blue lines the closest to horizontal green line on the center of screen.

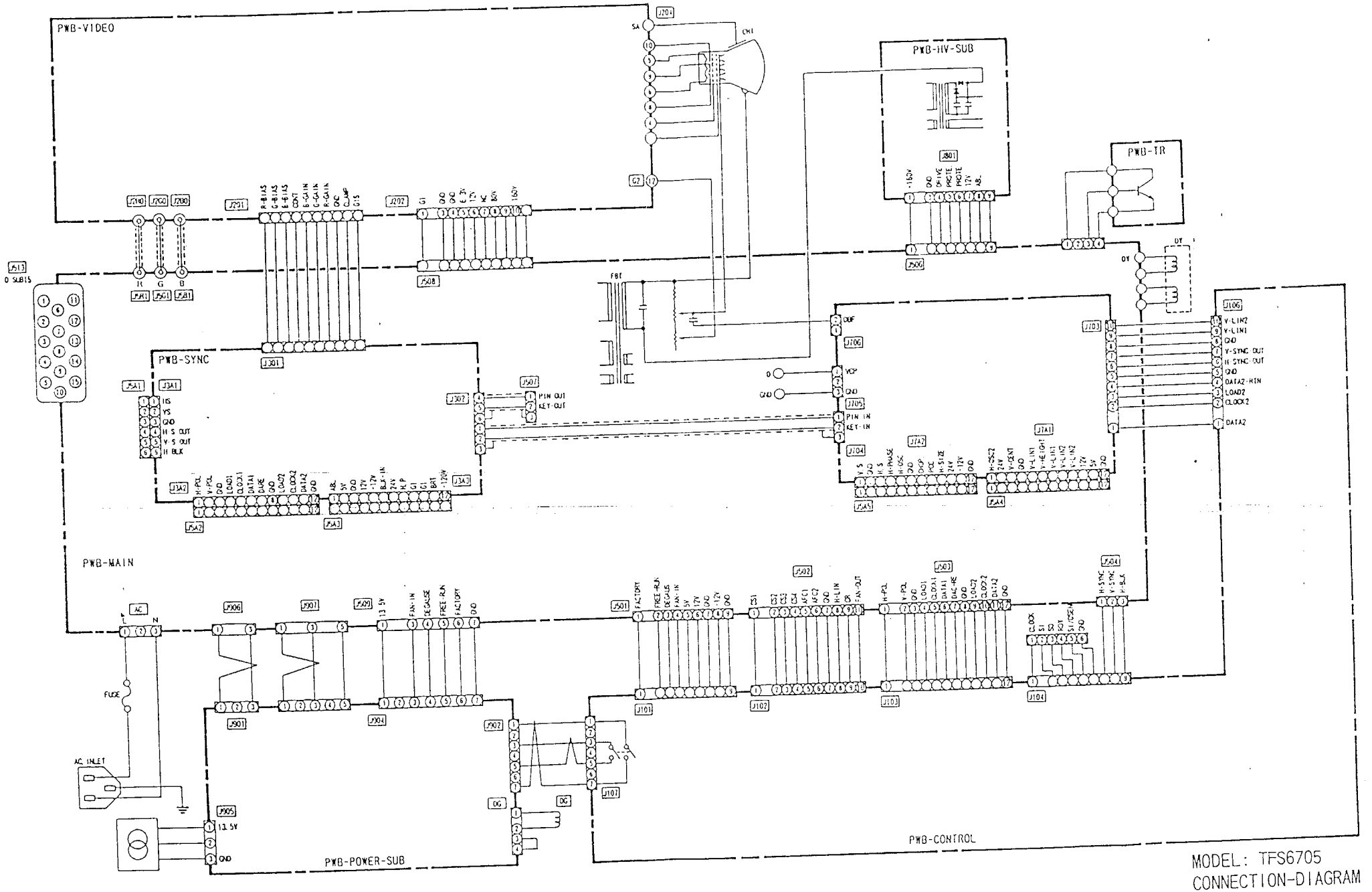
(5) Select the indication of H-STAT as shown Fig. 2-3 by select button in the front panel.

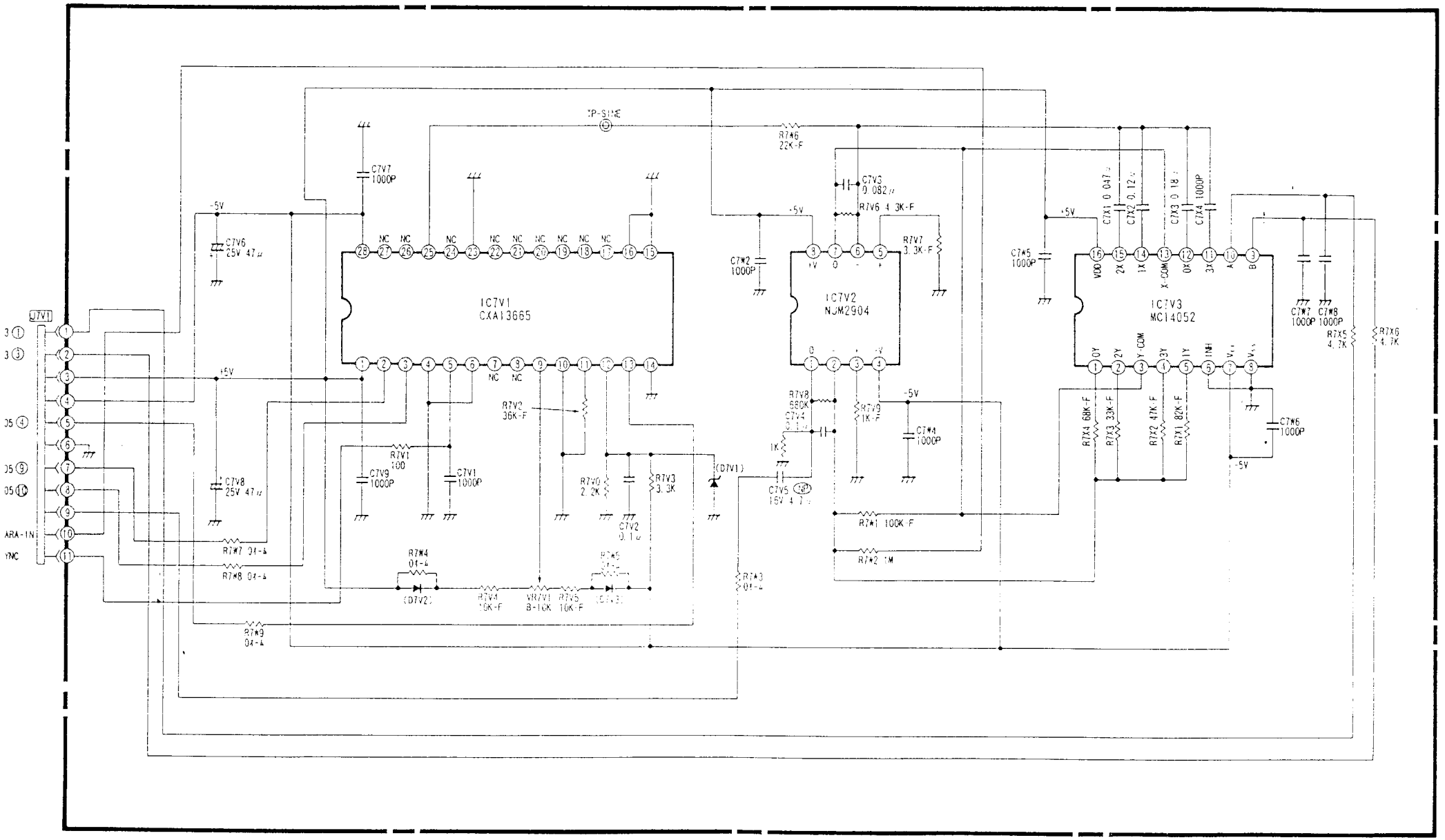
(6) Push the both "+" and "-" buttons in the front panel at the same time to get center position of horizontal convergence.

(7) Adjust RCVH-VR (H-STAT) on the radiator of VIDEO-UNIT to make both vertical red or blue lines the closest to vertical green line.




TO VIDEO J201
J301
G/S
CLAMP
GND
CONT
R-GAIN
G-GAIN
B-GAIN
R-BIAS
G-BIAS
B-BIAS
IC303 LM324
IC302 DAC8840FP
M52036SP
IC301
IC304 M62359P
IC305
911642
Q302S
2SC2412K
Q301S
2SA1037K
J3A1
J3A2
J3A3
J302
TO MAIN J5A1
TO MAIN J5A2
TO MAIN J5A3
TO DEFL SUB J104
TO MAIN J507
PWB-SYNC
MODEL:TFS6705K
PCB-SYNC-SUB
SCHEMATIC DIAGRAM


PWB-VIDEO
PWB-HV-SUB
PWB-TR
PWB-SYNC
PWB-MAIN
PWB-POWER-SUB
PWB-CONTROL
D SUB15
FBT
CRT
AC INLET
FUSE
MODEL: TFS6705
CONNECTION-DIAGRAM



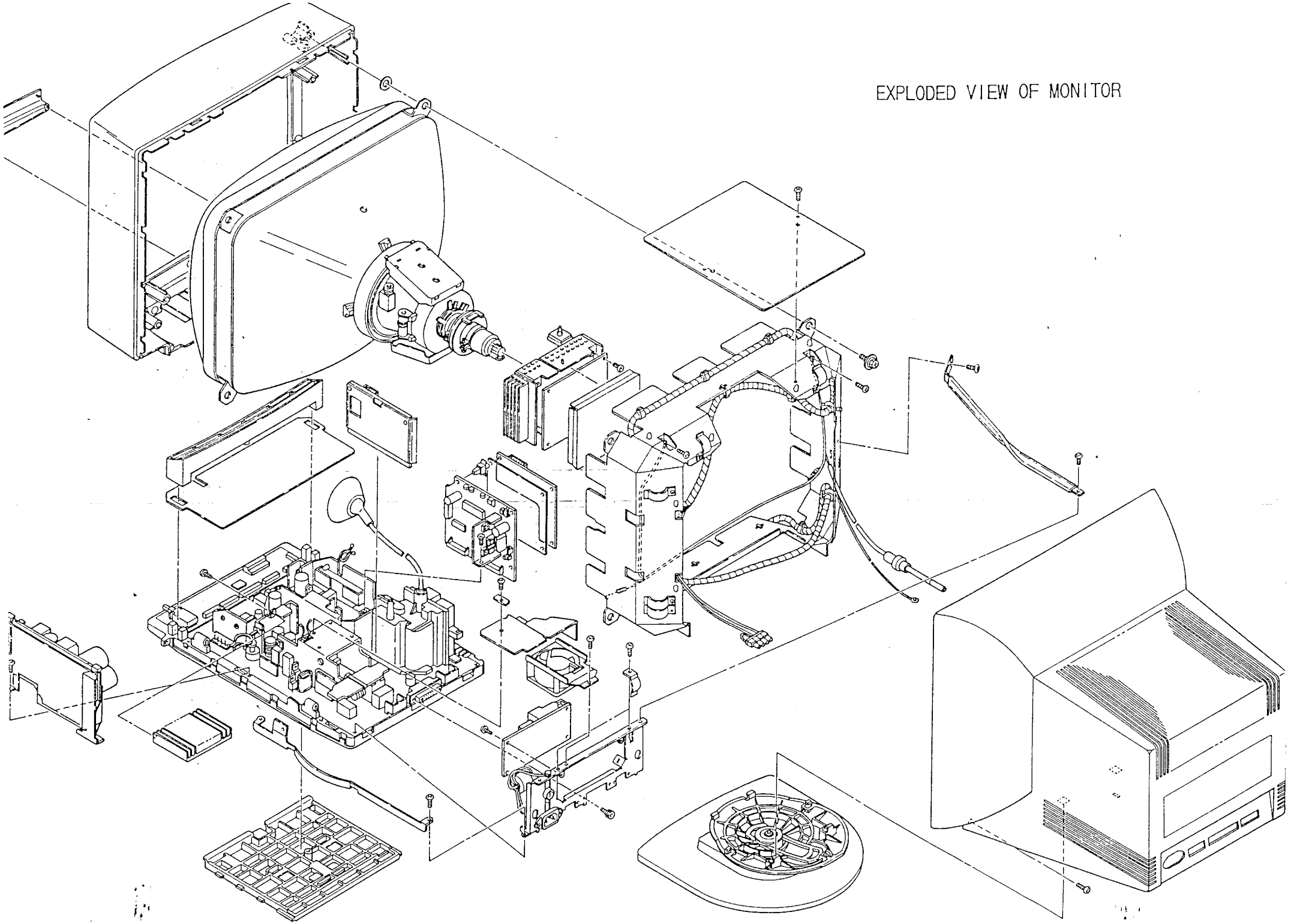
TRUTH TABLE

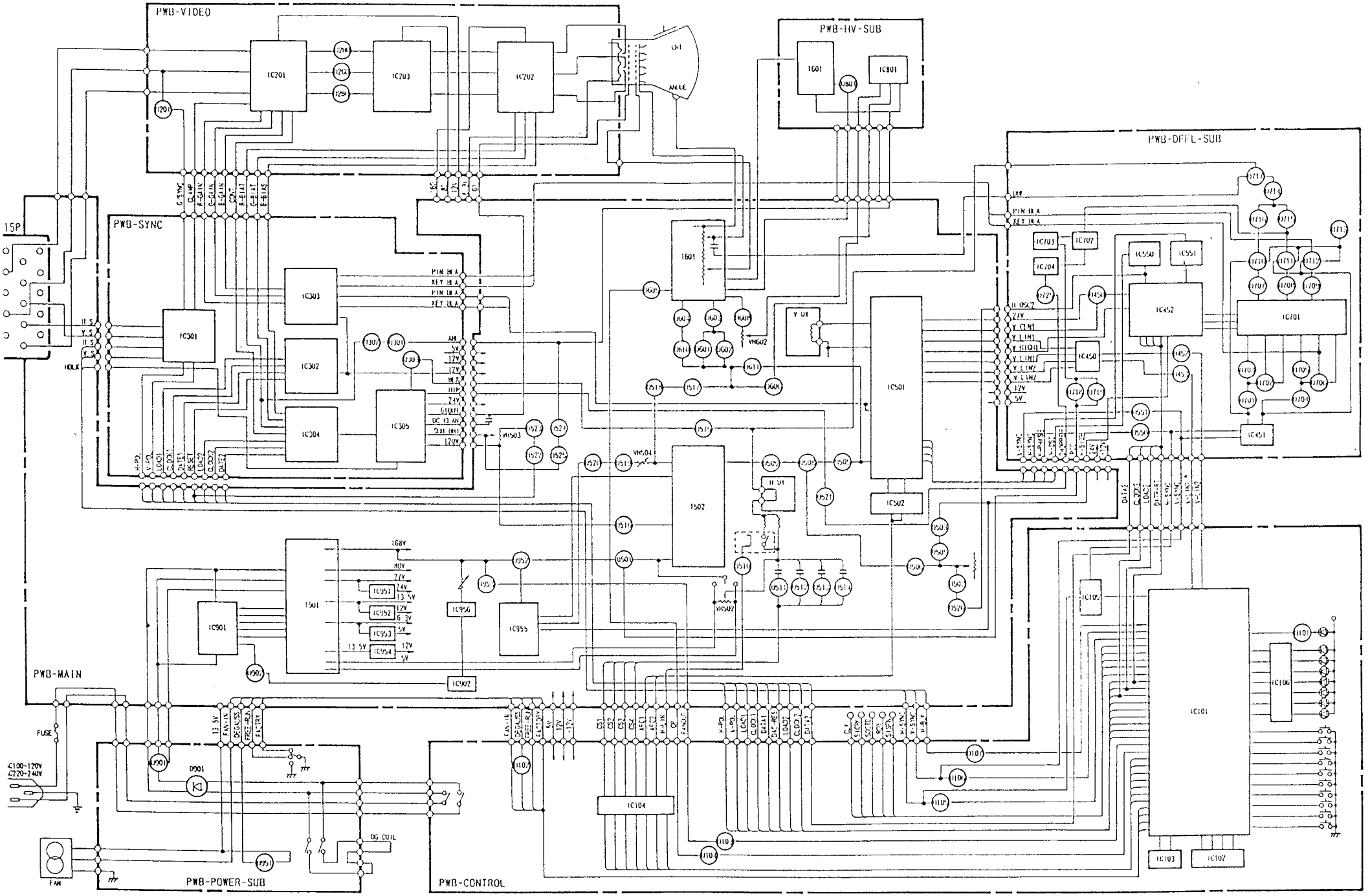
A	B	CHANN	fv
0	0	0X, 0Y	60
1	0	1X, 1Y	70
0	1	2X, 2Y	90
1	1	3X, 3Y	120

MODEL : TFS6705K

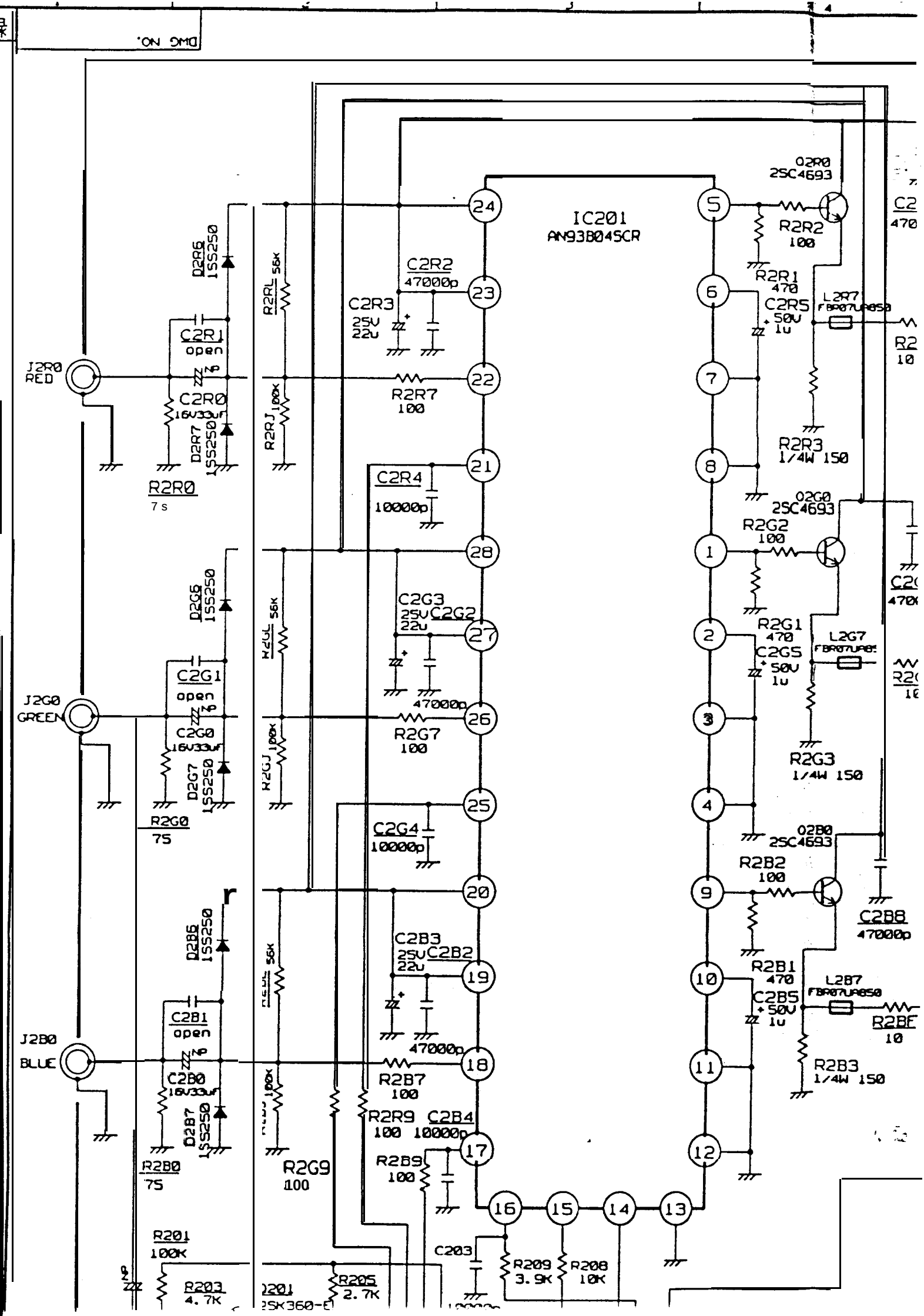
PCB-SINE

SCHEMATIC-DIAGRM


EXPLODED VIEW OF MONITOR



MODEL: TFS6705
BLOCK-DIAGRAM


IC201
AN93B04SCR
J2R0
RED
J2G0
GREEN
J2B0
BLUE
D2R6
1SS250
D2G6
1SS250
D2B6
1SS250
C2R1
open
C2G1
open
C2B1
open
C2R0
16V33uF
C2G0
16V33uF
C2B0
16V33uF
D2R7
1SS250
D2G7
1SS250
D2B7
1SS250
R2R0
7 s
R2G0
75
R2B0
75
R2RL 56K
R2RJ 100K
R2GL 56K
R2GJ 100K
R2BL 56K
R2BJ 100K
C2R2
47000p
C2R3
25V
22u
R2R7
100
C2R4
10000p
C2G3
25V
22u
C2G2
47000p
R2G7
100
C2G4
10000p
C2B3
25V
22u
C2B2
47000p
R2B7
100
R2R9
100
C2B4
10000p
R2B9
100
R2G9
100
R201
100K
R203
4.7K
R205
2.7K
C203
R209
3.9K
R208
10K
02R0
2SC4693
R2R2
100
R2R1
470
C2R5
50V
1u
L2R7
R2R3
1/4W 150
02G0
2SC4693
R2G2
100
R2G1
470
C2G5
50V
1u
L2G7
R2G3
1/4W 150
02B0
2SC4693
R2B2
100
R2B1
470
C2B5
50V
1u
L2B7
R2B3
1/4W 150
C2B8
47000p
24
23
22
21
28
27
26
25
20
19
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16
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5
6
7
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1
2
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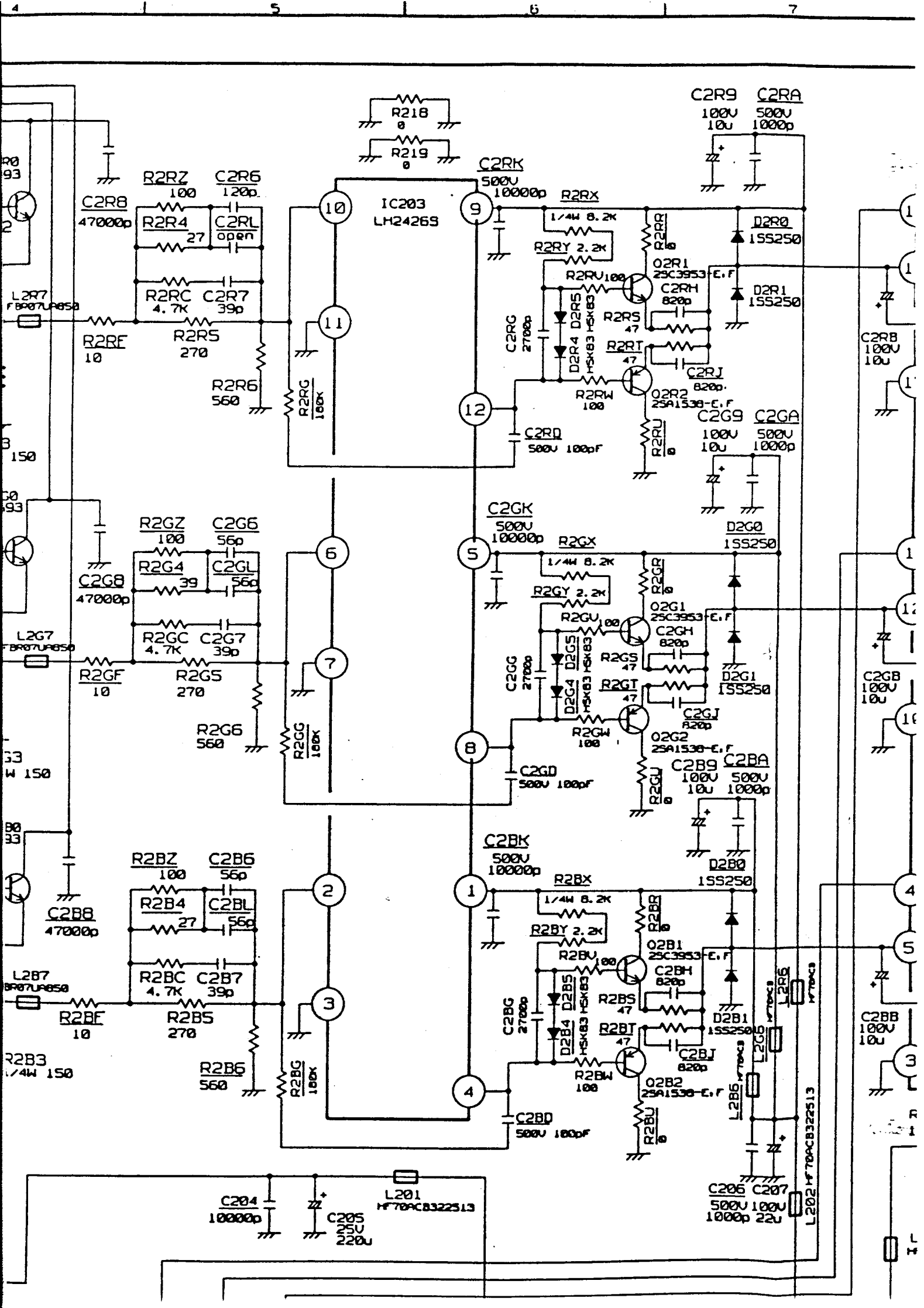
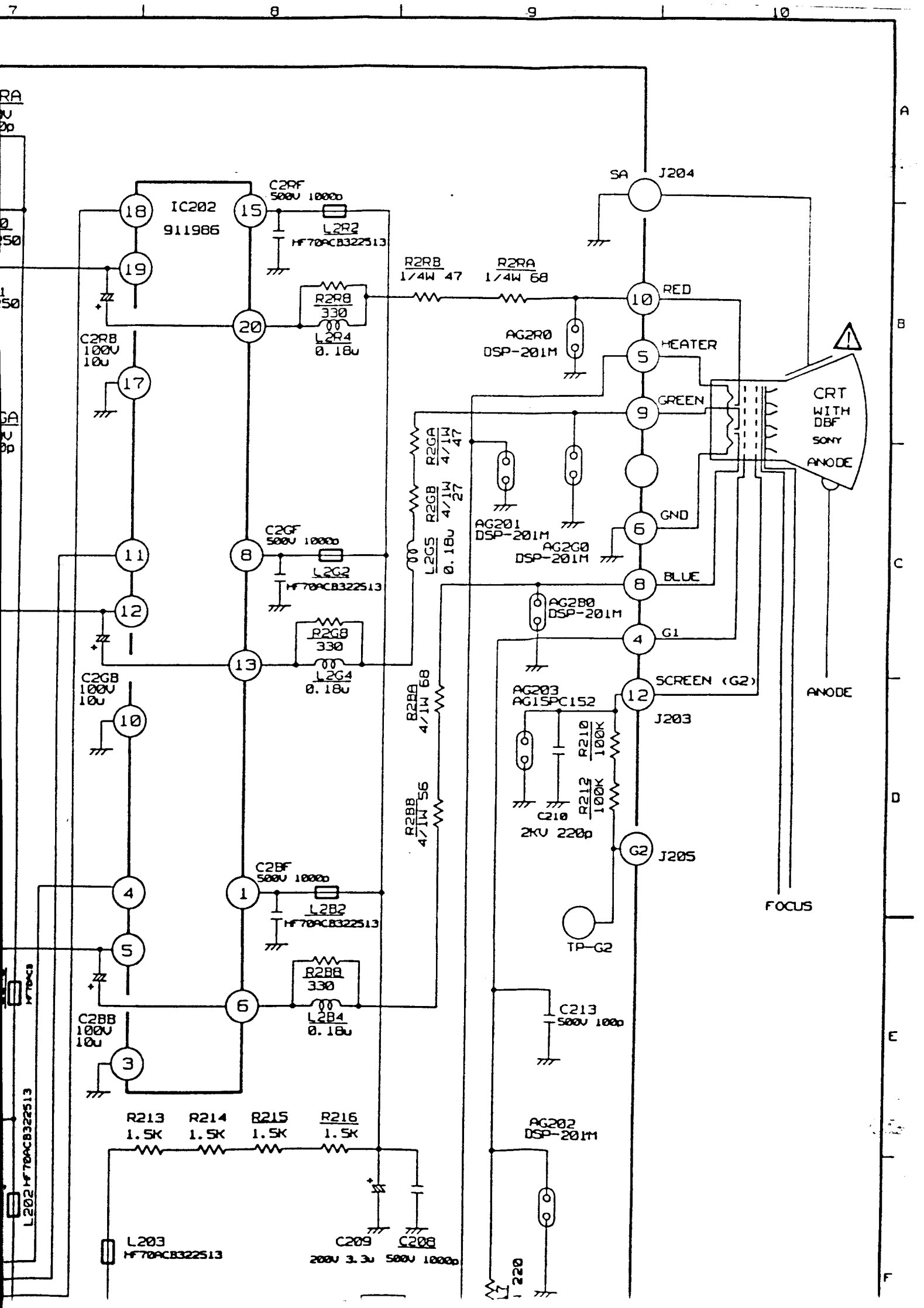
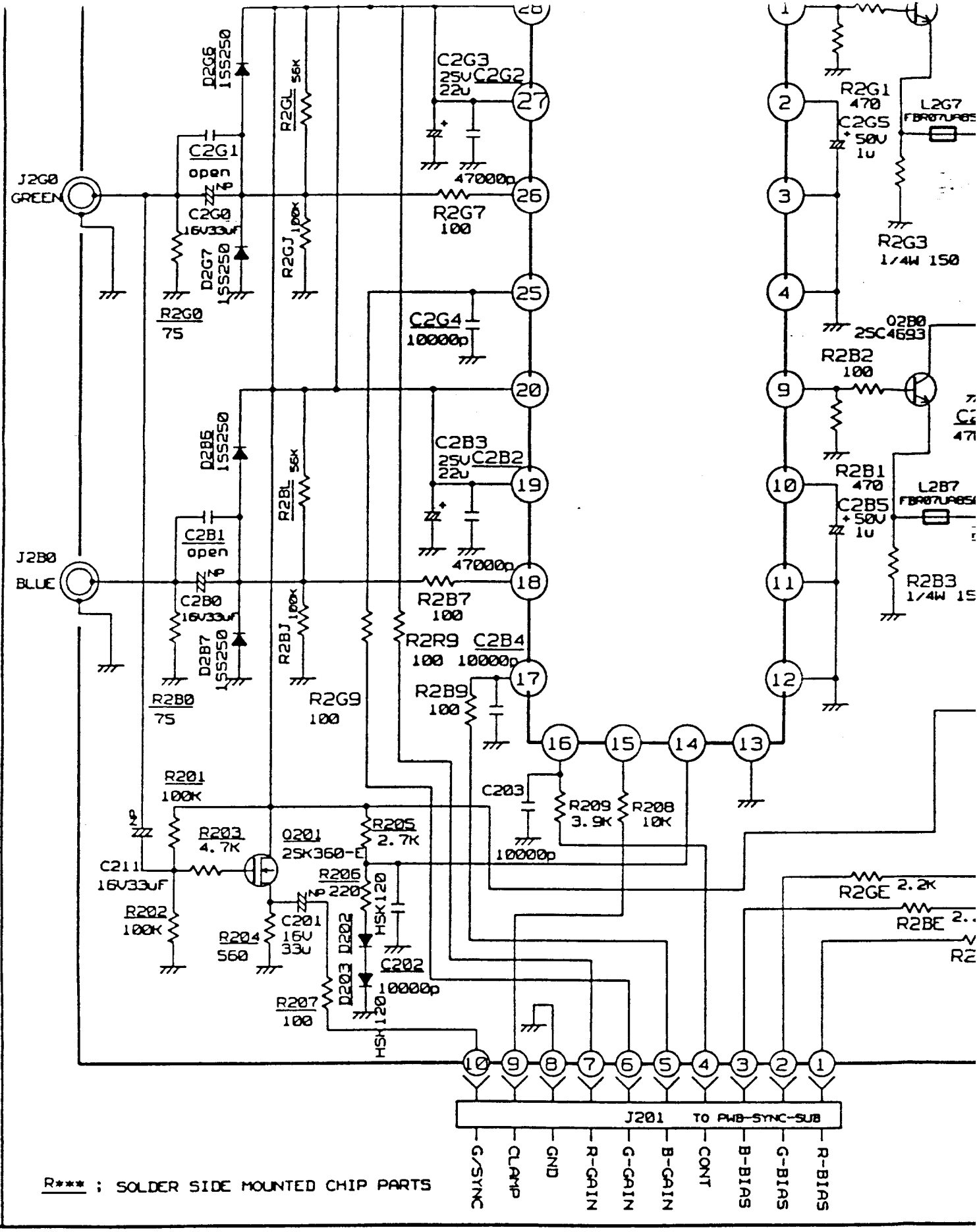
4
9
10
11
12


IC203
LH2426S
R218
0
R219
0
C2RK
500V
10000p
R2RX
C2R9
100V
10u
C2RA
500V
1000p
R2RZ
100
C2R6
120p
C2R8
47000p
R2R4
27
C2RL
open
R2RC
4.7K
C2R7
39p
R2RF
10
R2RS
270
R2R6
560
R2RG
180K
1/4W 8.2K
R2RY 2.2K
R2RV
100
Q2R1
2SC3953-E,F
C2RH
820p
R2RS
47
R2RT
47
C2RJ
820p
R2RW
100
Q2R2
2SA1538-E,F
R2RU
0
C2RD
500V 100pF
D2R0
1SS250
D2R1
1SS250
C2RG
2700p
D2R4
D2R5
HSK83
C2R9
100V
10u
C2RA
500V
1000p
C2GK
500V
10000p
R2GX
R2GZ
100
C2G6
56p
R2G4
39
C2GL
56p
R2GC
4.7K
C2G7
39p
R2GF
10
R2GS
270
R2G6
560
R2GG
180K
C2GD
500V 100pF
D2G0
1SS250
Q2G1
2SC3953-E,F
C2GH
820p
R2GS
47
R2GT
47
C2GJ
820p
R2GW
100
Q2G2
2SA1538-E,F
C2GG
2700p
D2G5
D2G4
HSK83
C2B9
100V
10u
C2BA
500V
1000p
C2BK
500V
10000p
R2BX
R2BZ
100
C2B6
56p
R2B4
27
C2BL
56p
R2BC
4.7K
C2B7
39p
R2BF
10
R2BS
270
R2B6
560
R2BG
180K
C2BD
500V 100pF
D2B0
1SS250
Q2B1
2SC3953-E,F
C2BH
820p
R2BS
47
R2BT
47
C2BJ
820p
R2BW
100
Q2B2
2SA1538-E,F
C2BG
2700p
D2B5
D2B4
HSK83
C2RB
100V
10u
C2GB
100V
10u
C2BB
100V
10u
L2R6
L2G6
L2B6
C204
10000p
C205
25V
220u
L201
HF70AC8322513
C206
500V
1000p
C207
100V
22u
L202 HF70AC8322513


IC202
911986
C2RF
500V 1000p
L2R2
MF70ACB322513
R2RB
1/4W 47
R2RA
1/4W 68
R2R8
330
L2R4
0.18u
C2R8
100V
10u
C2GF
500V 1000p
L2G2
MF70ACB322513
R2G8
330
L2G4
0.18u
C2GB
100V
10u
C2BF
500V 1000p
L2B2
MF70ACB322513
R2B8
330
L2B4
0.18u
C2BB
100V
10u
R2GA
4/1W 47
R2GB
4/1W 27
L2G5
0.18u
R2BA
4/1W 68
R2BB
4/1W 56
R213
1.5K
R214
1.5K
R215
1.5K
R216
1.5K
L203
MF70ACB322513
C209
200V 3.3u
C208
500V 1000p
L202 MF70ACB322513
SA
J204
RED
HEATER
GREEN
GND
BLUE
G1
SCREEN (G2)
J203
G2
J205
AG2R0
DSP-201M
AG201
DSP-201M
AG2G0
DSP-201M
AG2B0
DSP-201M
AG203
AG15PC152
R210
100K
R212
100K
C210
2KV 220p
TP-G2
C213
500V 100p
AG202
DSP-201M
CRT
WITH
DBF
SONY
ANODE
ANODE
FOCUS



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ABBREVE=17S

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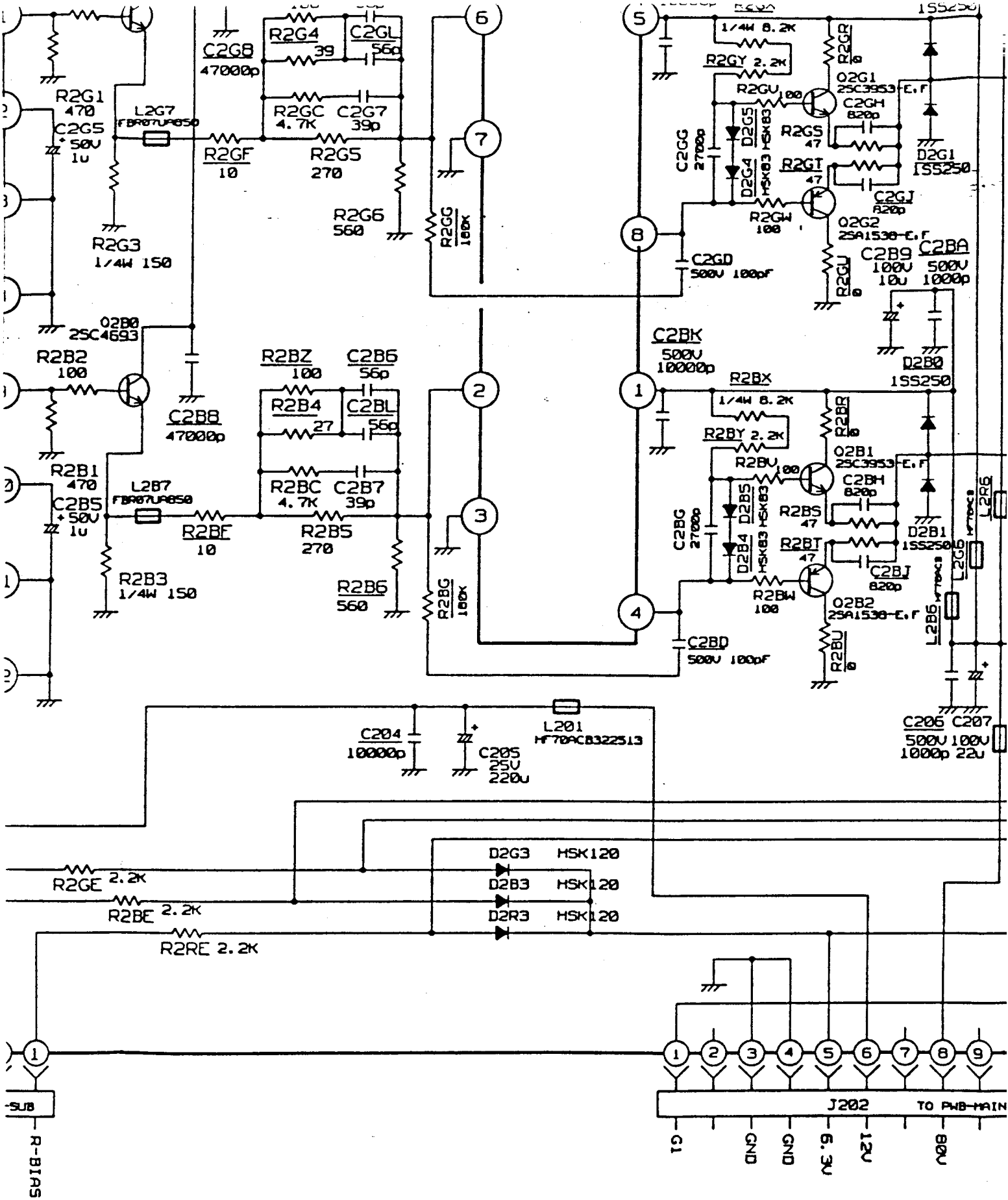
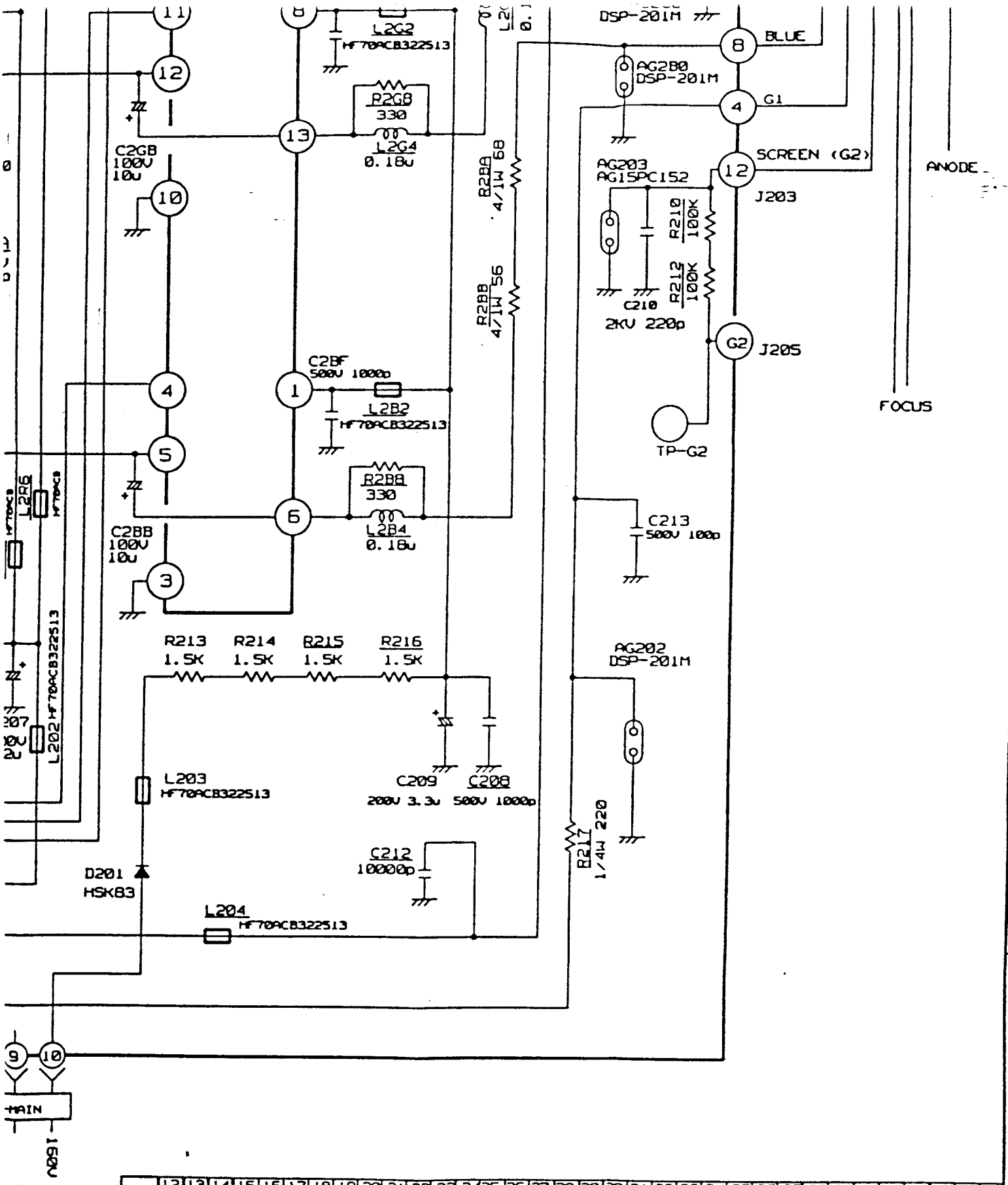


DEFINE

X_FIRST=0

X_STEP=SIZE

控		
出図用		
外注用		
計画	1	



CODE	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45

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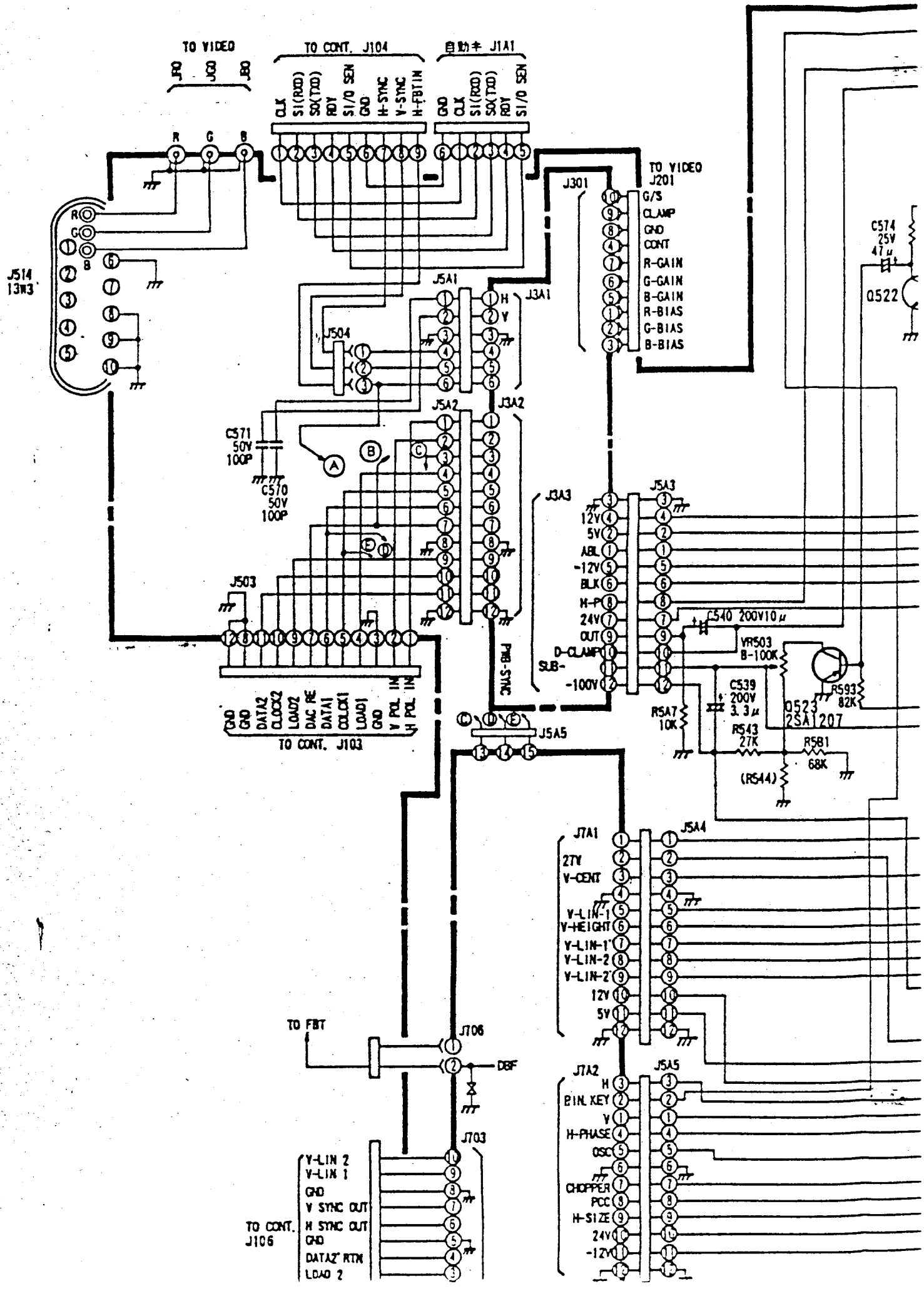
NAGASAKI WORKS

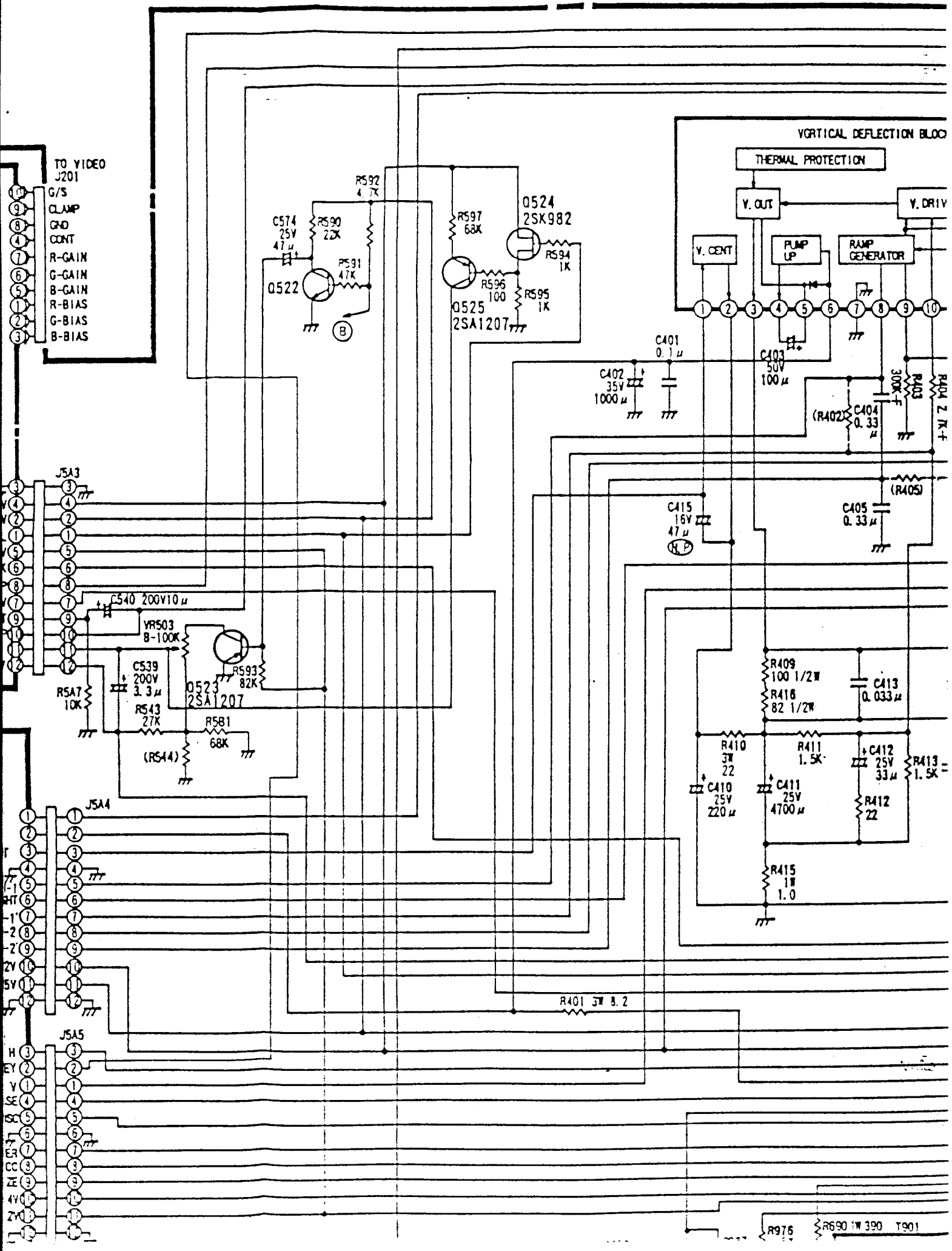
TFS6705SK

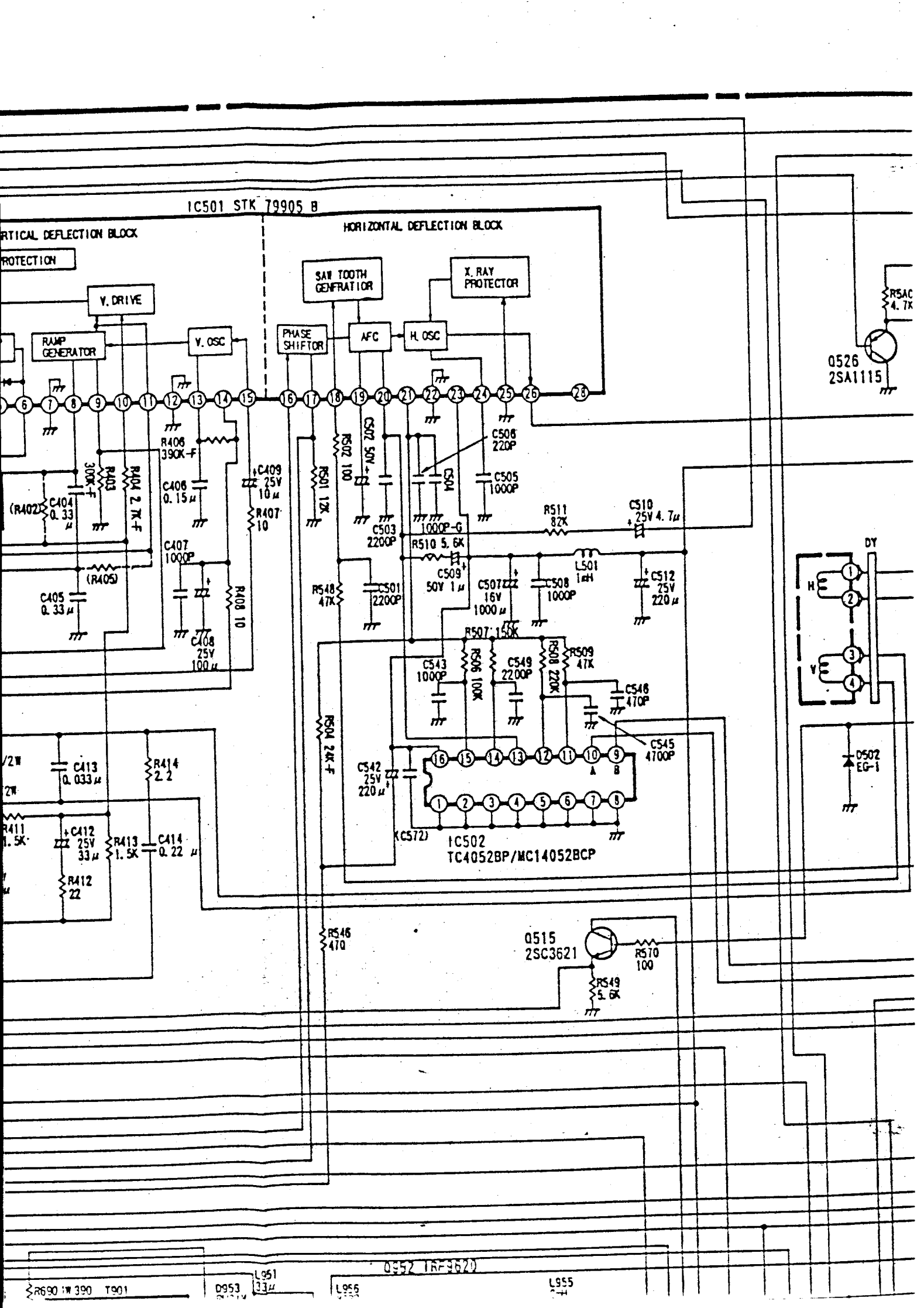
DIM. IN mm	DATE		APPROVED
SCALE	DRAWN		
:	CHECKED		
NTS	DESIGNED		

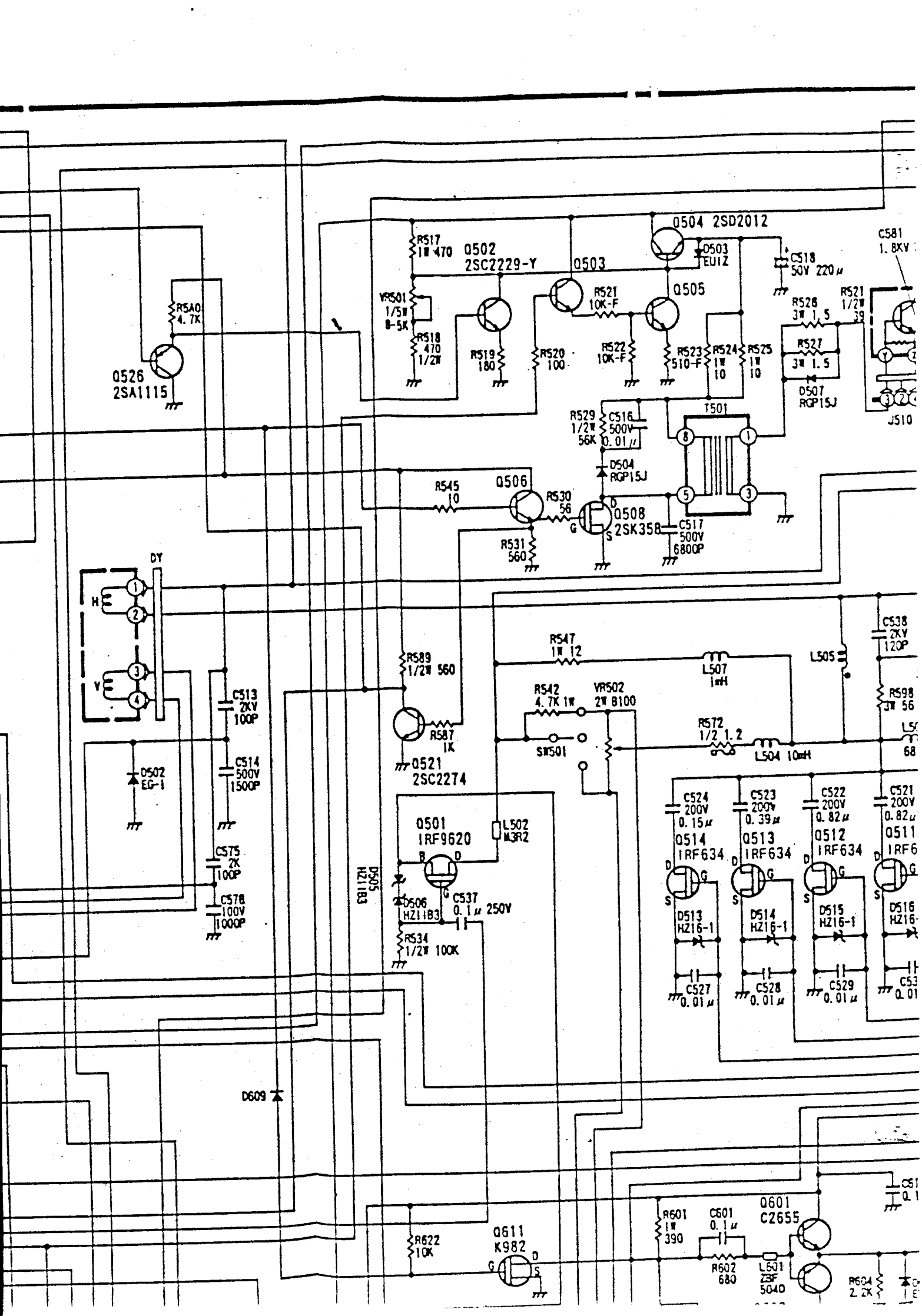
TITLE SCHEMATIC DIAGRAM
PCB-VIDEO

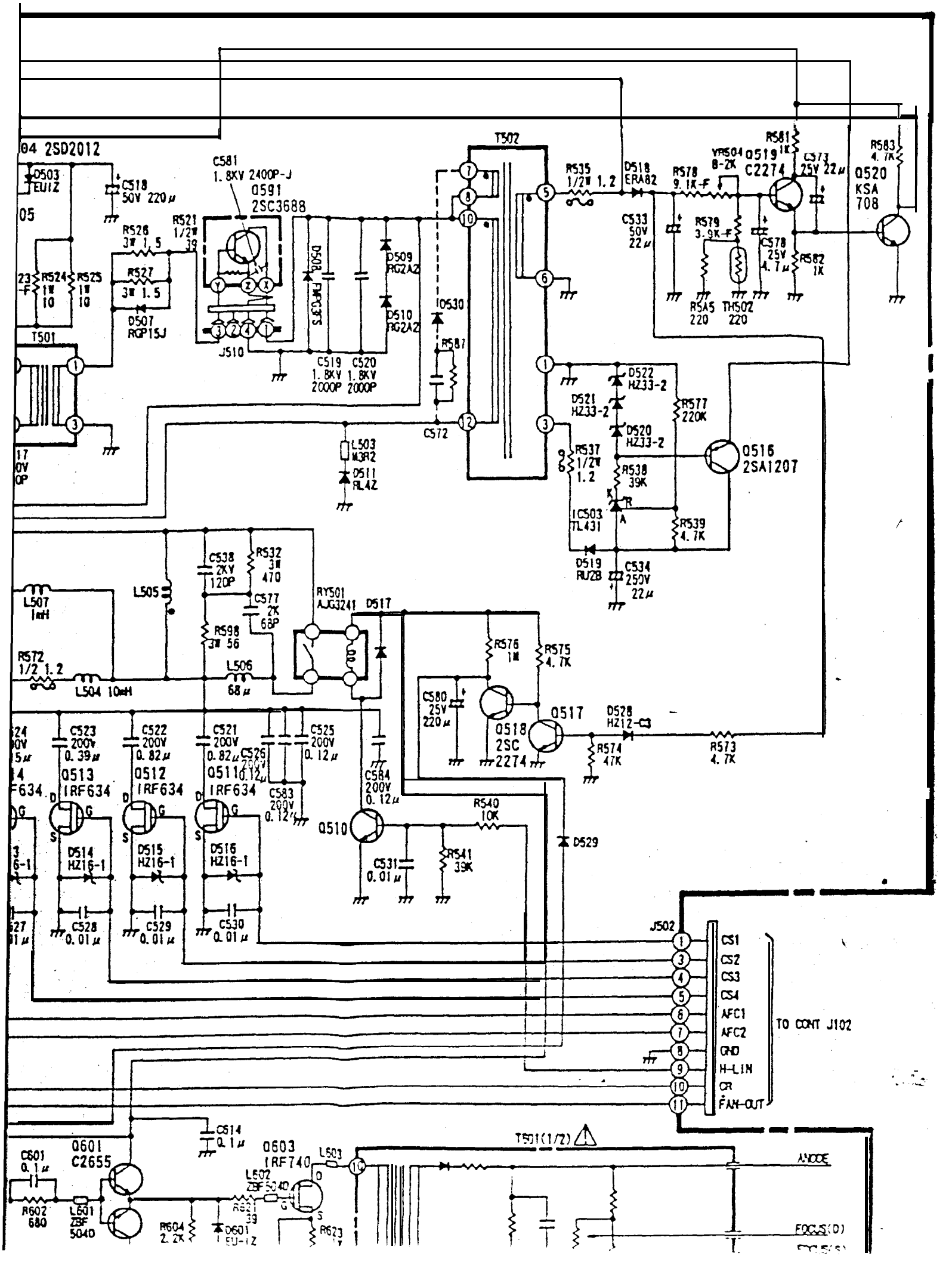
7 8 9 10

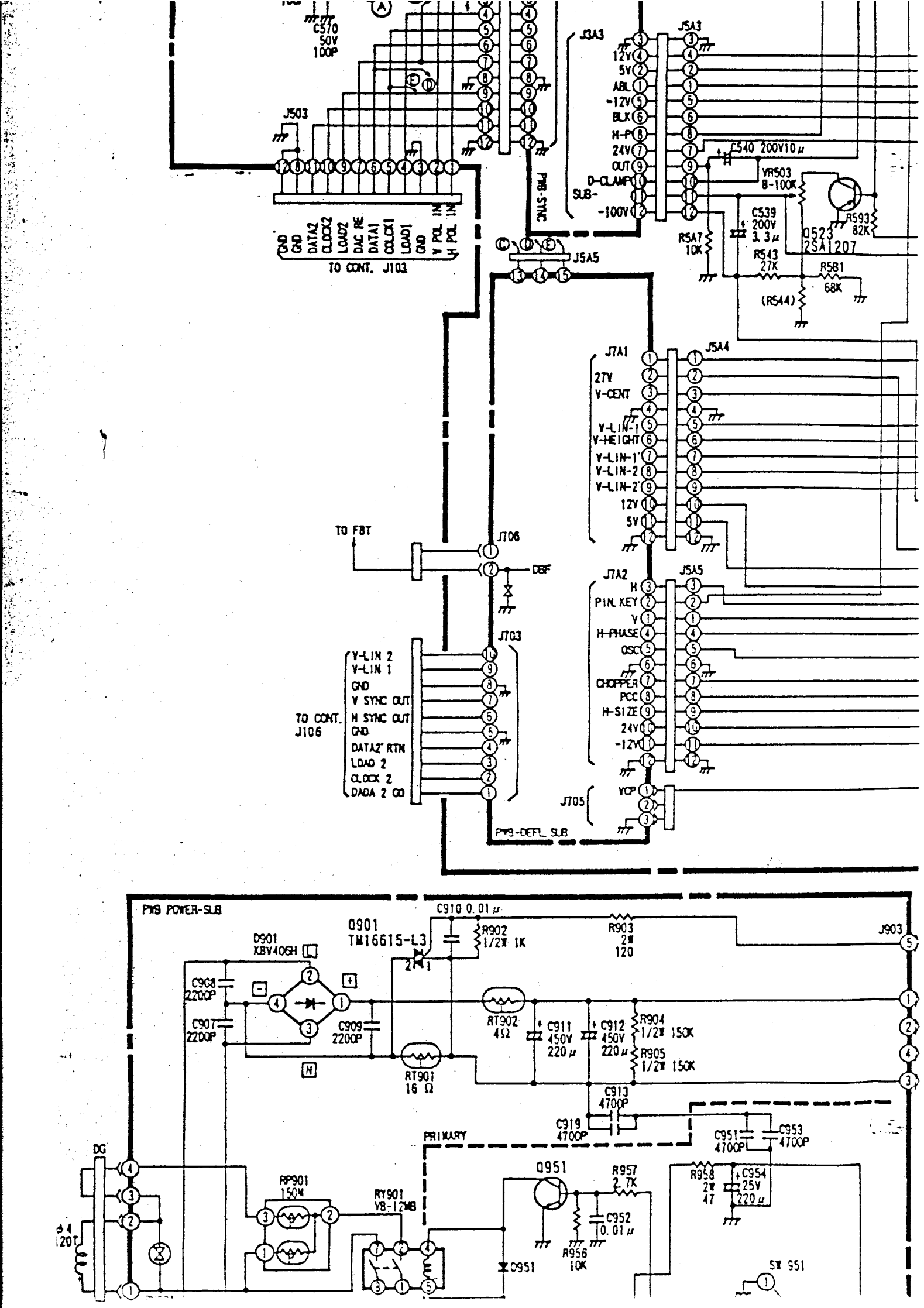

TO VIDEO
J201
TO CONT. J104
自動キ J1A1
CLK
SI(RXD)
SO(TXD)
RDY
SI/O SEN
GND
H-SYNC
V-SYNC
H-FBTIN
R
G
B
J514
13W3
J301
G/S
CLAMP
GND
CONT
R-GAIN
G-GAIN
B-GAIN
R-BIAS
G-BIAS
B-BIAS
J5A1
J3A1
J504
J5A2
J3A2
C571
50V
100P
C570
50V
100P
J503
J3A3
J5A3
12V
5V
ABL
-12V
BLK
H-P
24V
OUT
D-CLAMP
SUB-
-100V
C540 200V10μ
VR503
B-100K
R593
82K
C539
200V
3.3μ
R5A7
10K
R543
27K
R581
68K
(R544)
Q523
2SA1207
C574
25V
47μ
Q522
PBL-SYNC
J5A5
GND
GND
DATA2
CLOCK2
LOAD2
DAC RE
DATA1
CLOCK1
LOAD1
GND
V POL IN
H POL IN
TO CONT. J103
J7A1
J5A4
27V
V-CENT
V-LIN-1
V-HEIGHT
V-LIN-1'
V-LIN-2
V-LIN-2'
12V
5V
TO FBT
J706
DBF
J703
J7A2
J5A5
H
PIN. KEY
V
H-PHASE
OSC
CHOPPER
PCC
H-SIZE
24V
-12V
TO CONT.
J106
V-LIN 2
V-LIN 1
GND
V SYNC OUT
H SYNC OUT
GND
DATA2' RTN
LOAD 2

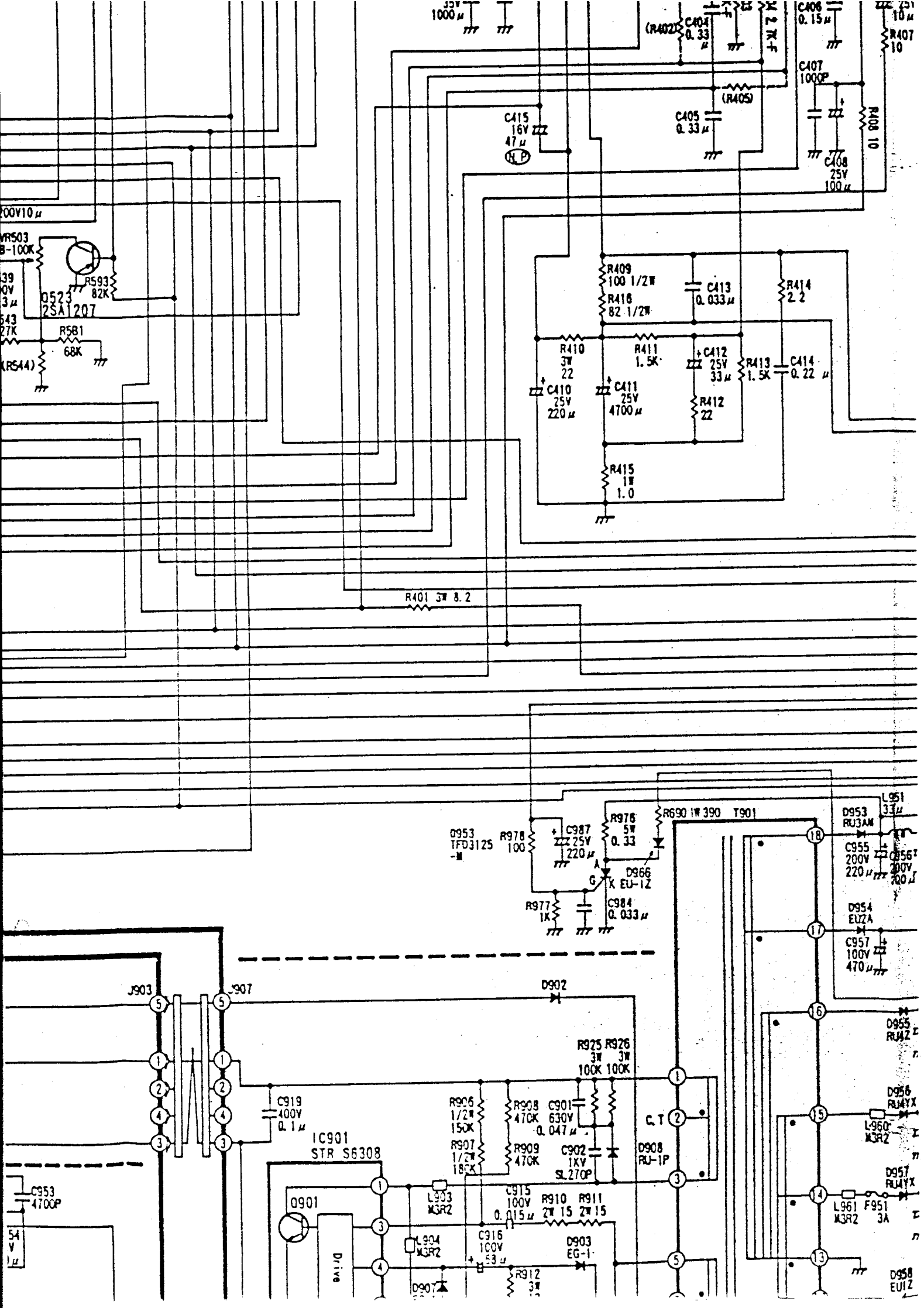

TO VIDEO
J201
G/S
CLAMP
GND
CONT
R-GAIN
G-GAIN
B-GAIN
R-BIAS
G-BIAS
B-BIAS
R592
4.7K
C574
25V
47μ
R590
22K
R591
47K
Q522
B
R597
68K
Q524
2SK982
R594
1K
R596
100
R595
1K
Q525
2SA1207
VERTICAL DEFLECTION BLOCK
THERMAL PROTECTION
V. OUT
V. DRIV
V. CENT
PUMP UP
RAMP GENERATOR
C401
0.1μ
C402
35V
1000μ
C403
50V
100μ
300K
R403
R404 2.7K
(R402)
C404
0.33μ
(R405)
C405
0.33μ
C415
16V
47μ
J5A3
C540 200V10μ
VR503
B-100K
R593
82K
Q523
2SA1207
R547
10K
C539
200V
3.3μ
R543
27K
R581
68K
(R544)
R409
100 1/2W
R416
82 1/2W
C413
0.033μ
R410
3W
22
C410
25V
220μ
R411
1.5K
C411
25V
4700μ
C412
25V
33μ
R412
22
R413
1.5K
R415
1W
1.0
J5A4
R401 3W 8.2
J5A5
R976
R690 1W 390
T901

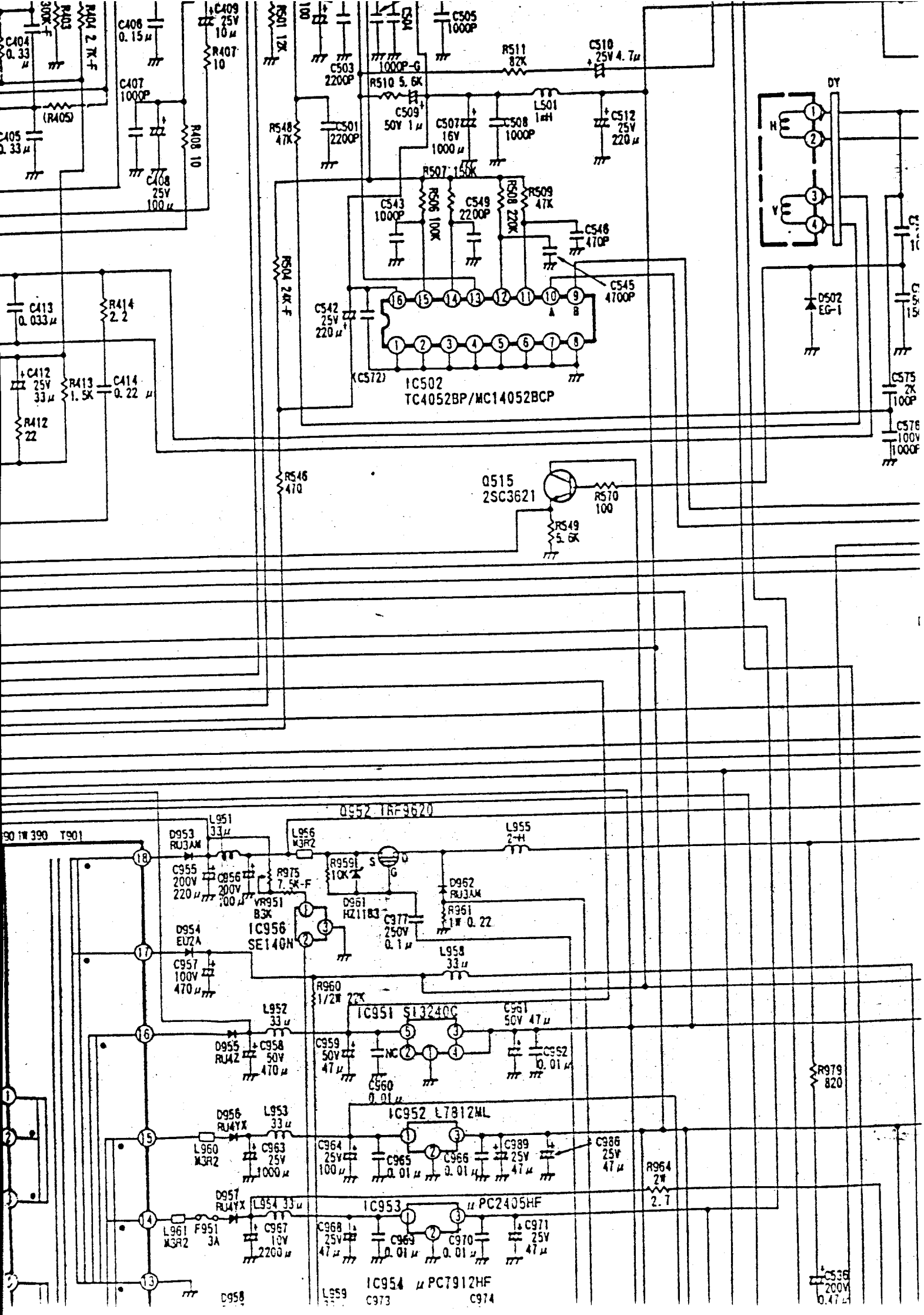

IC501 STK 79905 B
RTICAL DEFLECTION BLOCK
ROTECTION
HORIZONTAL DEFLECTION BLOCK
Y. DRIVE
RAMP GENERATOR
Y. OSC
PHASE SHIFTOR
AFC
H. OSC
SAW TOOTH GENFRATIOR
X. RAY PROTECTOR
R406 390K-F
C406 0.15μ
C409 25V 10μ
R407 10
C404 0.33μ
R403 300K-F
R404 2.7K-F
(R402)
(R405)
C405 0.33μ
C407 1000P
C408 25V 100μ
R408 10
R501 12K
R502 100
C502 50V
C503 2200P
C504
C505 1000P
C506 220P
1000P-G
R510 5.6K
C509 50V 1μ
R511 82K
C510 25V 4.7μ
L501 1mH
C507 16V 1000μ
C508 1000P
C512 25V 220μ
R548 47K
C501 2200P
R507 150K
R506 100K
C543 1000P
C549 2200P
R508 220K
R509 47K
C546 470P
C545 4700P
R504 2.2K-F
C542 25V 220μ
(C572)
IC502
TC4052BP/MC14052BCP
R546 470
Q515
2SC3621
R570 100
R549 5.6K
Q526
2SA1115
R5AC 4.7K
DY
H
V
D502 EG-1
C413 0.033μ
R414 2.2
R411 1.5K
C412 25V 33μ
R413 1.5K
C414 0.22μ
R412 22
R690 1W 390
T901
D953
L951 33μ
L956
L955
Q952 IRF9620

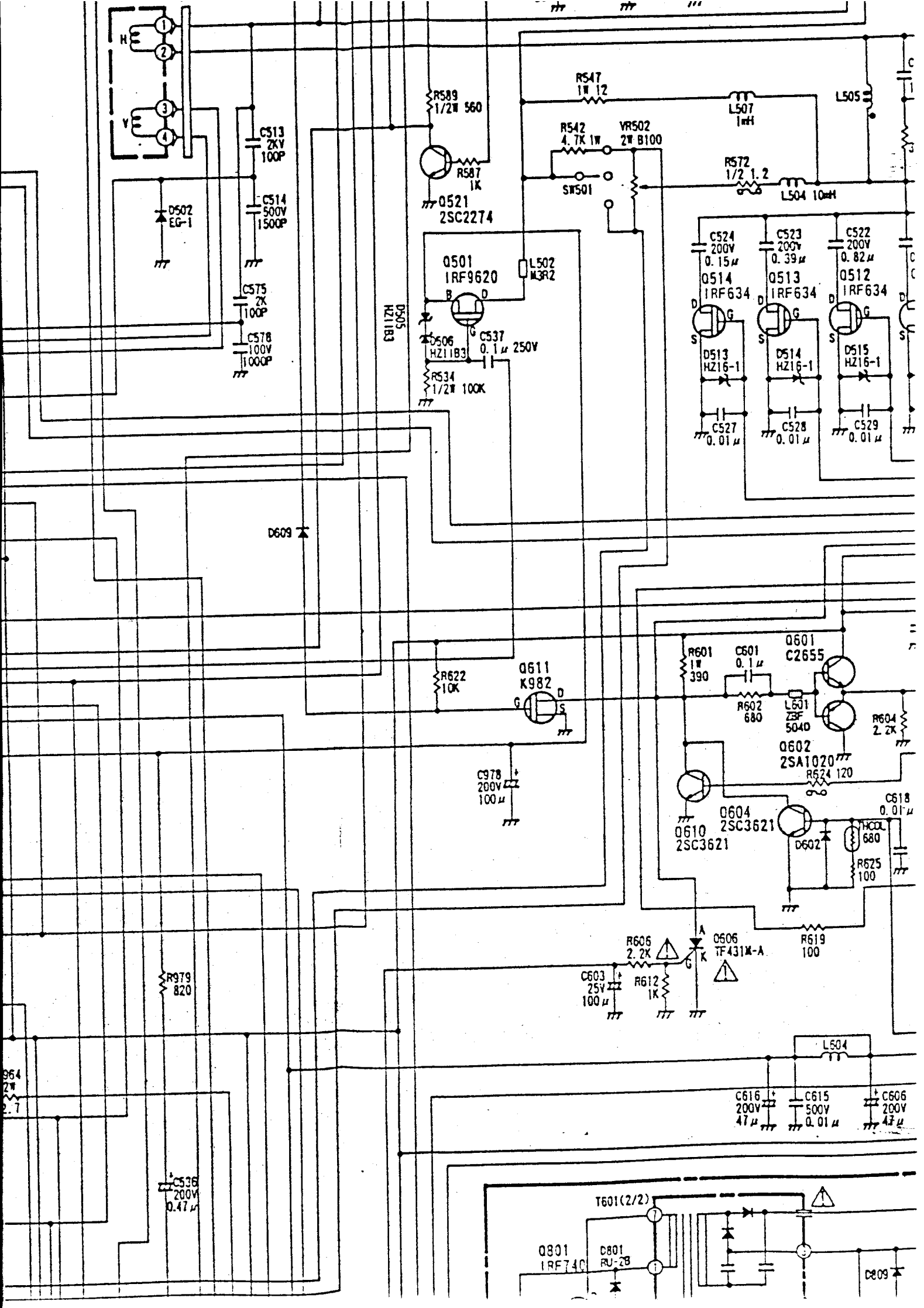

Q504 2SD2012
R517 1W 470
Q502 2SC2229-Y
Q503
D503 EU1Z
C518 50V 220μ
C581 1.8KV
VR501 1/5W B-5K
R518 470 1/2W
R519 180
R520 100
R521 10K-F
Q505
R522 10K-F
R523 510-F
R524 1W 10
R525 1W 10
R526 3W 1.5
R527 3W 1.5
R521 1/2W 39
D507 RGP15J
J510
R5A0 4.7K
Q526 2SA1115
R529 1/2W 56K
C516 500V 0.01μ
T501
D504 RGP15J
R545 10
Q506
R530 56
Q508 2SK358
C517 500V 6800P
R531 560
DY
H
V
C513 2KV 100P
C514 500V 1500P
D502 EG-1
C575 2K 100P
C578 100V 1000P
R589 1/2W 560
R587 1K
Q521 2SC2274
R547 1W 12
L507 1mH
L505
C538 2KV 120P
R598 3W 56
R542 4.7K 1W
VR502 2W B100
SW501
R572 1/2 1.2
L504 10mH
Q501 IRF9620
L502 M3R2
D505 HZ11B3
D506 HZ11B3
C537 0.1μ 250V
R534 1/2W 100K
C524 200V 0.15μ
C523 200V 0.39μ
C522 200V 0.82μ
C521 200V 0.82μ
Q514 IRF634
Q513 IRF634
Q512 IRF634
Q511 IRF6
D513 HZ16-1
D514 HZ16-1
D515 HZ16-1
D516 HZ16-
C527 0.01μ
C528 0.01μ
C529 0.01μ
D609
R622 10K
Q611 K982
R601 1W 390
C601 0.1μ
Q601 C2655
R602 680
L601 2SF 504D
R604 2.2K

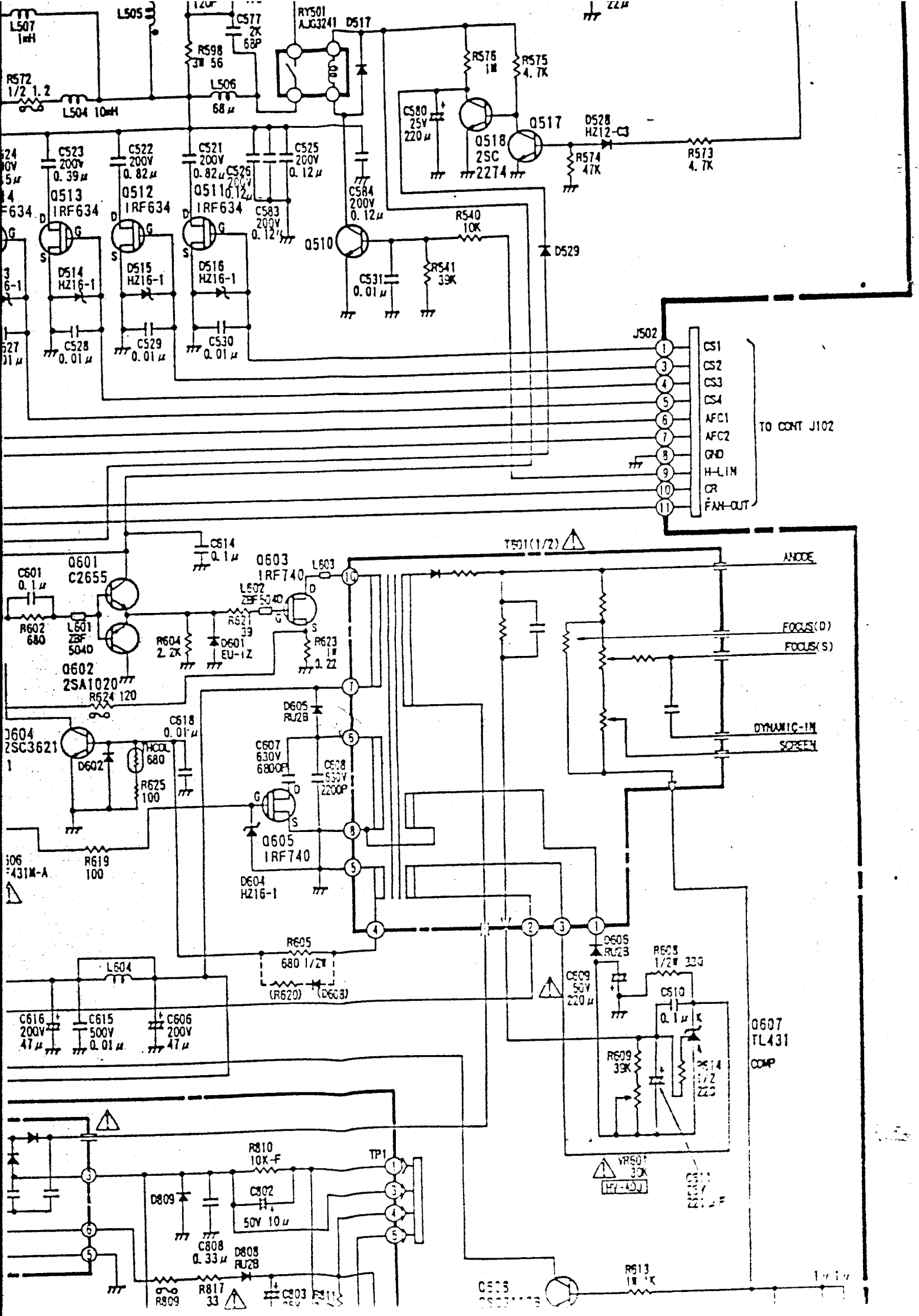

04 2SD2012
D503 EU1Z
C518 50V 220μ
05
R526 3W 1.5
R527 3W 1.5
D507 RGP15J
R524 1W 10
R525 1W 10
T501
C581 1.8KV 2400P-J
Q591 2SC3688
R521 1/2W 39
J510
D508 FMC3FS
D509 RG2A2
D510 RG2A2
C519 1.8KV 2000P
C520 1.8KV 2000P
T502
D530
R587
C572
L503 M3R2
D511 RL4Z
R535 1/2W 1.2
D518 ERA82
R578 9.1K-F
VR504 B-2K
Q519 C2274
C573 25V 22μ
R581 1K
R583 4.7K
Q520 KSA 708
C533 50V 22μ
R579 3.9K-F
C578 25V 4.7μ
R582 1K
R5A5 220
TH502 220
D522 HZ33-2
D521 HZ33-2
D520 HZ33-2
R577 220K
Q516 2SA1207
R537 1/2W 1.2
R538 39K
IC503 TL431
R539 4.7K
D519 RU2B
C534 250V 22μ
C538 2KV 120P
R532 3W 470
C577 2K 68P
R598 3W 56
L505
L507 1mH
L506 68μ
L504 10mH
R572 1/2 1.2
RY501 AJG3241
D517
R576 1M
R575 4.7K
C580 25V 220μ
Q518 2SC 2274
Q517
D528 HZ12-C3
R574 47K
R573 4.7K
C523 200V 0.39μ
C522 200V 0.82μ
C521 200V 0.82μ
C526 200V 0.12μ
C525 200V 0.12μ
C583 200V 0.12μ
C584 200V 0.12μ
Q513 IRF634
Q512 IRF634
Q511 IRF634
Q510
R540 10K
C531 0.01μ
R541 39K
D529
D514 HZ16-1
D515 HZ16-1
D516 HZ16-1
C528 0.01μ
C529 0.01μ
C530 0.01μ
J502
CS1
CS2
CS3
CS4
AFC1
AFC2
GND
H-LIN
CR
FAN-OUT
TO CONT J102
C614 0.1μ
Q601 C2655
Q603 IRF740
C601 0.1μ
L602 2SF5040
L603
R602 680
L601 2SF 5040
R604 2.2K
D601 EU-1Z
R623
T501(1/2)
ANODE
FOCUS(D)

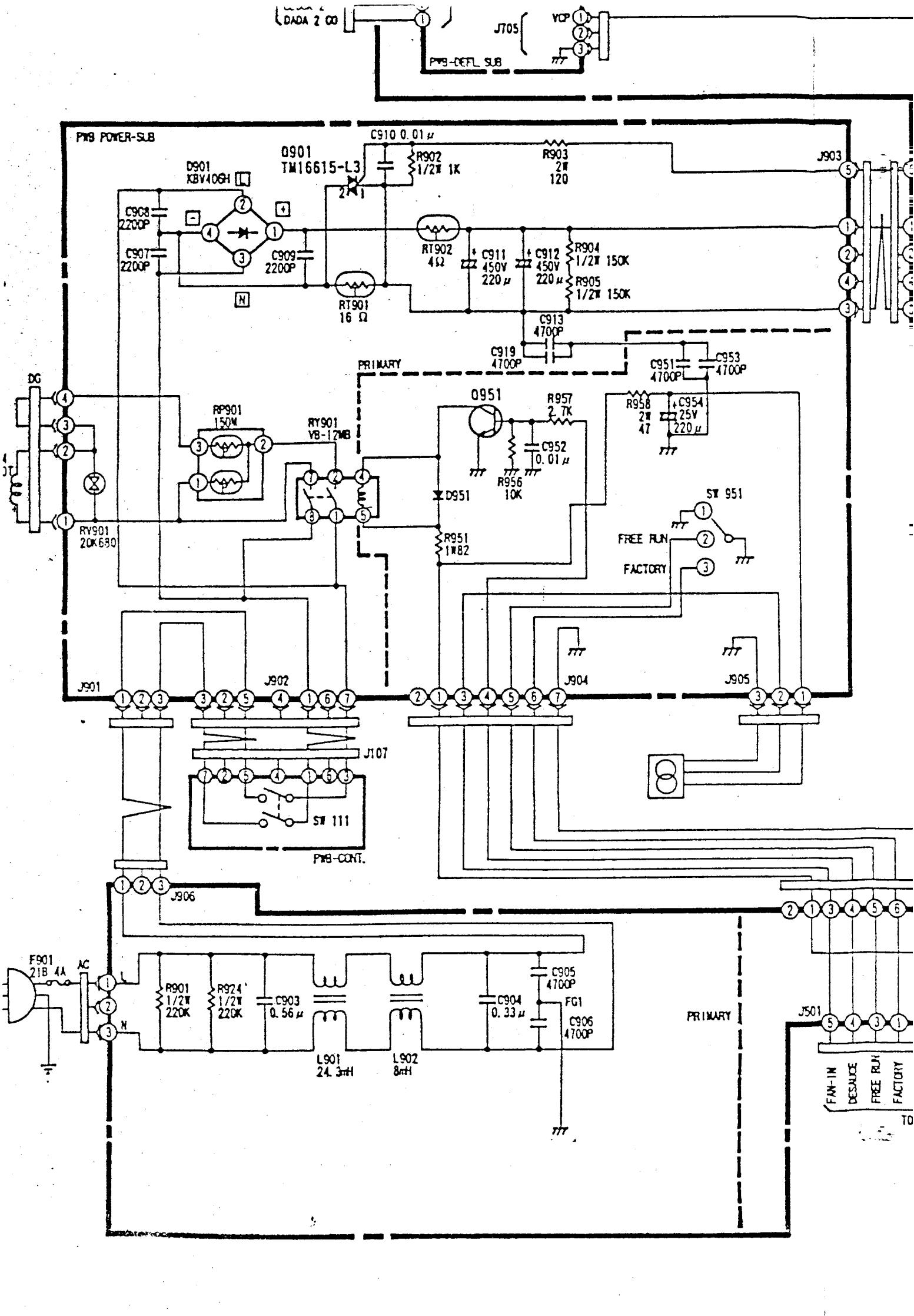

C570 50V 100P
J503
J3A3
J5A3
12V
5V
ABL
-12V
BLK
H-P
24V
OUT
D-CLAMP
SUB-
-100V
C540 200V10μ
VR503 B-100K
R593 82K
C539 200V 3.3μ
R5A7 10K
R543 27K
R581 68K
(R544)
Q523 2SA1207
GND GND DATA2 CLOCK2 LOAD2 DAC RE DATA1 CLOCK1 LOAD1 GND V POL IN H POL IN
TO CONT. J103
PWB-SYNC
J5A5
J7A1
J5A4
27V
V-CENT
V-LIN-1
V-HEIGHT
V-LIN-1'
V-LIN-2
V-LIN-2'
12V
5V
TO FBT
J706
DBF
J7A2
H
PIN. KEY
V
H-PHASE
OSC
CHOPPER
PCC
H-SIZE
24V
-12V
J703
Y-LIN 2
V-LIN 1
GND
V SYNC OUT
H SYNC OUT
GND
DATA2' RTN
LOAD 2
CLOCK 2
DATA 2 OUT
TO CONT. J106
J705
YCP
PWB-DEFL SUB
PWB POWER-SUB
C910 0.01μ
Q901 TM16615-L3
R902 1/2W 1K
R903 2W 120
J903
D901 KBV406H
C908 2200P
C907 2200P
C909 2200P
RT902 4Ω
C911 450V 220μ
C912 450V 220μ
R904 1/2W 150K
R905 1/2W 150K
RT901 16Ω
C913 4700P
C919 4700P
C951 4700P
C953 4700P
PRIMARY
DG
RP901 150M
RY901 YB-12MB
Q951
R957 2.7K
C952 0.01μ
R956 10K
D951
R958 2W 47
C954 25V 220μ
SW 951

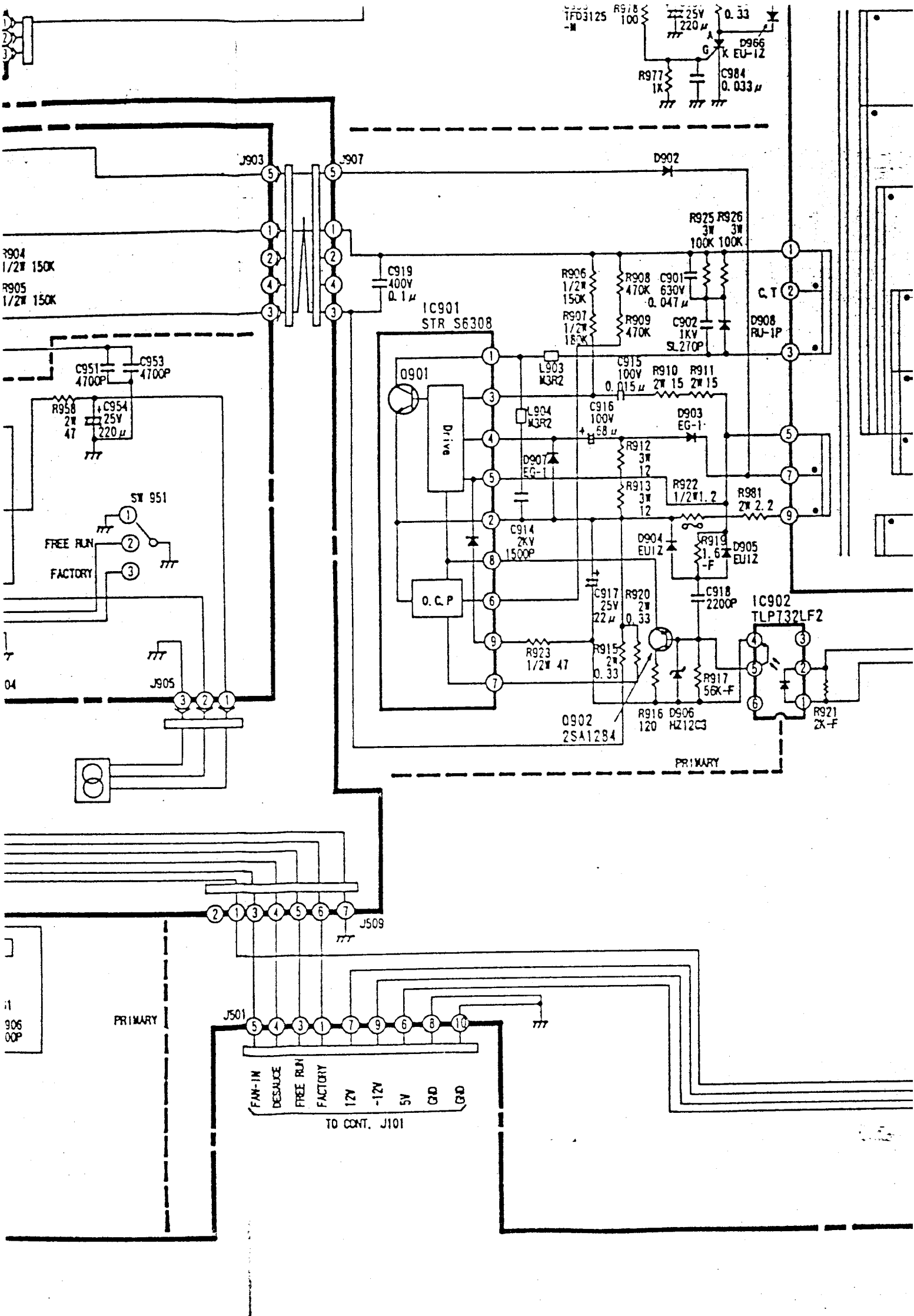

C415 16V 47μ
(R402)
C404 0.33μ
(R405)
C405 0.33μ
C406 0.15μ
R407 10
C407 1000P
C408 25V 100μ
R408 10
R409 100 1/2W
R416 82 1/2W
C413 0.033μ
R414 2.2
R410 3W 22
R411 1.5K
C412 25V 33μ
R413 1.5K
C414 0.22μ
C410 25V 220μ
C411 25V 4700μ
R412 22
R415 1W 1.0
R401 3W 8.2
R581 68K
R593 82K
0523 2SA1207
D953 TFD3125-M
R978 100
C987 25V 220μ
R976 5W 0.33
R690 1W 390
T901
D966 K EU-1Z
R977 1K
C984 0.033μ
L951 33μ
D953 RU3AM
C955 200V 220μ
D954 EU2A
C957 100V 470μ
D955 RU4Z
D956 RU4YX
L960 M3R2
D957 RU4YX
L961 M3R2
F951 3A
D958 EU1Z
J903
J907
D902
C919 400V 0.1μ
IC901 STR S6308
R906 1/2W 150K
R907 1/2W 180K
R908 470K
R909 470K
C901 630V 0.047μ
C902 1KV SL270P
R925 3W 100K
R926 3W 100K
D908 RU-1P
C.T
Q901
L903 M3R2
C915 100V 0.015μ
R910 2W 15
R911 2W 15
L904 M3R2
C916 100V 53μ
D903 EG-1
D907
R912 3W
C953 4700P

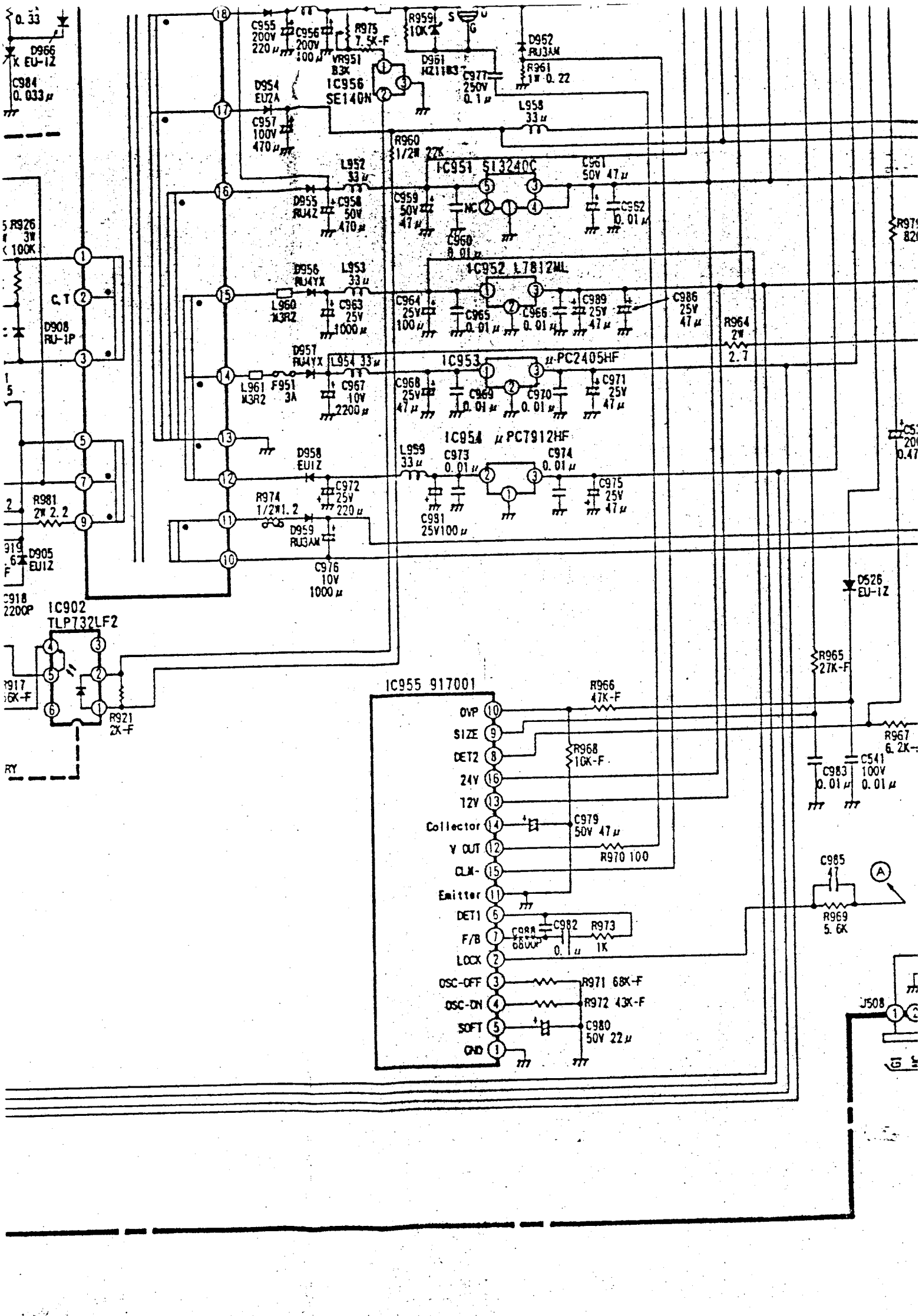

C404 0.33μ
R403 300K
R404 2.7K-F
C406 0.15μ
C409 25V 10μ
R407 10
C407 1000P
(R405)
C405 0.33μ
R408 10
C408 25V 100μ
R501 12K
C503 2200P
C505 1000P
1000P-G
R511 82K
C510 25V 4.7μ
R510 5.6K
C509 50V 1μ
C507 16V 1000μ
C508 1000P
L501 1mH
C512 25V 220μ
R548 47K
C501 2200P
R507 150K
R506 100K
C543 1000P
C549 2200P
R508 220K
R509 47K
C546 470P
C545 4700P
R504 2.2K-F
C542 25V 220μ
(C572)
IC502
TC4052BP/MC14052BCP
DY
H
V
D502 EG-1
C575 2K 100P
C576 100V 1000P
C413 0.033μ
R414 2.2
+C412 25V 33μ
R412 22
R413 1.5K
C414 0.22μ
R546 470
Q515 2SC3621
R570 100
R549 5.6K
Q952 IRF9620
T901
D953 RU3AM
L951 33μ
L956 M3R2
L955 2-H
C955 200V 220μ
C956 200V 100μ
R975 7.5K-F
VR951 B3K
IC956 SE140N
R959 10K
D961 HZ11B3
C377 250V 0.1μ
D962 RU3AM
R961 1W 0.22
D954 EU2A
C957 100V 470μ
L958 33μ
R960 1/2W 22K
IC951 S1324QC
C961 50V 47μ
L952 33μ
D955 RU4Z
C958 50V 470μ
C959 50V 47μ
NC
C952 0.01μ
C960 0.01μ
R979 820
D956 RU4YX
L953 33μ
L960 M3R2
C963 25V 1000μ
IC952 L7812ML
C964 25V 100μ
C965 0.01μ
C966 0.01μ
C989 25V 47μ
C986 25V 47μ
R964 2W 2.7
D957 RU4YX
L954 33μ
IC953 μPC2405HF
L961 M3R2
F951 3A
C967 10V 2200μ
C968 25V 47μ
C969 0.01μ
C970 0.01μ
C971 25V 47μ
IC954 μPC7912HF
C536 200V 0.47μ
D958
L959
C973
C974

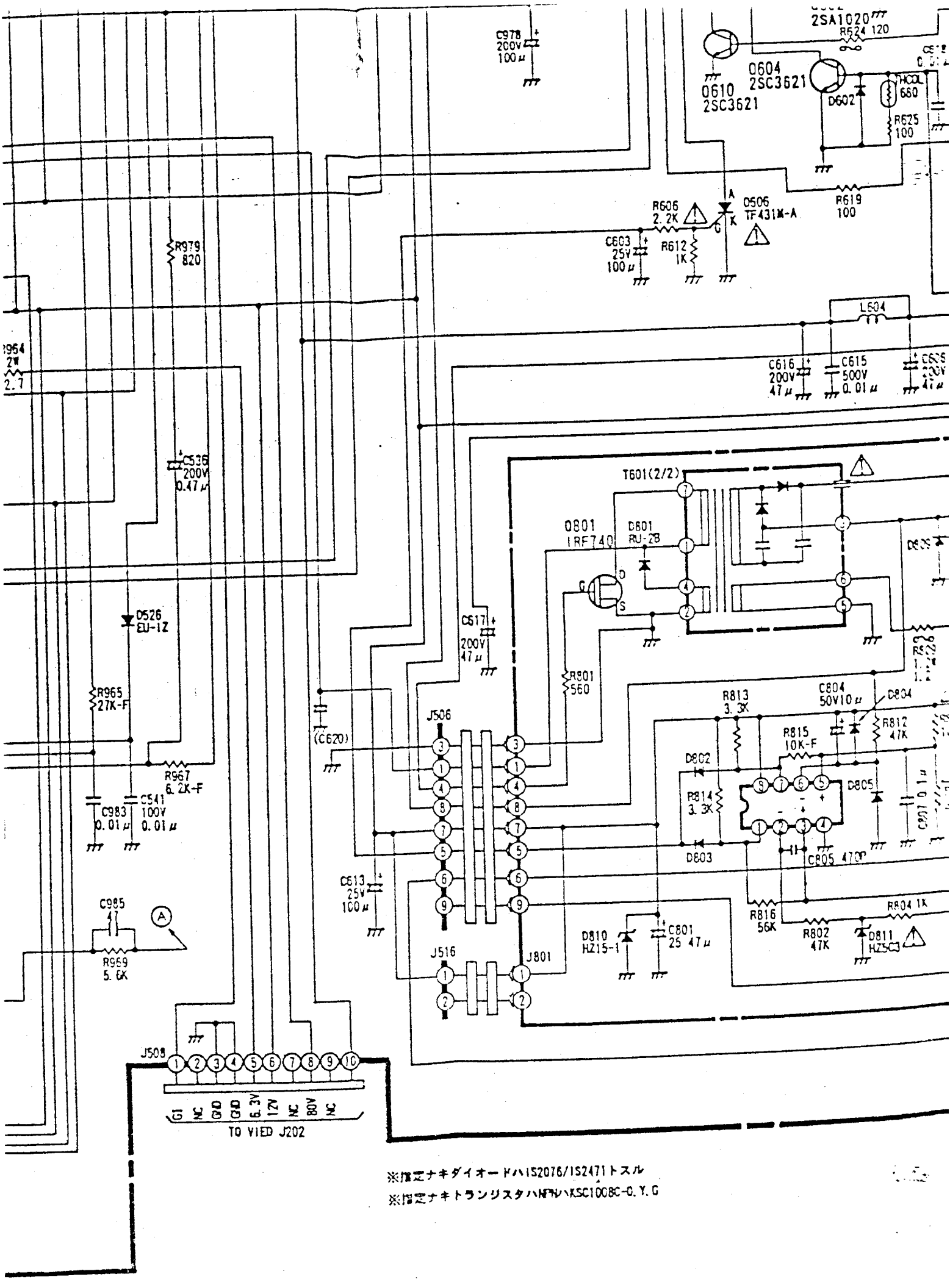

H
V
C513 2KV 100P
C514 500V 1500P
C575 2K 100P
C578 100V 1000P
D502 EG-1
R589 1/2W 560
R587 1K
Q521 2SC2274
R547 1W 12
L507 1mH
L505
R542 4.7K 1W
VR502 2W B100
SW501
R572 1/2 1.2
L504 10mH
Q501 IRF9620
L502 M3R2
D505 HZ11B3
D506 HZ11B3
C537 0.1μ 250V
R534 1/2W 100K
C524 200V 0.15μ
C523 200V 0.39μ
C522 200V 0.82μ
Q514 IRF634
Q513 IRF634
Q512 IRF634
D513 HZ16-1
D514 HZ16-1
D515 HZ16-1
C527 0.01μ
C528 0.01μ
C529 0.01μ
D609
R622 10K
Q611 K982
C978 200V 100μ
R601 1W 390
C601 0.1μ
Q601 C2655
R602 680
L601 Z3F 5040
R604 2.2K
Q602 2SA1020
R624 120
Q610 2SC3621
Q604 2SC3621
C618 0.01μ
D602
HOOL 680
R625 100
R606 2.2K
Q606 TF431K-A
R619 100
C603 25V 100μ
R612 1K
R979 820
L504
C616 200V 47μ
C615 500V 0.01μ
C606 200V 47μ
C536 200V 0.47μ
T601(2/2)
Q801 IRF740
D801 RU-2B
D809


L507 1mH
L505
C577 2K 6BP
RY501 AJG3241
D517
R598 3W 56
L506 68μ
R572 1/2 1.2
L504 10mH
R576 1M
R575 4.7K
C580 25V 220μ
Q518 2SC 2274
Q517
D528 HZ12-C3
R574 47K
R573 4.7K
C523 200V 0.39μ
C522 200V 0.82μ
C521 200V 0.82μ
C525 200V 0.12μ
C526 200V 0.12μ
C583 200V 0.12μ
C584 200V 0.12μ
Q513 IRF634
Q512 IRF634
Q511 IRF634
Q510
R540 10K
D529
D514 HZ16-1
D515 HZ16-1
D516 HZ16-1
C528 0.01μ
C529 0.01μ
C530 0.01μ
C531 0.01μ
R541 39K
J502
CS1
CS2
CS3
CS4
AFC1
AFC2
GND
H-LIN
CR
FAN-OUT
TO CONT J102
C514 0.1μ
Q601 C2655
C601 0.1μ
R602 680
L601 2SF 504D
Q603 IRF740
L603
L602 2SF 504D
R621 39
R604 2.2K
D601 EU-1Z
R623 1W 0.22
Q602 2SA1020
R624 120
T501(1/2)
ANODE
FOCUS(D)
FOCUS(S)
DYNAMIC-IN
SCREEN
Q604 2SC3621
D602
HCOL 680
R625 100
C618 0.01μ
C607 630V 6800P
C608 630V 2200P
D605 RU2B
Q605 IRF740
D604 HZ16-1
R619 100
R605 680 1/2W
(R620)
(D603)
L604
C616 200V 47μ
C615 500V 0.01μ
C606 200V 47μ
D606 RU2B
R608 1/2W 330
C609 50V 220μ
C610 0.1μ K
Q607 TL431 COMP
R609 39K
R614 1/2 220
VR601 30K HV-ADJ
R810 10K-F
TP1
D809
C802 50V 10μ
C808 0.33μ
D808 RU2B
R809
R817 33
C803
R613 1W 1K


PWB POWER-SUB
Q901
TM16615-L3
D901
KBV406H
C908
2200P
C907
2200P
C909
2200P
C910 0.01μ
R902
1/2W 1K
R903
2W
120
RT902
4Ω
C911
450V
220μ
C912
450V
220μ
R904
1/2W 150K
R905
1/2W 150K
RT901
16 Ω
C913
4700P
C919
4700P
J903
PRIMARY
C951
4700P
C953
4700P
DG
RP901
150M
RY901
VB-12MB
Q951
R957
2.7K
R958
2W
47
C954
25V
220μ
C952
0.01μ
R956
10K
D951
SW 951
FREE RUN
FACTORY
RY901
20K680
R951
1W82
J901
J902
J904
J905
J107
SW 111
PWB-CONT.
J906
F901
21B 4A
AC
R901
1/2W
220K
R924
1/2W
220K
C903
0.56μ
L901
24.3mH
L902
8mH
C905
4700P
C904
0.33μ
FG1
C906
4700P
PRIMARY
J501
FAN-IN
DESUICE
FREE RUN
FACTORY

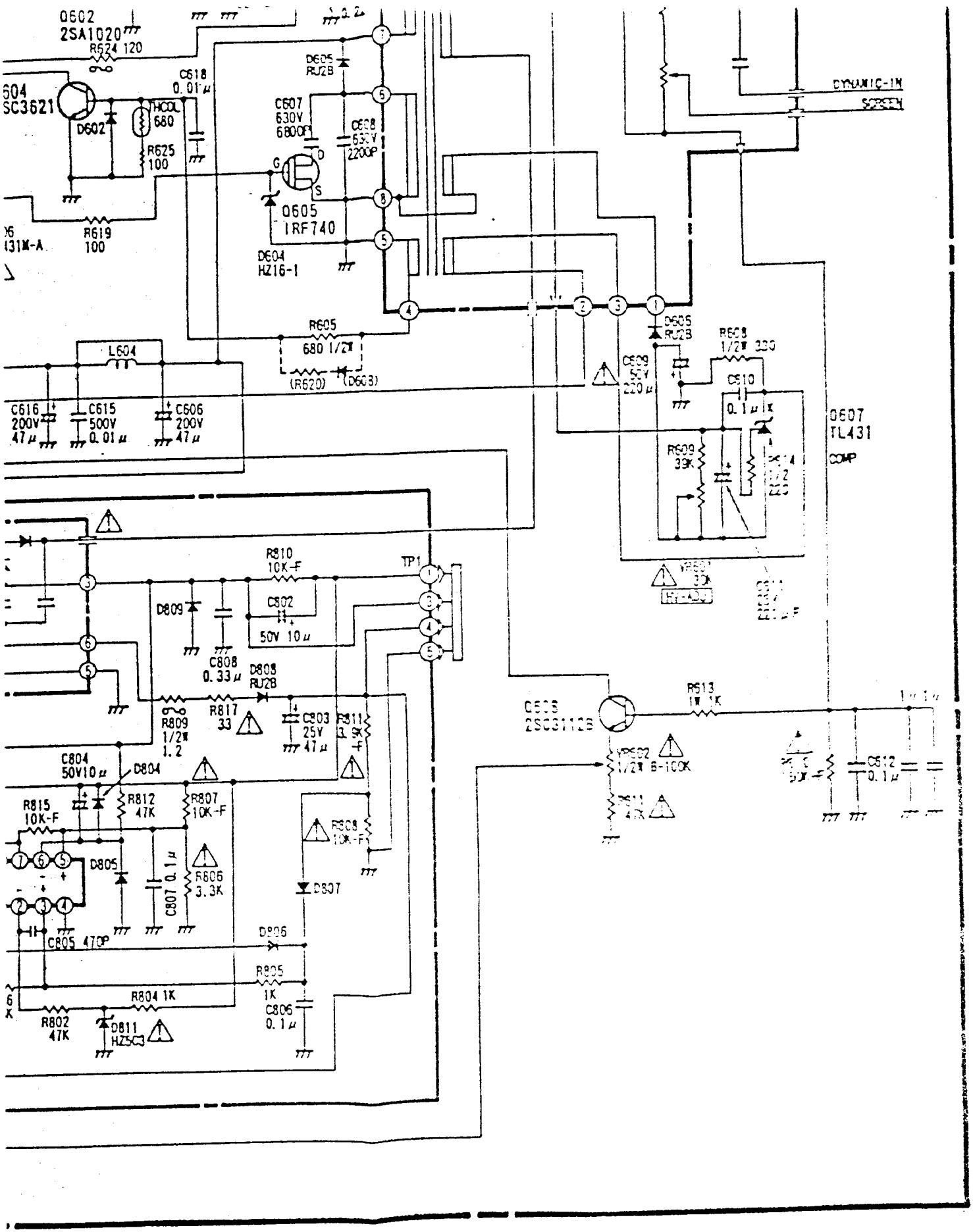

J903
J907
D902
R925 3W 100K
R926 3W 100K
C919 400V 0.1μ
R906 1/2W 150K
R908 470K
C901 630V 0.047μ
R907 1/2W 180K
R909 470K
C902 1KV SL270P
D908 RU-1P
C.T
IC901
STR S6308
Q901
L903 M3R2
C915 100V 0.015μ
R910 2W 15
R911 2W 15
L904 M3R2
C916 100V 68μ
D903 EG-1
D907 EG-1
R912 3W 12
R913 3W 12
R922 1/2W 1.2
R981 2W 2.2
C914 2KV 1500P
D904 EU1Z
R919 1.6K-F
D905 EU1Z
C917 25V 22μ
R920 2W 0.33
C918 2200P
IC902 TLP732LF2
O.C.P
R923 1/2W 47
R915 2W 0.33
R917 56K-F
R916 120
D906 HZ12C3
R921 2K-F
Q902 2SA1284
PRIMARY
C951 4700P
C953 4700P
R958 2W 47
C954 25V 220μ
SW 951
FREE RUN
FACTORY
J905
J509
J501
PRIMARY
FAN-IN
DESAUCE
FREE RUN
FACTORY
12V
-12V
5V
GND
GND
TO CONT. J101


IC956 SE140N
IC951 S13240C
IC952 L7812ML
IC953 μPC2405HF
IC954 μPC7912HF
IC902 TLP732LF2
IC955 917001
OVP
SIZE
DET2
24V
12V
Collector
V OUT
CLK-
Emitter
DET1
F/B
LOCK
OSC-OFF
OSC-ON
SOFT
GND
D908 RU-1P
D905 EU1Z
D526 EU-1Z
D954 EU2A
D955 RU4Z
D956 RU4YX
D957 RU4YX
D958 EU1Z
D959 RU3AM
D962 RU3AM
D966 X EU-1Z
R926 3W 100K
R981 2W 2.2
R921 2K-F
R974 1/2W1.2
R975 7.5K-F
R960 1/2W 27K
R961 1W 0.22
R964 2W 2.7
R965 27K-F
R966 47K-F
R967 6.2K-F
R968 10K-F
R969 5.6K
R970 100
R971 68K-F
R972 43K-F
R973 1K
C955 200V 220μ
C956 200V 100μ
C957 100V 470μ
C958 50V 470μ
C959 50V 47μ
C960 0.01μ
C961 50V 47μ
C962 0.01μ
C963 25V 1000μ
C964 25V 100μ
C965 0.01μ
C966 0.01μ
C967 10V 2200μ
C968 25V 47μ
C969 0.01μ
C970 0.01μ
C971 25V 47μ
C972 25V 220μ
C973 0.01μ
C974 0.01μ
C975 25V 47μ
C976 10V 1000μ
C977 250V 0.1μ
C979 50V 47μ
C980 50V 22μ
C981 25V100μ
C982 0.1μ
C983 0.01μ
C984 0.033μ
C985 47
C986 25V 47μ
C989 25V 47μ
L952 33μ
L953 33μ
L954 33μ
L958 33μ
L959 33μ
L960 M3R2
L961 M3R2
F951 3A
VR951 B3K
R959 10K
D961 MZ118B3
J508
A



※指定ナキダイオードハ1S2076/1S2471トスル

※指定ナキトランジスタハ無ハKSC1008C-O, Y, G



MODEL: TFS6705K

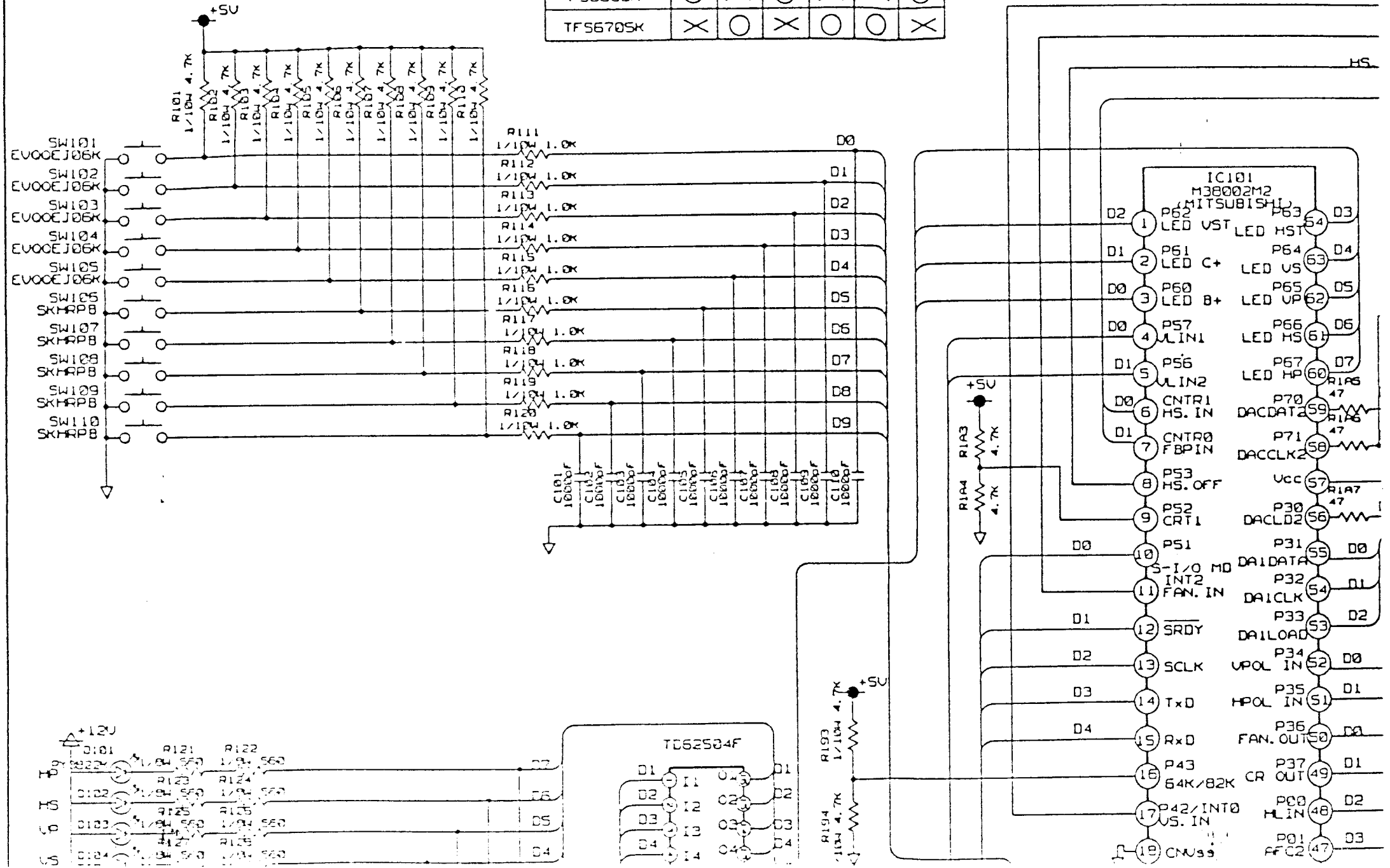
PCB - MAIN

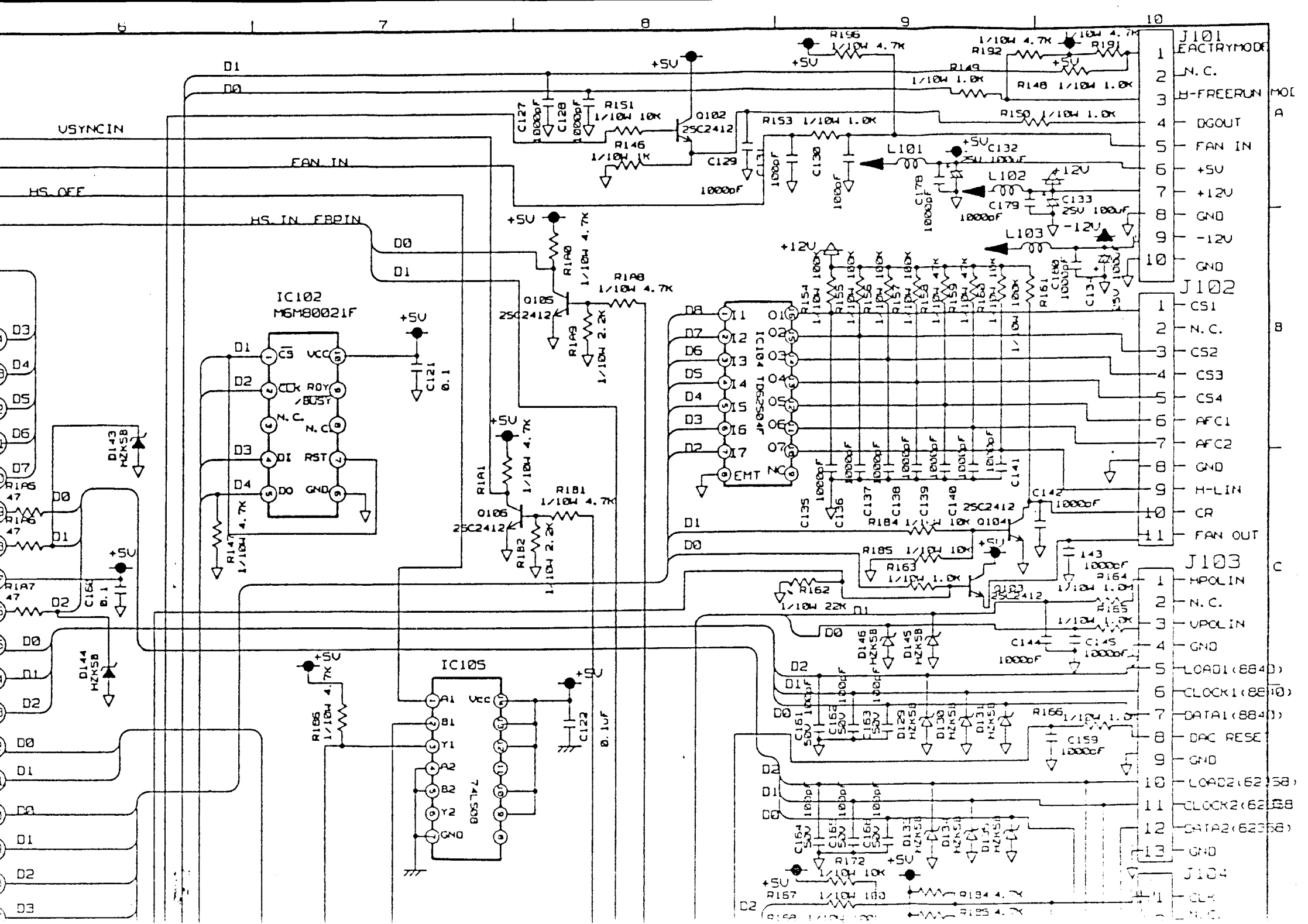
SCHEMATIC DIAGRAM

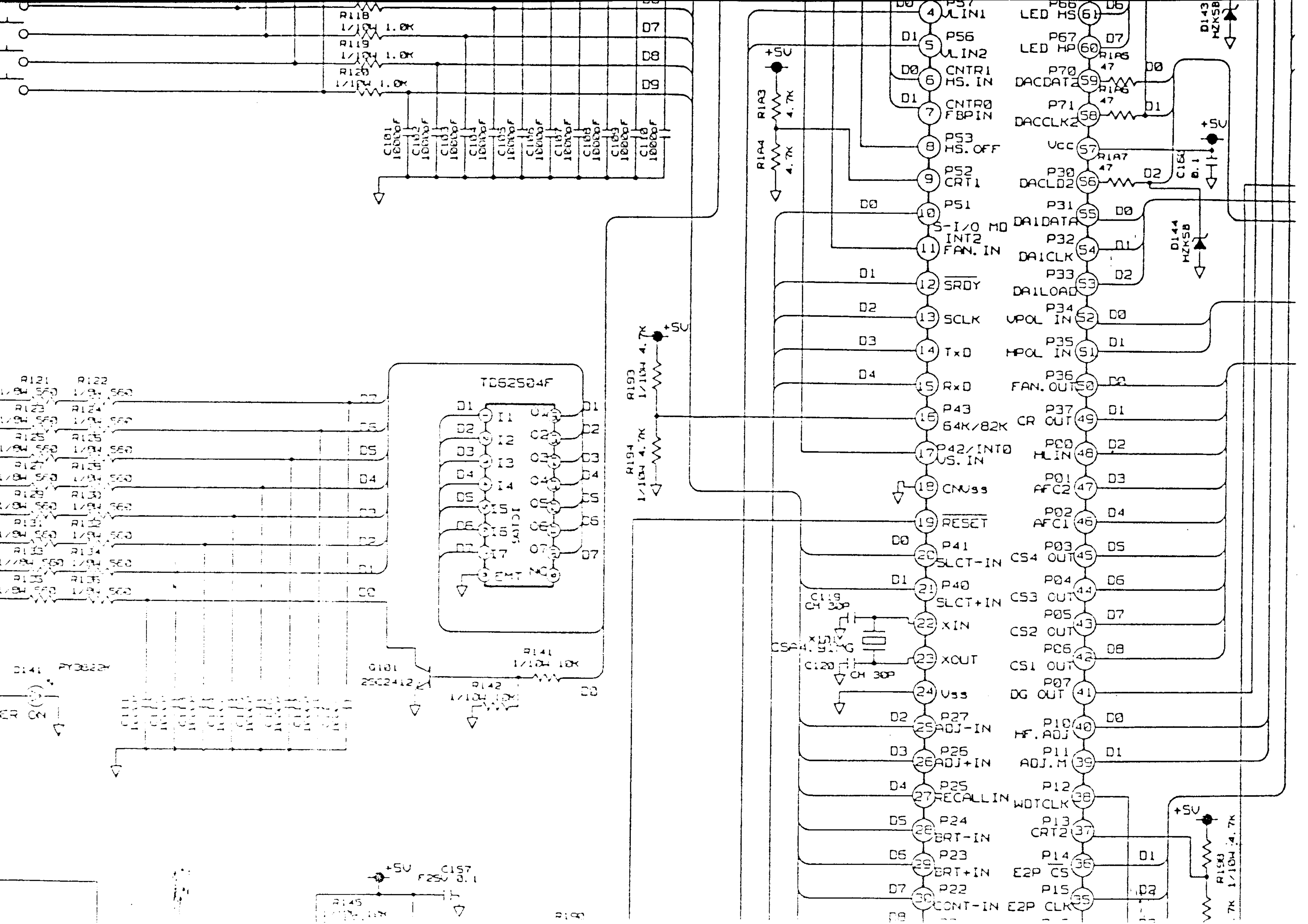
DWG NO.

Parts No. / MODEL	R193	R194	R198	R199	R1A3	R1A4
FS660SK	○	×	○	×	×	○
TFS670SK	×	○	×	○	○	×

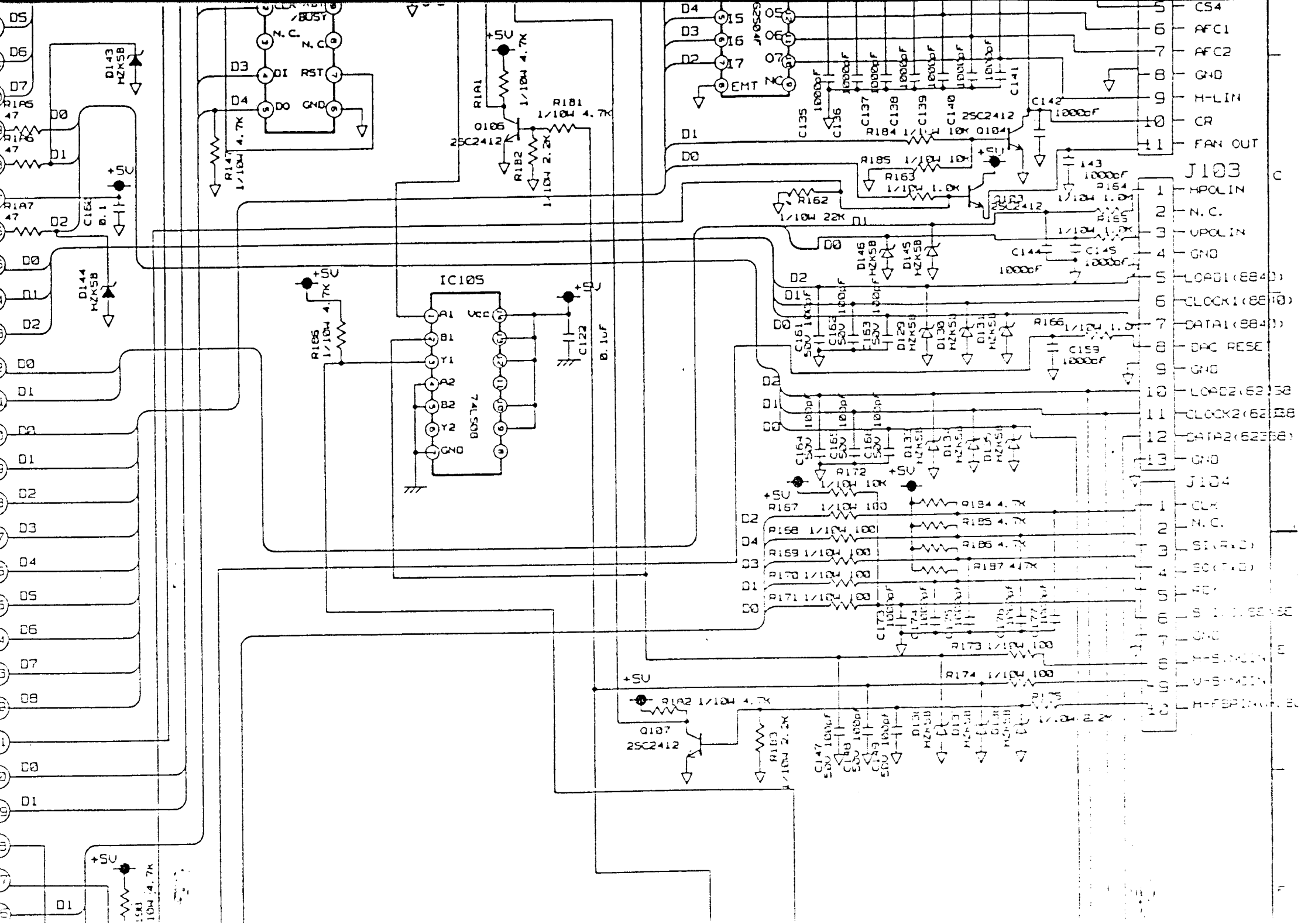
○ → Mounted
× → Not Mounted

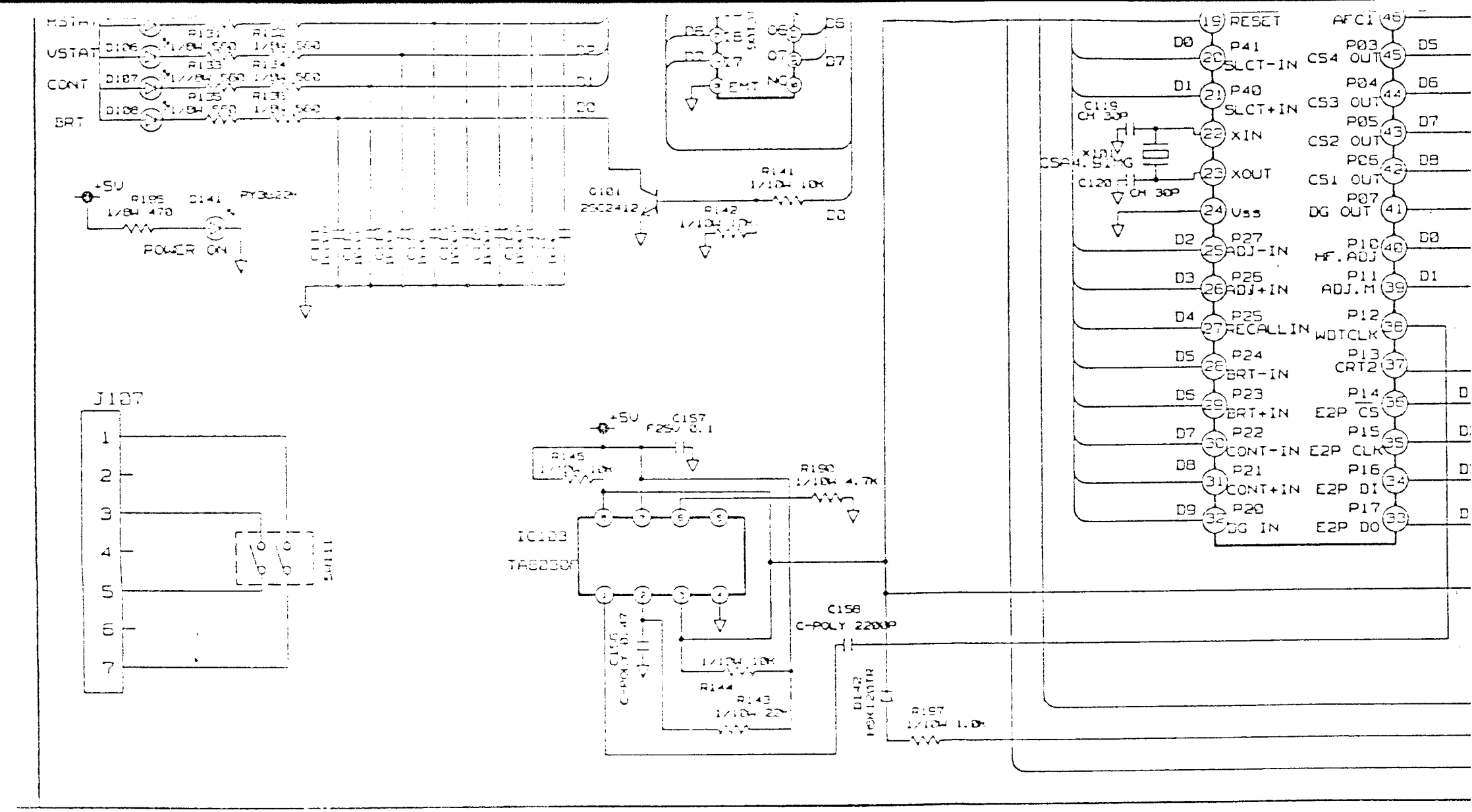



VSYNCIN
FAN IN
HS OFF
HS IN FBPIN
IC102
M6M80021F
IC104 TD62504F
IC105
74LS08
J101
J102
J103
J104
EACTRYMODE
N.C.
H-FREERUN
DGOUT
FAN IN
+5V
+12V
GND
-12V
CS1
CS2
CS3
CS4
AFC1
AFC2
H-LIN
CR
FAN OUT
HPOLIN
VPOLIN
LOAD1(8840)
CLOCK1(8840)
DATA1(8840)
DAC RESE
LOAD2(62358)
CLOCK2(62358)
DATA2(62358)
CLK
Q102 2SC2412
Q103 2SC2412
Q104 2SC2412
Q105 2SC2412
Q106 2SC2412



R118 1/10W 1.0K
R119 1/10W 1.0K
R120 1/10W 1.0K
D7
D8
D9
C101 1000pF
C102 1000pF
C103 1000pF
C104 1000pF
C105 1000pF
C106 1000pF
C107 1000pF
C108 1000pF
C109 1000pF
C110 1000pF
+5V
R1A3 4.7K
R1A4 4.7K
P57 LIN1
P56 LIN2
CNTR1 HS. IN
CNTR0 FBPIN
P53 HS. OFF
P52 CRT1
P51 S-I/O MD
INT2 FAN. IN
SRDY
SCLK
TxD
RxD
P43 64K/82K
P42/INT0 VS. IN
CNVss
RESET
P41 SLCT-IN
P40 SLCT+IN
XIN
XOUT
Vss
P27 ADJ-IN
P26 ADJ+IN
P25 RECALL IN
P24 BRT-IN
P23 BRT+IN
P22 CONT-IN
P66 LED HS
P67 LED HP
P70 DACDAT2
P71 DACCLK2
Vcc
P30 DACLD2
P31 DA1DATA
P32 DA1CLK
P33 DA1LOAD
P34 VPOL IN
P35 HPOL IN
P36 FAN. OUT
P37 CR OUT
P00 HLIN
P01 AFC2
P02 AFC1
P03 CS4 OUT
P04 CS3 OUT
P05 CS2 OUT
P06 CS1 OUT
P07 DG OUT
P10 HF. ADJ
P11 ADJ.M
P12 WDTCLK
P13 CRT2
P14 E2P CS
P15 E2P CLK
R1A5 47
R1A6 47
R1A7 47
C164 0.1
D143 HZK5B
D144 HZK5B
R193 1/10W 4.7K
R194 1/10W 4.7K
R198 1/10W 4.7K
C119 CH 30P
C120 CH 30P
X101 CSA4.91MG
TD62504F
IC103
EMT
NC
R121 1/8W 560
R122 1/8W 560
R123 1/8W 560
R124 1/8W 560
R125 1/8W 560
R126 1/8W 560
R127 1/8W 560
R128 1/8W 560
R129 1/8W 560
R130 1/8W 560
R131 1/8W 560
R132 1/8W 560
R133 1/8W 560
R134 1/8W 560
R135 1/8W 560
R136 1/8W 560
Q101 2SC2412
R141 1/10W 10K
R142 1/10W 10K
D141
ER ON
C157 F25V 0.1
R145

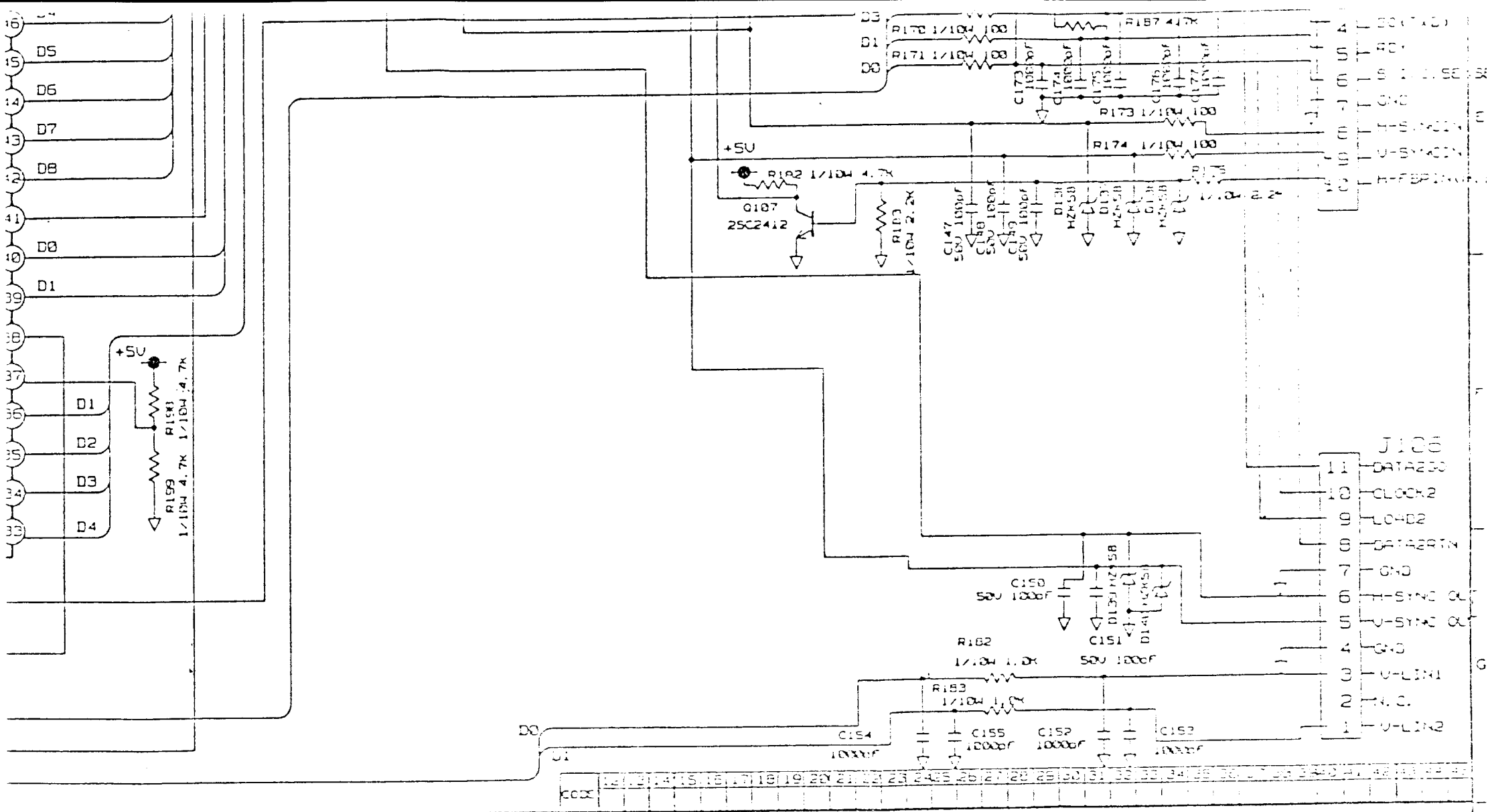

IC105
74LS08
J103
CS4
AFC1
AFC2
GND
H-LIN
CR
FAN OUT
HPOLIN
N.C.
VPOLIN
GND
LOAD1(8840)
CLOCK1(8840)
DATA1(8840)
DAC RESE
GND
LOAD2(6258
CLOCK2(6258
DATA2(6258
GND
J104
CLK
N.C.
SI(RxD)
SO(TxD)
+5V
R184 4.7K
R185 4.7K
R186 4.7K
R187 4.7K
R173 1/10W 100
R174 1/10W 100
Q187
2SC2412
R183
1/10W 2.2K
Q103
2SC2412
Q104
2SC2412
Q105
2SC2412
Q106
2SC2412
R162
1/10W 22K
R163
1/10W 1.0K
R164
1/10W 1.0K
R165
1/10W 1.0K
R166
1/10W 1.0K
R172
1/10W 10K
R185
1/10W 10K
R181
1/10W 4.7K
R182
1/10W 2.2K
R183
1/10W 2.2K
R184
1/10W 10K
C122
0.1uF
C142
10000pF
C143
10000pF
C144
10000pF
C145
10000pF
C159
10000pF
D143
MZK5B
D144
MZK5B
D145
MZK5B
D146
MZK5B



DEFINE

X_FIRST=0

X_STEP=SIZE


D5
D6
D7
D8
D0
D1
+5V
R181 1/10W 4.7K
R199 1/10W 4.7K
D1
D2
D3
D4
D3
D1
D0
R170 1/10W 100
R171 1/10W 100
R187 4.7K
C173 1000pF
C174 1000pF
C175 1000pF
C176 1000pF
C177 1000pF
R173 1/10W 100
R174 1/10W 100
+5V
R182 1/10W 4.7K
Q187 2SC2412
R183 1/10W 2.2K
C147 50V 1000pF
C148 50V 1000pF
C149 50V 1000pF
D138 MZ458
D139 MZ458
D140 MZ458
R175 1/10W 2.2K
J106
11 DATA2SD
10 CLOCK2
9 LOAD2
8 DATA2RTN
7 GND
6 H-SYNC OUT
5 V-SYNC OUT
4 GND
3 V-LIN1
2 N.C.
1 V-LIN2
C150 50V 1000pF
D137 MZ458
D141 MZ458
C151 50V 1000pF
R182 1/10W 1.8K
R183 1/10W 1K
C154 1000pF
C155 1000pF
C152 1000pF
C153 1000pF
D0
J1
CCCC
MITSUBISHI ELECTRIC CORPORATION
NAGASAKI WORKS
S CHASSIS FCB-CONTROL
DIM. IN mm
DATE 92. 4. 3
APPROVED
SCALE : NTS
DRAWN
CHECKED
DESIGNED
TITLE FS660SK/TFS660SK SCHEMATIC DIAGRAM
1/1