SERVICE MANUAL

AX3817UT

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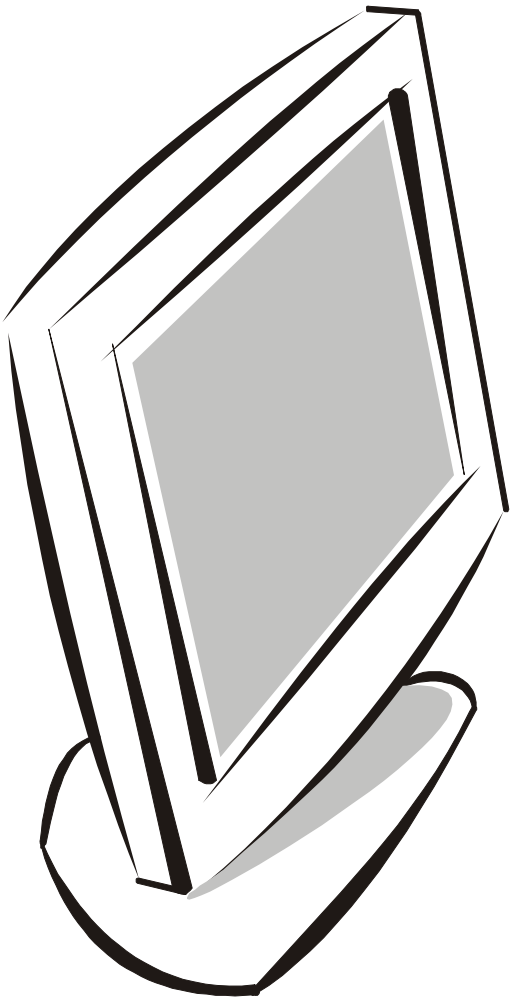
15" LCD Monitor



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1. SPECIFICATIONS FOR LCD MONITOR

1-1 General specifications General specifications

1. LCD-PANEL : USE HANNSTAR-SIP HSD150SX82
   Active display area 15 inches diagonal
   Pixel pitch 0.298 mm x 0.298 mm
   Pixel format 1024 x 768 RGB vertical stripe arrangement

2. Display Color :
   Panel display colors is 6-bit, 262144 colors , but we use Dithering to improve to 8 –bit, 16million colors

3. **External Controls :**
   Power button, MENU-key , Left & Right key, Auto key.
   Osd-menu control item :
   Contrast, Brightness, Black-level, Focus, Clock,
   H-position, V-position, Language, Color, Auto-Level ,Reset, Osd -Position, Exit.

4. Input Video Signal :
   Analog-signal 0.7Vpp
   Video signal termination impedance 75 OHM

5. Scanning Frequencies :
   Horizontal: 29 KHz - 60 KHz
   Vertical: 55 Hz – 75 Hz
   Pixel clock: 80 MHz

6. Factory Preset Timing : 18
   User Timings : 19
   Input signal tolerance : H tolerance ± 1 K, V tolerance ± 1 Hz

7. Power Source :
   Switching Mode Power Supply
   AC 100 – 240 V, 50/60 Hz Universal Type

8. Operating Temperature : 0°C - 50°C Ambient
   Non-operating Temperature : -20°C - 60°C

9. Humidity :
   Operating : 20% to 80% RH (non-condensing)
   Non Operating : 5% to 95%RH (38.7°C maximum wet bulb temperature)

10. Weight : 5.2 kg

11. External Connection : 15Pin D-type Connector, AC power-Cord

12. View Angle : x-axis right/left = 60, y-axis up/down = 45

13. Outside dimension : Width x Height x Thickness = 390mm x 385mm x 215mm

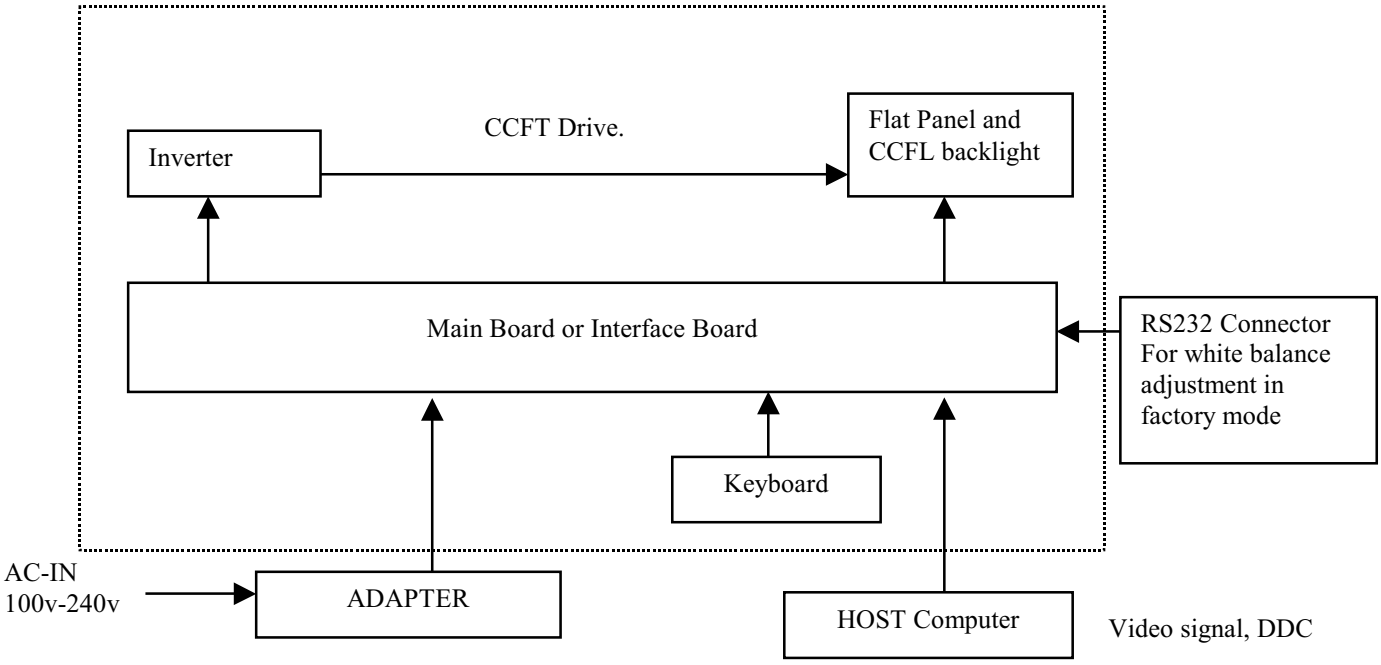
14. Plug and Play : VESA DDC1/DDC2B

15. Power saving : VESA DPMS

1-2 LCD MONITOR DESCRIPTION

The LCD MONITOR will contain an main board, an Inverter module, keyboard and External Adapter which house the flat panel control logic, brightness control logic, DDC and DC-DC conversion
The Inverter module will drive the backlight of panel .
The Adapter will provides the 12V DC-power 5 Amp to Main-board and Inverter module .

Monitor Block Diagram



1-3 Interface Connectors

(A) AC-Power Cable
(B) Video Signal Connectors and Cable
(C) External Adapter

2. PRECAUTIONS AND NOTICES

2-1 ASSEMBLY PRECAUTION

(1) Please do not press or scratch LCD panel surface with anything hard. And do not soil LCD panel surface by touching with bare hands (Polarizer film, surface of LCD panel is easy to be flawed)
In the LCD panel, the gap between two glass plates is kept perfectly even to maintain display characteristic and reliability. If this panel is subject to hard pressing, the following occurs :
(a) Uniform color (b) Orientation of liquid crystal becomes disorder
(2) Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.
(3) Please wipe out drops of adhesive like saliva and water in LCD panel surface immediately.
They might damage to cause panel surface variation and color change.
(4) Do not apply any strong mechanical shock to the LCD panel.

2-2 OPERATING PRECAUTIONS

(1) Please be sure to unplug the power cord before remove the back-cover. (be sure the power is turn-off)
(2) Please do not change variable resistance settings in MAIN-BOARD, they are adjusted to the most suitable value. If they are changed, it might happen LUMINANCE does not satisfy the white balance spec.
(3) Please consider that LCD backlight takes longer time to become stable of radiation characteristic in low temperature than in room temperature.
(4) Please pay attention to displaying the same pattern for very long-time. Image might stick on LCD.

2-3 STORAGE PRECAUTIONS

(1) When you store LCD for a long time, it is recommended to keep the temperature between 0℃-40℃ without the exposure of sunlight and to keep the humidity less than 90% RH.
(2) Please do not leave the LCD in the environment of high humidity and high temperature such as 60℃ 90%RH.
(3) Please do not leave the LCD in the environment of low temperature; below -15℃.

2-4 HIGH VOLTAGE WARNING

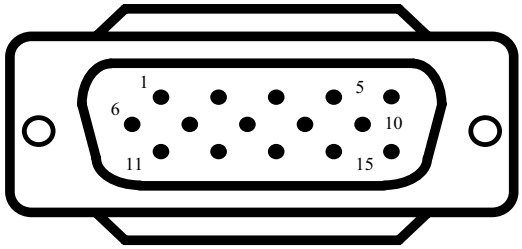
The high voltage was only generated by INVERTER module, if carelessly contacted the transformer on this module, can cause a serious shock. (the lamp voltage after stable around 600V, with lamp current around 8mA, and the lamp starting voltage was around 1500V, at Ta=25℃)

3. OPERATING INSTRUCTIONS

This procedure gives you instructions for installing and using the LCD monitor display.

1. Position the display on the desired operation and plug–in the power cord into External Adapter AC outlet. Three-wire power cord must be shielded and is provided as a safety precaution as it connects the chassis and cabinet to the electrical conduct ground. If the AC outlet in your location does not have provisions for the grounded type plug, the installer should attach the proper adapter to ensure a safe ground potential.

2. Connect the 15-pin color display shielded signal cable to your signal system device and lock both screws on the connector to ensure firm grounding. The connector information is as follow:



15 - Pin Color Display Signal Cable

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1.	RED	9.	5V power from VGA-card
2.	GREEN	10.	GND
3.	BLUE	11.	SYNC. GND
4.	GND	12.	SDA
5.	GND	13.	HORIZ. SYNC
6.	GND-R	14.	VERT. SYNC
7.	GND-G	15.	SCL
8.	GND-B		

3. Apply power to the display by turning the power switch to the "ON" position and allow about thirty seconds for Panel warm-up. The Power-On indicator lights when the display is on.
4. With proper signals feed to the display, a pattern or data should appear on the screen, adjust the brightness and contrast to the most pleasing display, or press auto-key to get the best picture-quality.
5. This monitor has power saving function following the VESA DPMS. Be sure to connect the signal cable to the PC.
6. If your LCD monitor requires service, it must be returned with the power cord & Adapter.

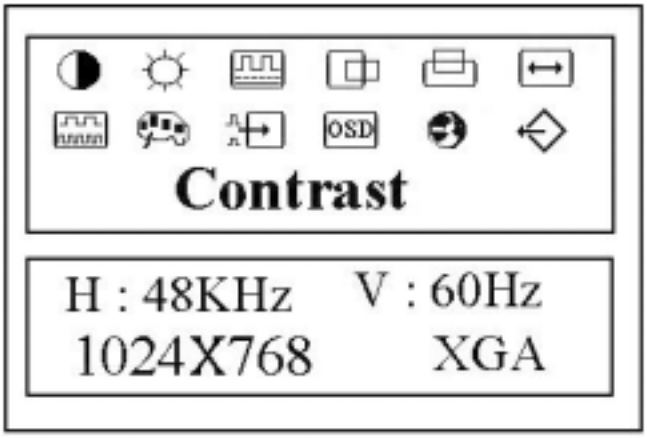
4. ADJUSTMENT

4-1 ADJUSTMENT CONDITIONS AND PRECAUTIONS

Adjustments should be undertaken only on following function : contrast, brightness Black-level, focus, clock, h-position, v-position, Color, Auto-Level, Osd-Position, Language, Reset.

4-2 ADJUSTMENT METHOD

Press MENU button to activate OSD Menu or make a confirmation on desired function, Press Left/Right button to select the function or done the adjustment.



1. White-Balance, Luminance adjustment
   Approximately 30 minutes should be allowed for warm up before proceeding white balance adjustment.

   Before started adjust white balance ,please setting the Chroma-7120 **MEM. Channel 1 to 9300** color and **MEM. channel 2 to 7300** color, (our 9300 parameter is x = 281 ± 10, y = 311 ± 10, Y = 160 ± 5cd/m2 and 7300 parameter is x = 301 ± 10, y = 317 ± 10, Y = 160 ± 5 cd/m^2)

   How to setting MEM.channel you can reference to chroma 7120 user guide or simple use " **SC**" key and " **NEXT**" key to modify xyY value and use "**ID**" key to modify the TEXT description

   Following is the procedure to do white-balance adjust

   Press MENU button during 2 seconds along with plug in the DC-power cord will activate the factory mode, and the OSD screen will located at **left top of panel**, and the **OSD-Position** ICON OSD will change to black-level2 symbol, when you move the cursor right on it

   I. <u>Bias (Low luminance) adjustment :</u>

   1. Press " AUTO" button , and wait for message " Pass" ,Move the cursor to "OSD-position" icon OSD , Check the Black-level2 value on OSD should be large than 30, if less than 30 that means the offset calculation FAIL, please manual adjust the blacklevel2 to value 43
   2. set the contrast (Icon 1) and black-level (Icon 3) to **maximal** value , and user RGB to "**50**".
   3. adjust the **Brightness** until chroma 7120 measurement reach the value Y=210 cd/m^2 ± 5 cd/m^2

II. Gain adjustment :

a. Adjust 9300 color-temperature

4. Set the Contrast to 30, Black-level  to 50
5. Switch the chroma-7120 to **RGB-mode** (with press "MODE" button)
6. switch the MEM.channel to Channel 01 (with up or down arrow on chroma 7120)
7. The lcd-indicator on chroma 7120 will show x = 281 ± 10, y = 311 ± 10, Y = 160 ± 5 cd/m^2
8. Adjust the RED on OSD window until chroma 7120 indicator reached the value R=100
9. adjust the GREEN on OSD, until chroma 7120 indicator reached G=100
10. adjust the BLUE on OSD, until chroma 7120 indicator reached B=100
11. repeat above procedure (item 8,9,10) until chroma 7120 RGB value meet the tolence =100± 2
12. Press 93 on OSD window to save the adjustment result

b. adjust 7300 color-temperature

1 Set the Contrast to 35, Black-level  to 50
2 Switch the chroma-7120 to **RGB-mode** (with press "MODE" button)
3 switch the MEM.channel to Channel 02 (with up or down arrow on chroma 7120)
4 The lcd-indicator on chroma 7120 will show x = 301 ± 10, y = 317 ± 10, Y = 160 ± 5 cd/m^2
5 Adjust the RED on OSD window until chroma 7120 indicator reached the value R=100
6 adjust the GREEN on OSD, until chroma 7120 indicator reached G=100
7 adjust the BLUE on OSD, until chroma 7120 indicator reached B=100
8 repeat above procedure (item 5,6,7) until chroma 7120 RGB value meet the tolence =100 ± 2

9 Press 73 on OSD window to save the adjustment result

Turn the POWER-button off to on to quit from factory mode (at USER-mode, the OSD window location will placed at middle of screen)

2. Clock adjustment
   Set the Chroma at pattern 63 (cross-talk pattern) or WIN98/95 shut-down mode (dot-pattern).
   Adjust until the vertical-Stripe-shadow as wide as possible or no visible.
   This function is adjust the PLL divider of ADC to generate an accurate pixel clock
   Example : Hsyn = 31.5KHz Pixel freq. = 25.175MHz (from VESA spec)
   The Divider number is (N) = (Pixel freq. x 1000)/Hsyn
   From this formula, we get the Divider number, if we fill this number in ADC register (divider register), the PLL of ADC will generate a clock which have same period with above Pixel freq.(25.175MHz) the accuracy of this clock will effect the size of screen.(this clock was called PIXEL-CLOCK)

3. Focus adjustment
   Set the Chroma at pattern 63 (cross talk pattern) or WIN98/95 shut down mode (dot-pattern).
   Adjust the horizontal interference as less as possible
   This function is adjust the phase shift of PIXEL-CLOCK to acquire the right pixel data .
   If the relationship of pixel data and pixel clock not so match, we will see the horizontal interference on screen ,we only find this phenomena in crosstalk pattern or dot pattern .

4. H/V-Position adjustment
   Set the Chroma to pattern 1 (crosshatch pattern) or WIN98/95 full-white pattern confirm above item 2 & 3 functions (clock & focus) was done well, if that 2 functions failed, the H/V position will be failed too.
   Adjust the four edge until all four-edges are visible at the edge of screen.

5. MULTI-LANGUAGE function
   There have 5 language for selection, press “MENU” to selected and confirm , press “ LEFT” or “ RIGHT” to change the kind of language (English , Deutch , Francais, Espanol, Italian)

6. Auto-Level Function
   Automatically Adjust Contrast & RGB to appropriate value according to INPUT RGB level

7. OSD-Position Function
   there is 5 location selectable for OSD-position.

8. Reset function
   Clear each old status of auto-configuration and re-do auto-configuration (for all mode)
   This function also recall 7800 color-temperature , if the monitor status was in “ Factory-mode” this reset function will clear Power-on counter (backlight counter) too.

9. OSD-LOCK function
   Press Left & Right key during switching on the monitor, the access to the OSD is locked, user only has access to “ Contrast, Brightness, Auto-key “.
   If the operator pressed the Left & Right during switching on the monitor again , the OSD is unlocked.

10. View Power-on counter and reset the Power-on counter(if not necessary , no suggest to entry factory mode)
    The Power-on counter was used to record how long the backlight of panel already working, the backlight life time was guarantee minimal 25000 hours, the maintainer can check the record only in factory mode.
    Press MENU button for 2 seconds along with plug-in DC power cord will be in factory mode, and the OSD screen will located at **left top of panel** but take cautions don’t press icon “93” & “73”, if you press 93/73 , your white-balance data will overlap with the new-one, and you must perform the white-balance process again.
    The result of counter was place at top of OSD, the maximal of record memory was 65000 hours, if exceed 65000 hours the counter will keep in 65000 hours until press “ RESET” at osd-menu in factory mode.
    The “ RESET” function in factory mode will execute following function:
    1. clear the Power-on counter to zero hours
    2. clear old auto-configuration status for all mode , so the monitor will automatically re-do auto-config when change to next mode or power on-off

11. Portrait mode for LCD Monitor
    Press “ Auto” button ,during switching on the monitor will activate / disactivated the OSD-PORTRAIT mode.

4-3 FRONT PANEL CONTROL KNOBS

Power button : Press to switch on or switch off the monitor.

Auto button : to perform the automatic adjustment from CLOCK, FOCUS, H/V POSITION, but no affect the color-temperature

Left/Right button : select function or do an adjustment.

MENU button : to activate the OSD window or to confirm the desired function

5. CIRCUIT-DESCRIPTION

5-1 SPECIAL FUNCTION with PRESS-KEY

A). press **Menu** button during 2 seconds along with **plug-in the DC Power cord**:
That operation will set the monitor into "Factory- mode", in Factory mode we can do the White balance adjustment with RS232 , and view the Backlight counter (this counter is use to record the panel activate hours ,for convenient the maintainer to check the panel backlight life time)
In Factory mode, OSD-screen will locate in left top of screen.
Press POWER-button off to on once will quit from factory mode and back to user-mode.

B). Press **both Left & Right button along with Power button** off to on once will activate the OSD-LOCK function, repeat this procedure will disable OSD-LOCK
In OSD-LOCK function, all OSD function will be lock , except Contrast and Brighness

OSD-INDEX EXPLANATION

1. **CABLE NOT CONNECTED**: Signal-cable not connected.

2. **INPUT NOT SUPPORT**:
   a. INPUT frequency out of range: H > 81kHz, v > 75Hz or H < 28kHz, v < 55Hz
   b. INPUT frequency out of VESA-spec. (out of tolerance too far)

3. **UNSUPPORT mode, try different Video-card Setting**:
   Input frequency out of tolerance, but still can catch-up by our system (if this message show, that means, this is new-user mode, AUTO-CONFIG will disable)

5-2 CHIPSET SIMPLE-INTRODUCTION

1. GMZAN1 (all-in-one chip solution for ADC, OSD, scalar and interpolation) :
   USE for computer graphics images to convert analog RGB data to digital data with interpolation process, zooming, generated the OSD font , perform overlay function and generate drive-timing for LCD-PANEL.

2. M6759 (ALI- MCU, type 8052 series with 64k Rom-size and 512 byte ram) :
   Use for calculate frequency, pixel-dot , detect change mode, rs232-communication, power-consumption control, OSD-index warning , …etc.

3. 24LC21 (MicroChip IC) :
   EePROM type, 1K ROM-SIZE, for saving DDC-CONTENT.

4. 24C04 (ATMEL IC) :
   EePROM type, 4K ROM-SIZE, for saving AUTO-config data, White-balance data, and Power-key status and Backlight-counter data.

5. LM2569S(NS brand switching regulator 12V to 5V with 3A load current) .

6. AIC 1084-33CM (AIC brand linear regulator 5V to 3.3V)

7. WFP4620D (timing Controller use Winbond)
   The WFP4620D is an integrated TFT-LCD timing controller,it provides the interface signal routing ,such as Source-IC start pulse and Gate-IC start pulse and Gate-IC pulse width which can adjustable by set the IO-input pin to high 3.3V or low level (Note: the Source & Gate-IC is resides on the flat panel)
   and some exchange function such as swap the output data bus between odd & even bus , swap high byte and low byte , this swapping function will convenient the PCB layout to the most shortest and smoothly way.
   And some Inversion function to reduce EMI

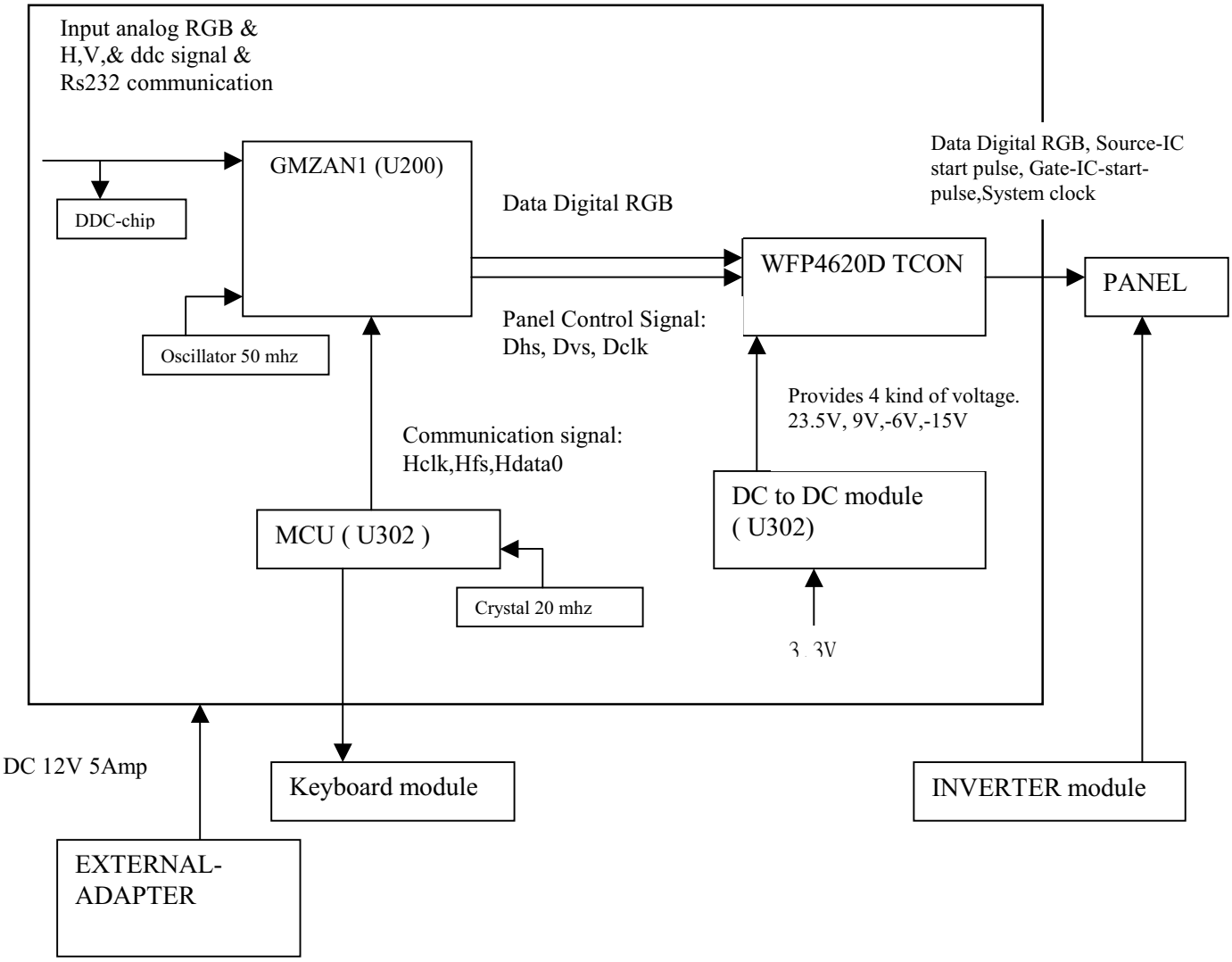
8. DC to DC module
   It convert the DC-3.3v to 4 level DC voltage which provide the panel power as follow :
   23.5V for Gate-IC turn on voltage , -6V for Gate-IC turn off , -15V for panel substrate compensate voltage, +9v for Source IC
   there is some start-up priority between those voltage, the first start-up voltage must be –15v, then –6v then +9V , and the last is +23.5V.

MODULE-TPYE COMPONENT :

1. ADAPTER : CONVERSION-module to convert AC 110V-240V to 12VDC, with 3.5 AMP for LCD Monitor and 12Vdc,3A + 9Vdc , 1A (Audio)

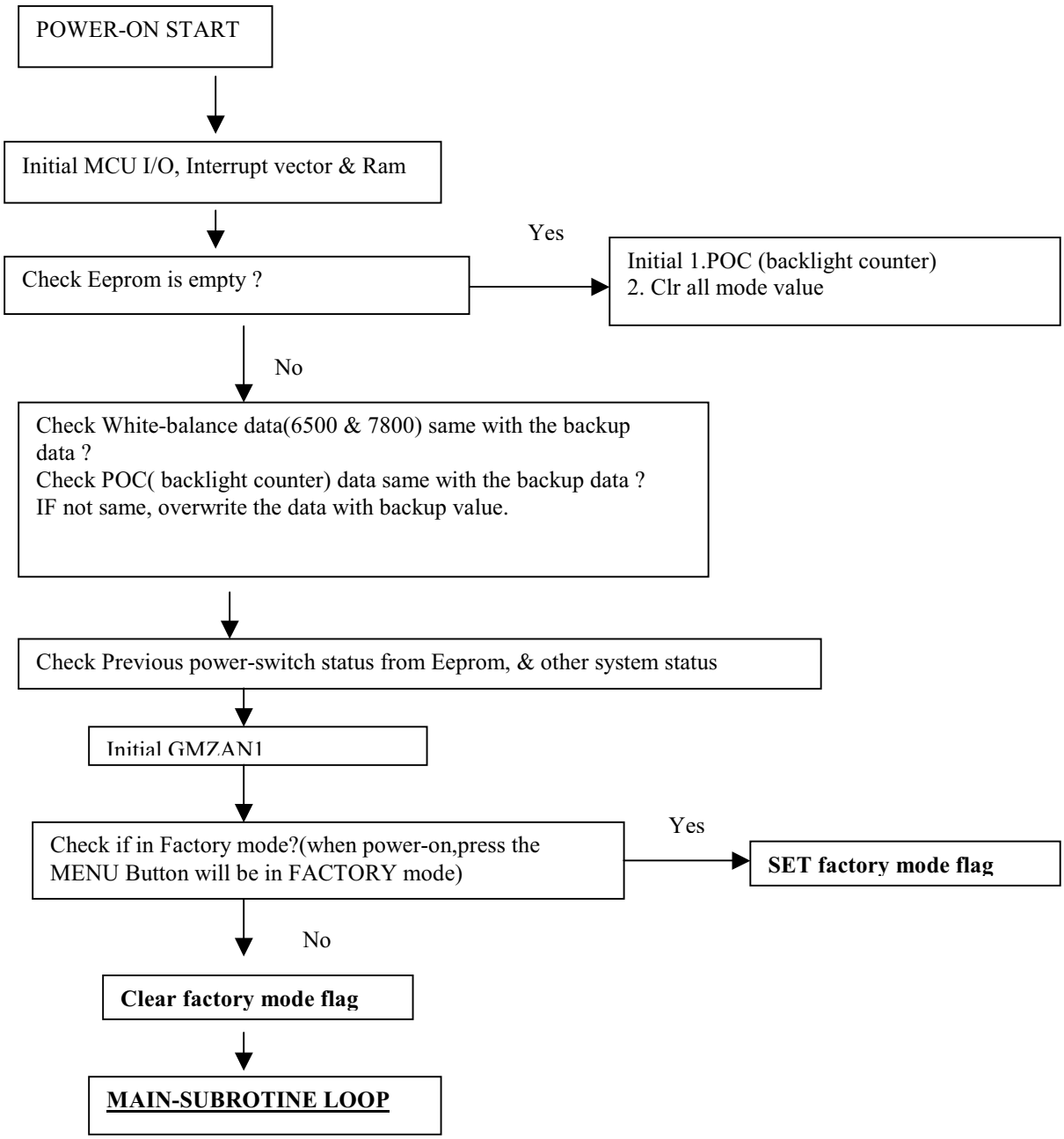
2. INVERTER : CONVERSION-module to convert DC 12V to High-Voltage around 1600V, with frequency 30K-60Khz,4mA-8Ma

Main-board Block diagram

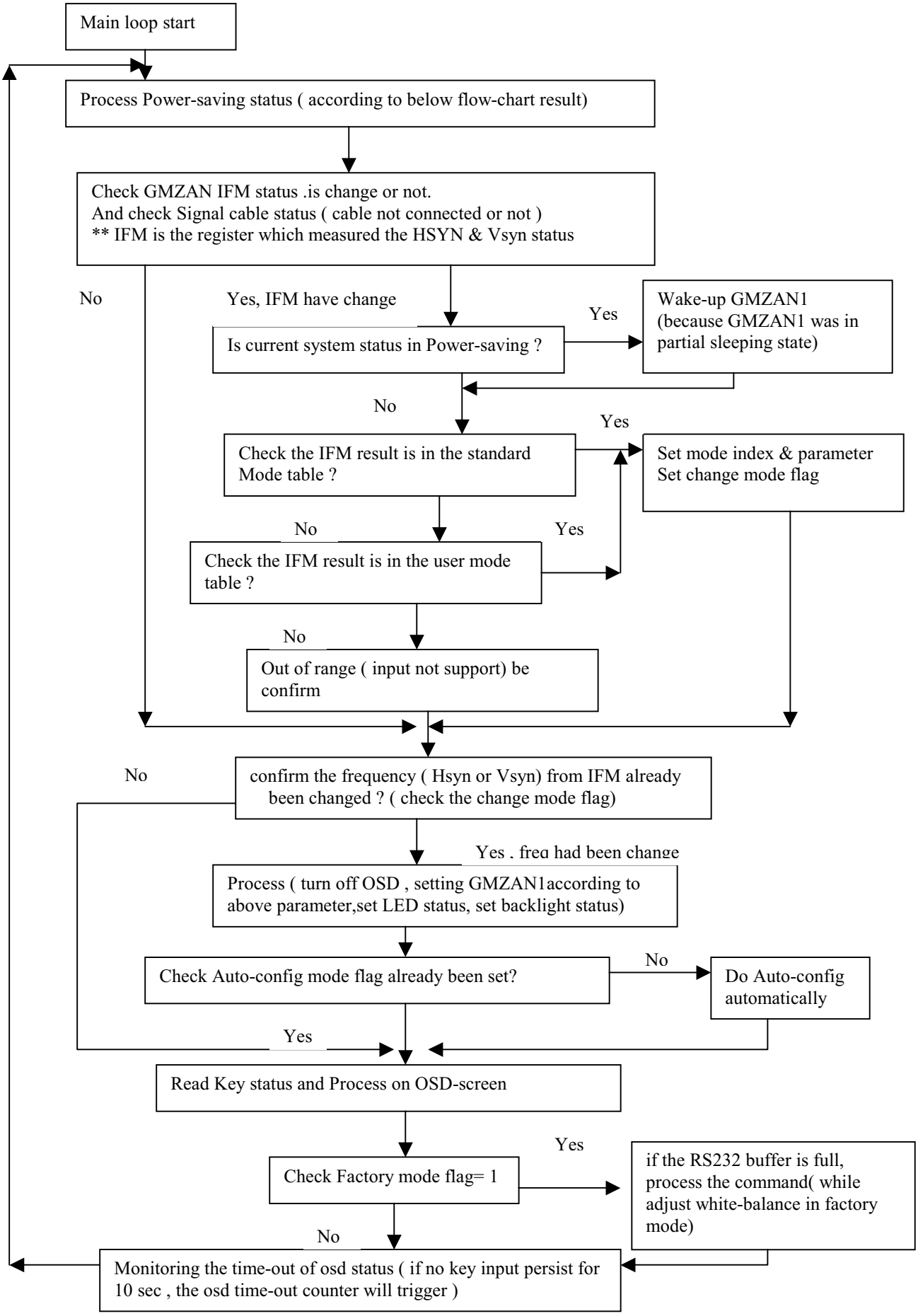


5-3 SOFTWARE FLOW CHART

I. Power-On Subrotine CHART



II. MAIN SUBROTINE LOOP

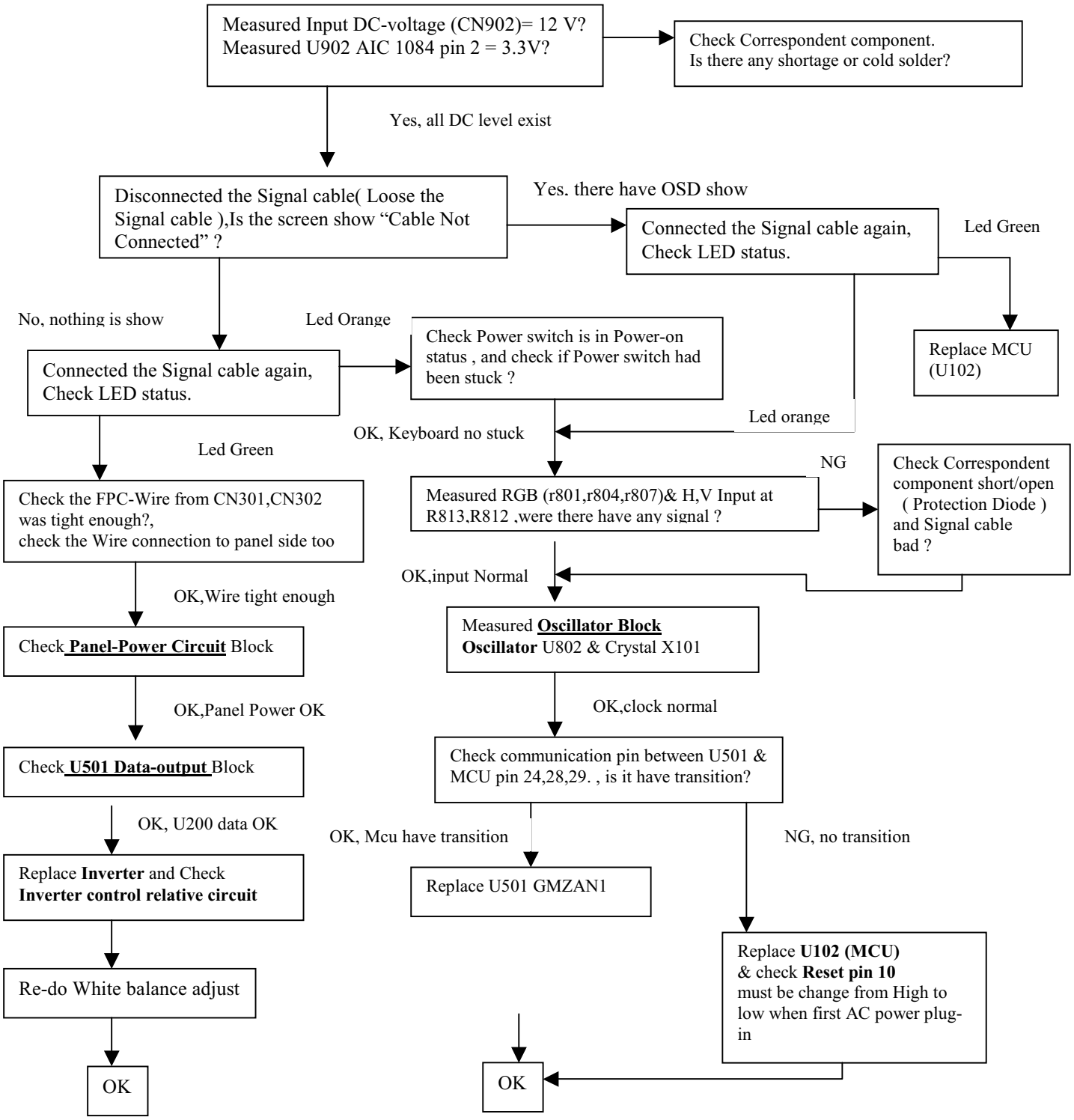


6. A). Interface-Board Trouble-Shooting chart

***Use the PC Win 98 white pattern, with some icon on it, and Change the Resolution to 640x480 60 Hz / 31 KHz**
****NOTICE : The free-running freq. of our system is 48 KHz / 60 Hz, so we recommend to use another resolution to do trouble shooting, this trouble shooting is proceed with 640x480 @60Hz 31Khz**

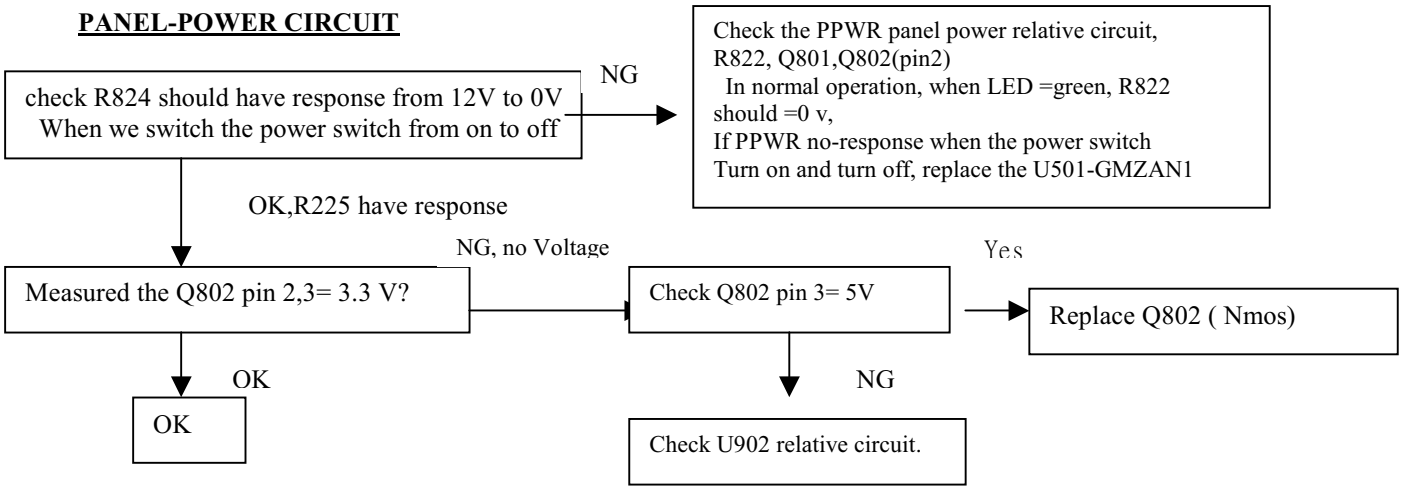
I. NO SCREEN APPEAR

DC-Power Part

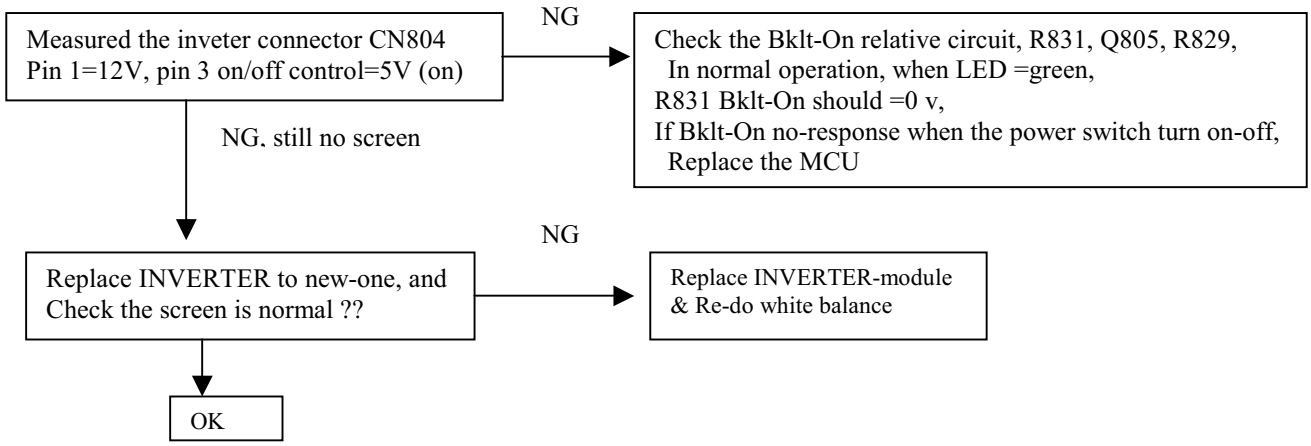


Note: 1. if Replace "**MAIN-BOARD**" , Please re-do "DDC-content" programmed & "WHITE-Balance".
2. if Replace " **INVERTER**" only, Please re-do " WHITE-Balance"

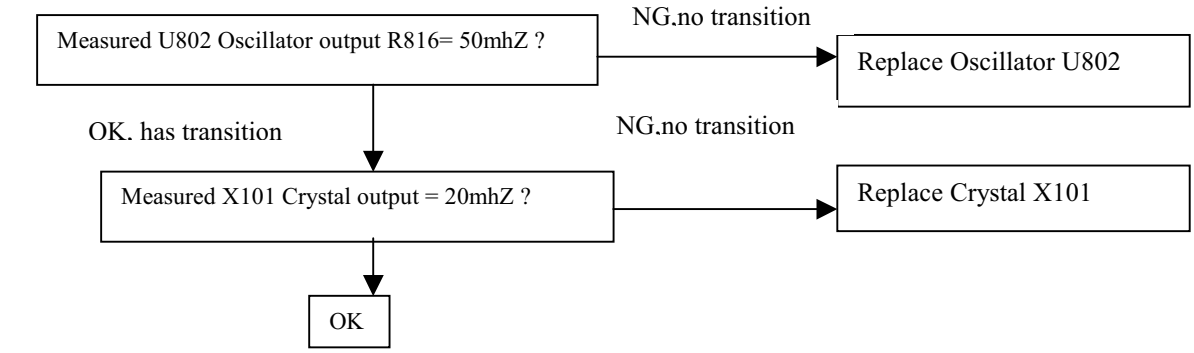
PANEL-POWER CIRCUIT



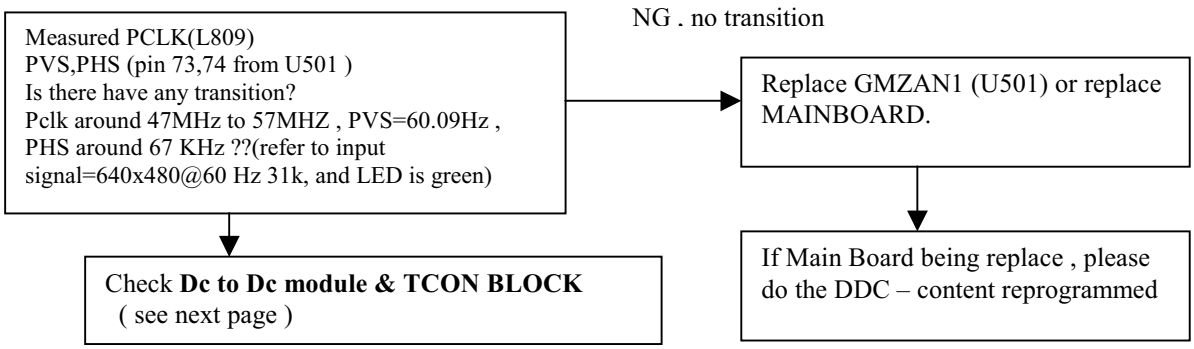
INVERTER Control Relative Circuit



OSCILLATOR BLOCK

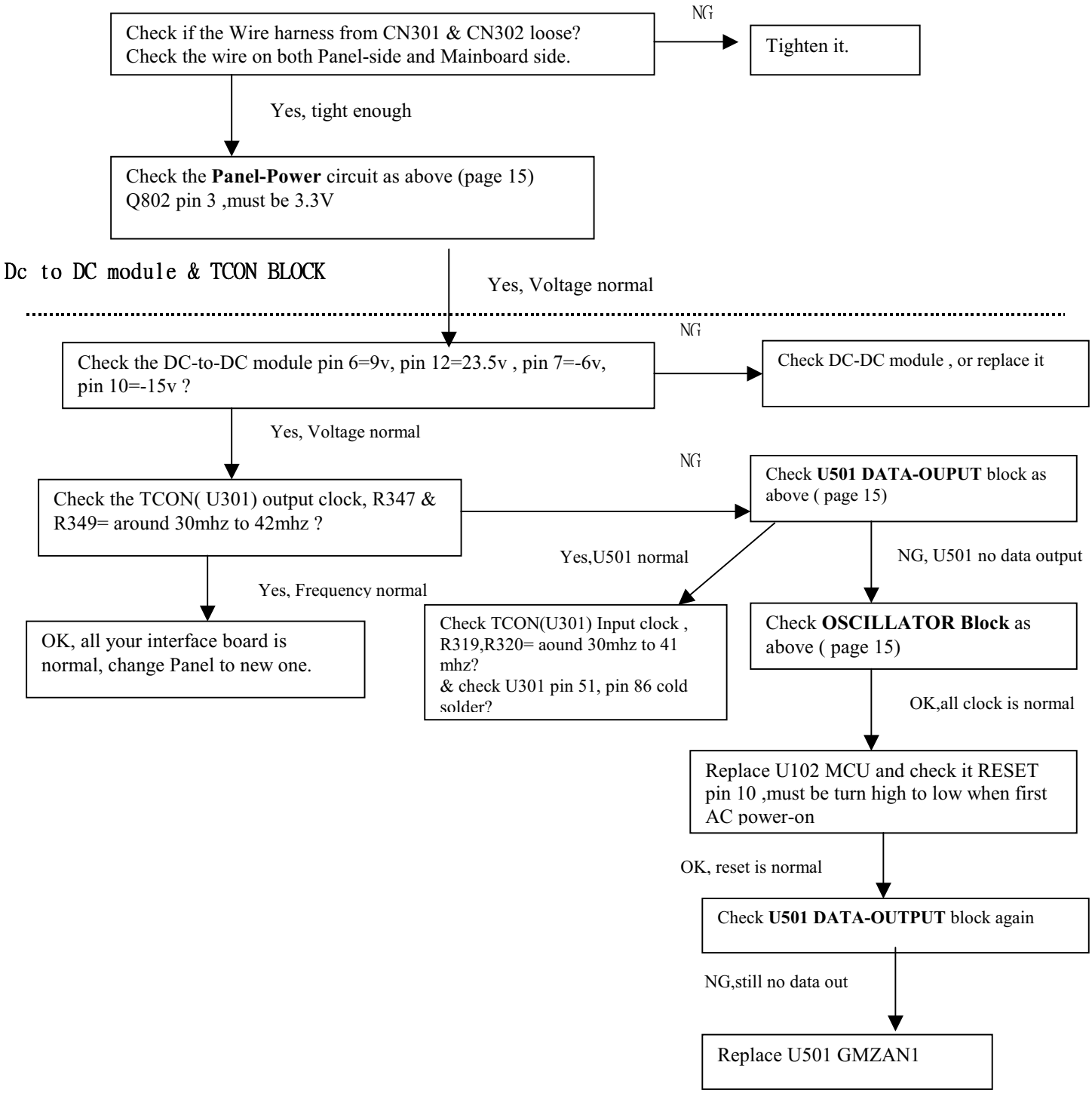


U501-DATA OUTPUT



II (a) THE SCREEN is Abnormal , stuck at white screen, OSD window can't appear, but keyboard & LED was normal operation.

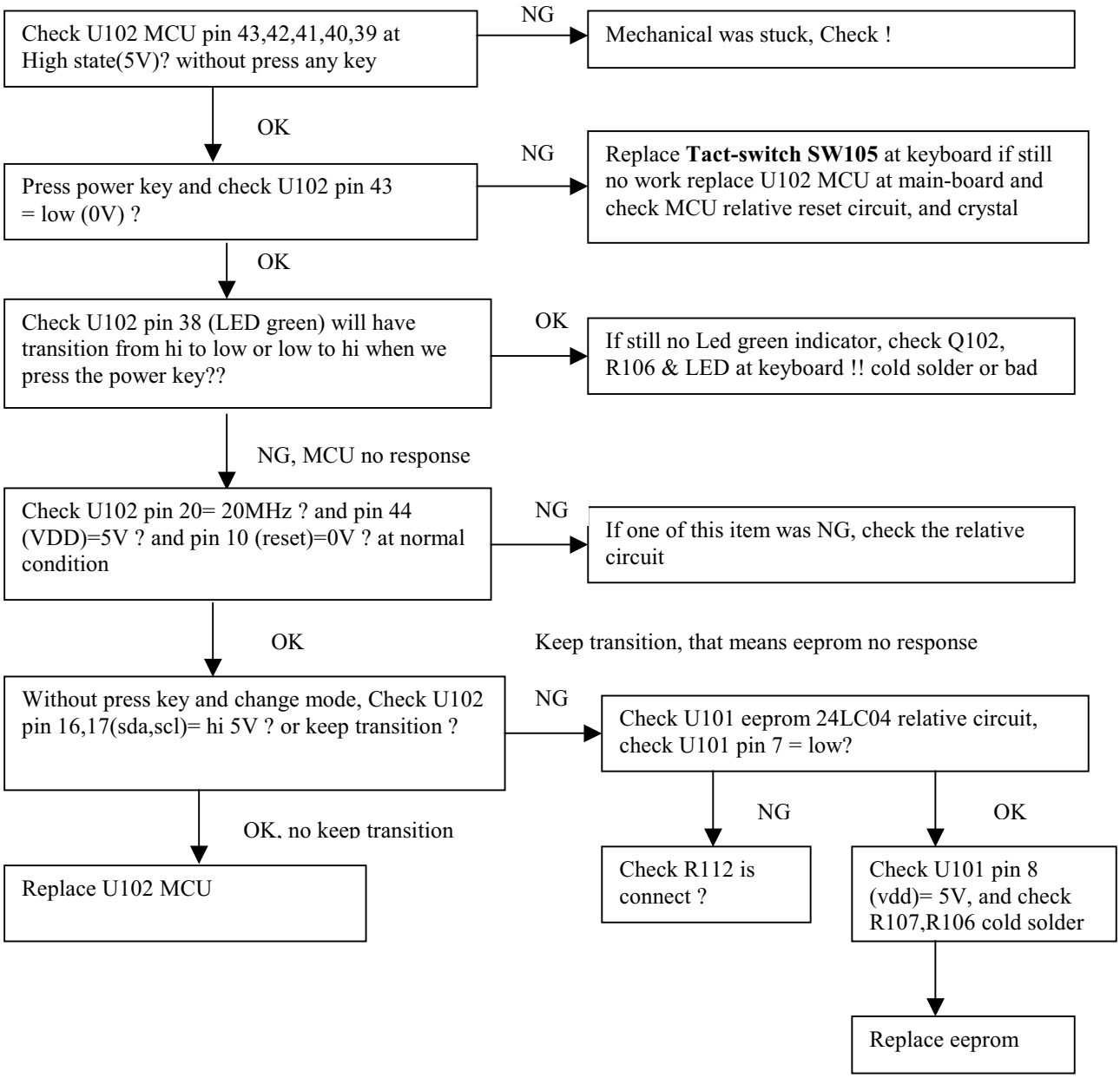
At general, this symptom is cause by missing panel data or panel power, so we must check our wire-harness which connected to panel or the panel power controller (U202)



II. (b)The screen had the Vertical Straight Line, might be stuck in Red, Green, Blue

That symptom is cause by bad Panel issue (might be the Source IC from Panel is cold solder or open loop) so REPLACE THE PANEL TO NEW ONE.

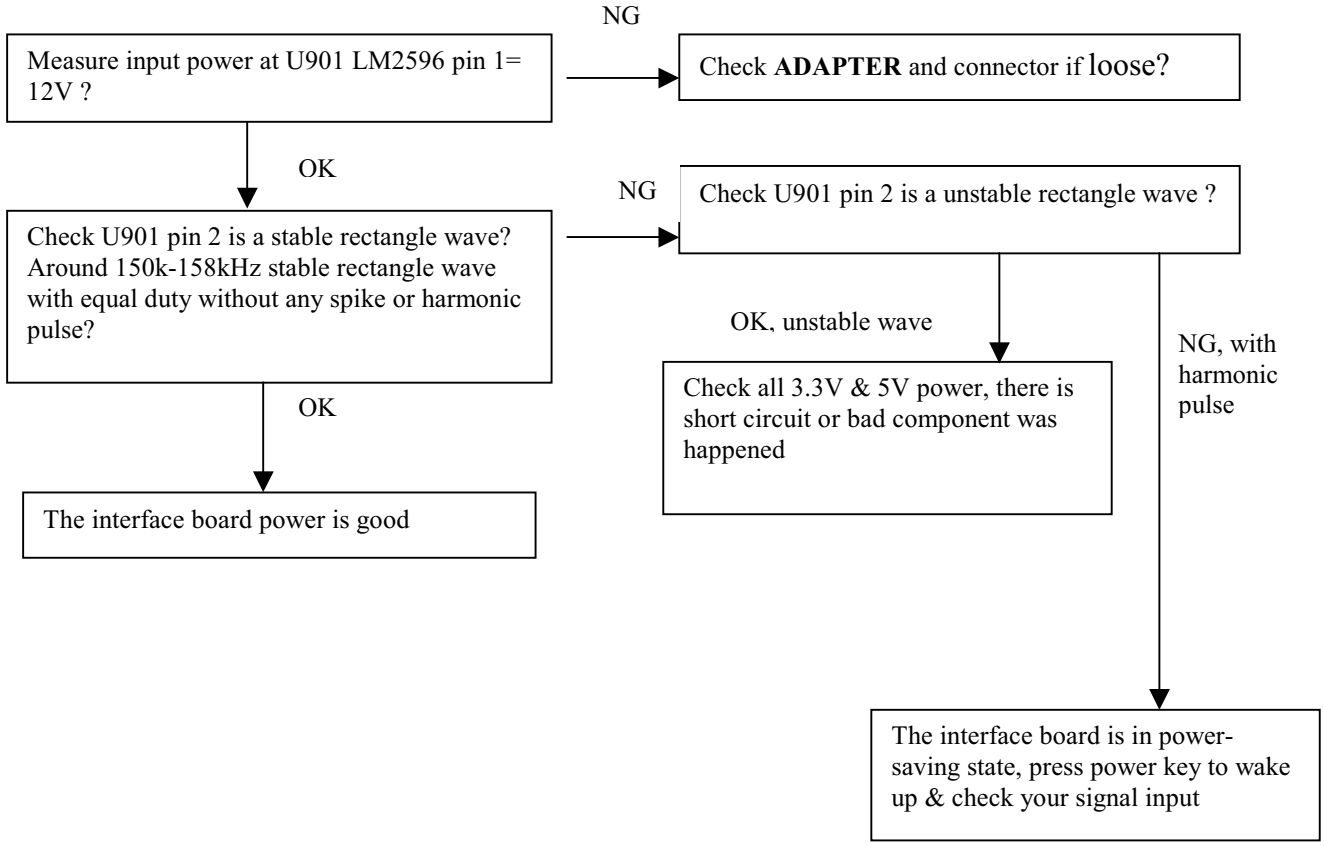
KEYBOARD BLOCK check



POWER-BLOCK check

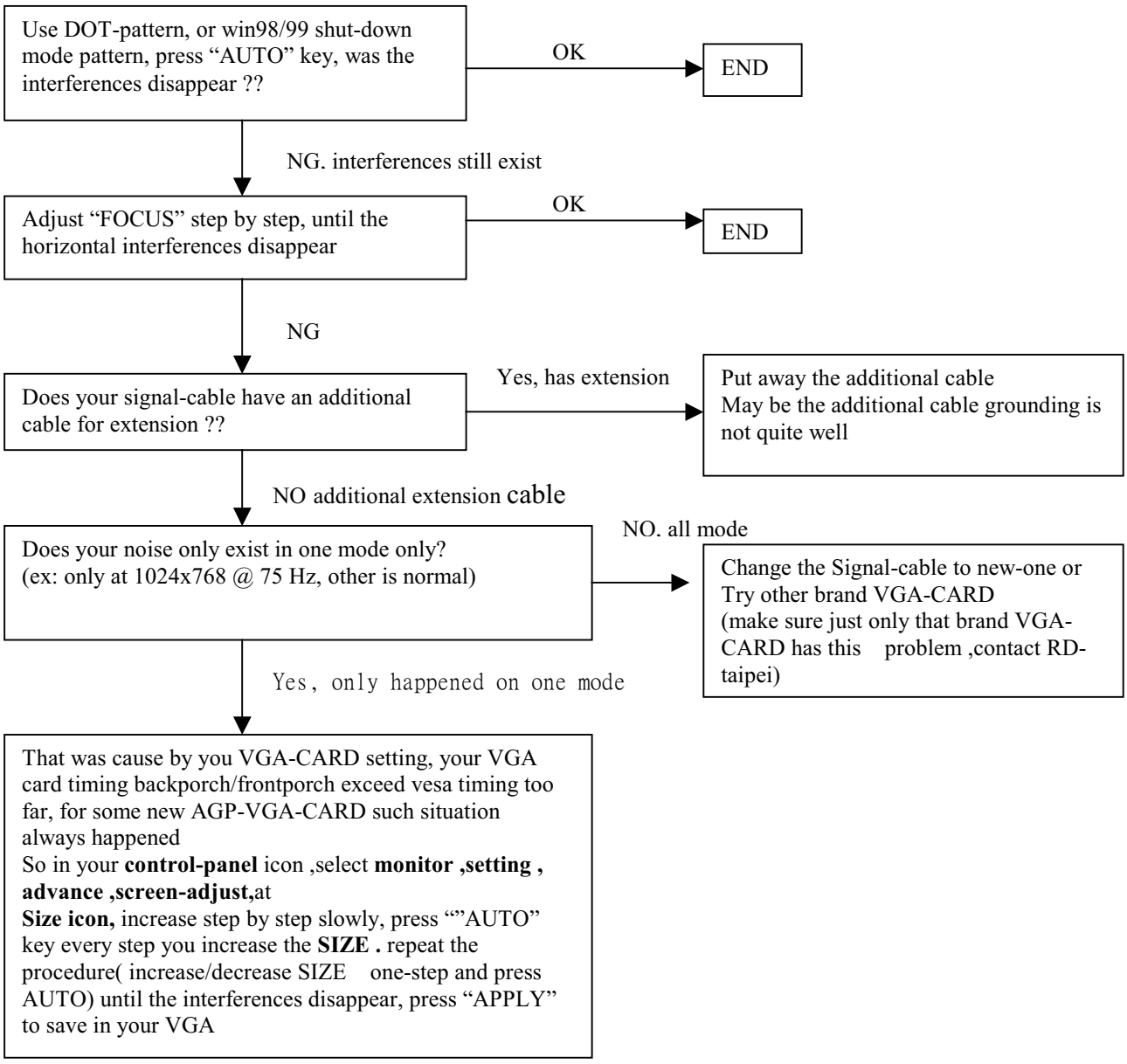
**Note : the Waveform of U901 pin 2 can determined the power situation

1. stable rectangle waveform with equal duty, freq around 150K-158KHz
   that means all power of this interface board is in normal operation
   ,and all status of 5V & 3.3V is working well
2. unstable or uneven rectangle waveform without same duty, that means ABNORMAL operation was happened, check 3.3V or 5V ,if short-circuit or bad component
3. rectangle waveform with large spike & harmonic pulse on front side , means all 3.3v is no load, U501 **Gmzan1** was shut-down, and only U102 **MCU** still working , that means the monitor is in power saving status , all power system is working well .



III.ALL SCREEN HAS INTERFERENCES OR NOISE, CAN'T BE FIXED BY AUTO KEY

**** NOTE:** There is so many kind of interferences, 1). One is cause by some VGA-CARD that not meet VESA spec or power grounding too bad that influence our circuit
2).other is cause by external interferences, move the monitor far from electronic equipment.(rarely happened)



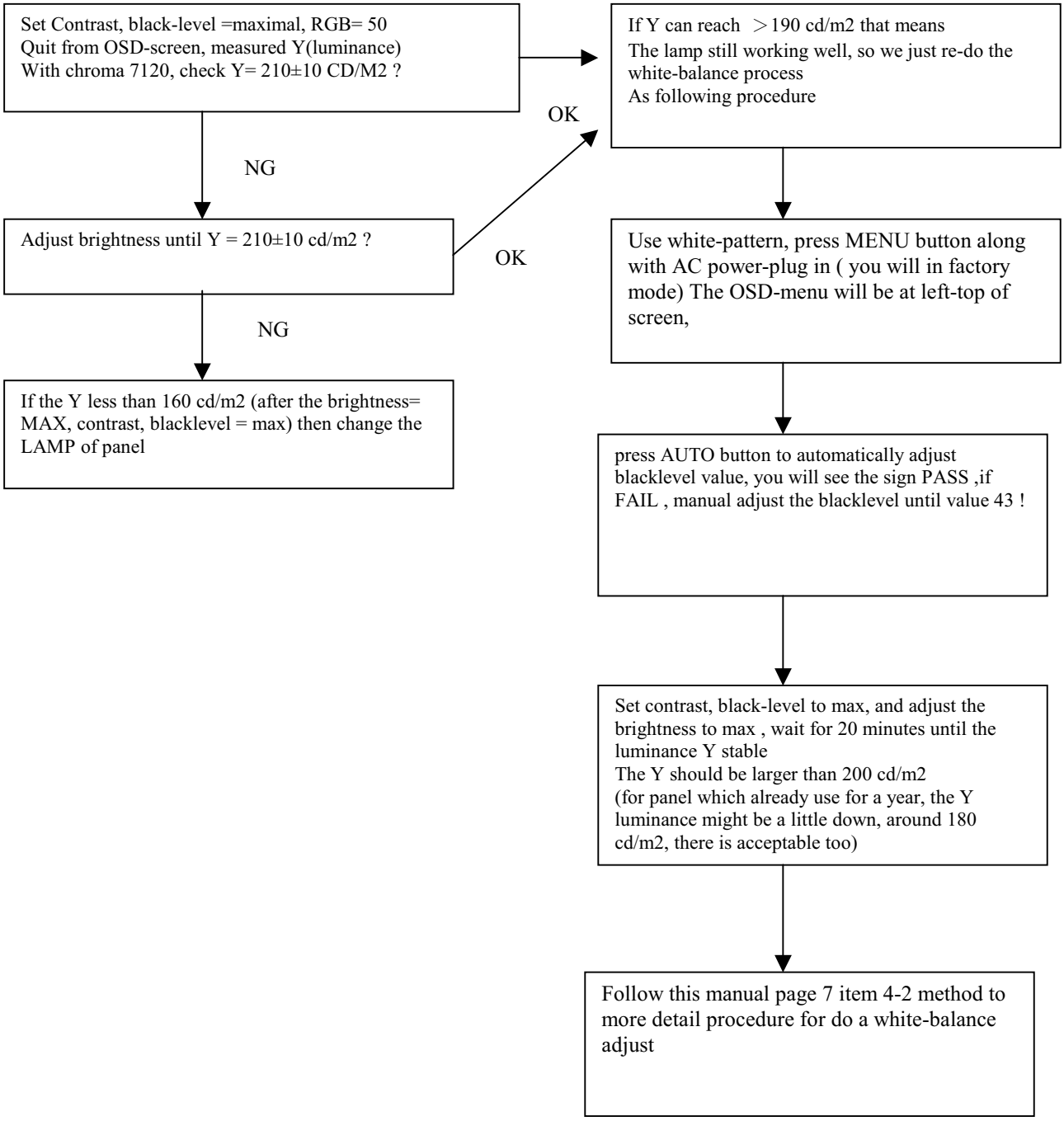
There is an interferences in **DOS MODE**

NOTE :the criteria of doing AUTO-CONFIGURATION : must be a full-size screen, if the screen not full , the auto-configuration will fail. So in dos mode ,just set your "CLOCK" in OSD-MENU to zero or use some EDITOR software which can full fill the whole screen (ex: PE2, HE) and then press "AUTO"

Or you can use "DOS1.EXE" which attached in your Driver disk to optimize DOS mode performance

V.THE PANEL LUMINANCE WAS DOWN

Use white pattern and resolution 1024x768 @ 60Hz , CHROMA 7120 measured the center of panel



6 B). Inverter –MODULE Spec &Trouble Shooting Chart

we use HANNSTAR SIP panel, and the INVERTER PROVIDER is SAMPO-CORPORATION

I.) TROUBLE SHOOTING OF HANNSTAR INVERTER (part no : 79AL15-7-S)

TYPE: L0068 FOR HANNSTAR 15" SIP PANEL

TROUBLE SHOOTING OF SIP-Hannstar INVERTER (DIVTL0068-D21- -)

1.SAMPO PART NO .: L0068 ,AOC PART NO.: 79AL15-7-S

2.SCOPE : this is to specify the requirements of the subject parts used in SIP-HANNSTAR(AP3R-150MX82) 15 inch (2 C.C.F.L.) LCD MONITOR

3.CONNECTOR PIN ASSIGMENT:

4-1. CON1: INPUT

MODEL NO.: S5B-PH-SM3-TB

PIN	SYMBOL	DESCRIPTION
1	Vin	Input voltage: 12V
2	GND	GND
3	ON/OFF	ON: 3V OFF:0V
4	Dimming	Dimming range (0V~+5.0V)
5	Dimming	Dimming range (0V~+5.0V

4-2. CON2,CON3 : OUTPUT

MODEL NO.: SM02(8.0)B-BHS-1-TB

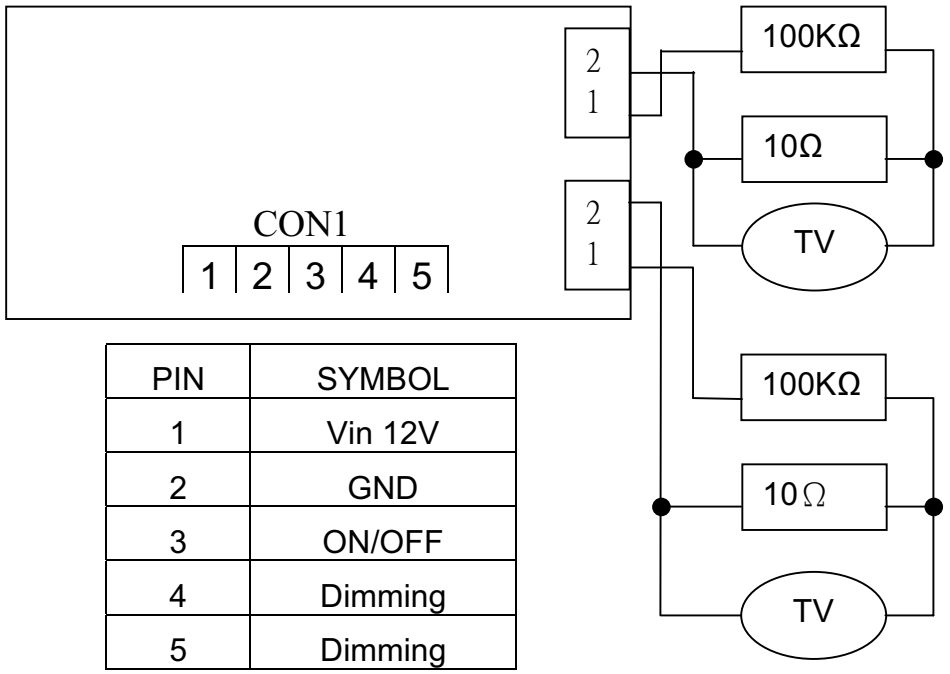
PIN	SYMBOL	DESCRIPTION
1	HV OUTPUT	Input H.V to lamps
2	RETURN	Return to control

5.FUNCTION SPECIFICATIONS:

The data test with the set of SAMPO, and the test circuit is as below.

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARK
Input voltage	Vin	10.8	12	13.2	V	
Input current	Iin	--	840	1300	mA	
output current adj:0v(min.)	Iout (min)	1.9	2.2	3.8	mA	FOR 1 CCFL LOAD:100KΩ
Output current adj.:5 v(max.)	Iout (max)	5.4	5.8	6.2	mA	FOR 1 CCFL LOAD:110KΩ
Frequency	F	40	50	60	KHZ	
H.V open	Vopen	1350	1500	1650	Vrms	NO LOAD
H.V Load	Vload	480	580	680	Vrms	Adj=0V

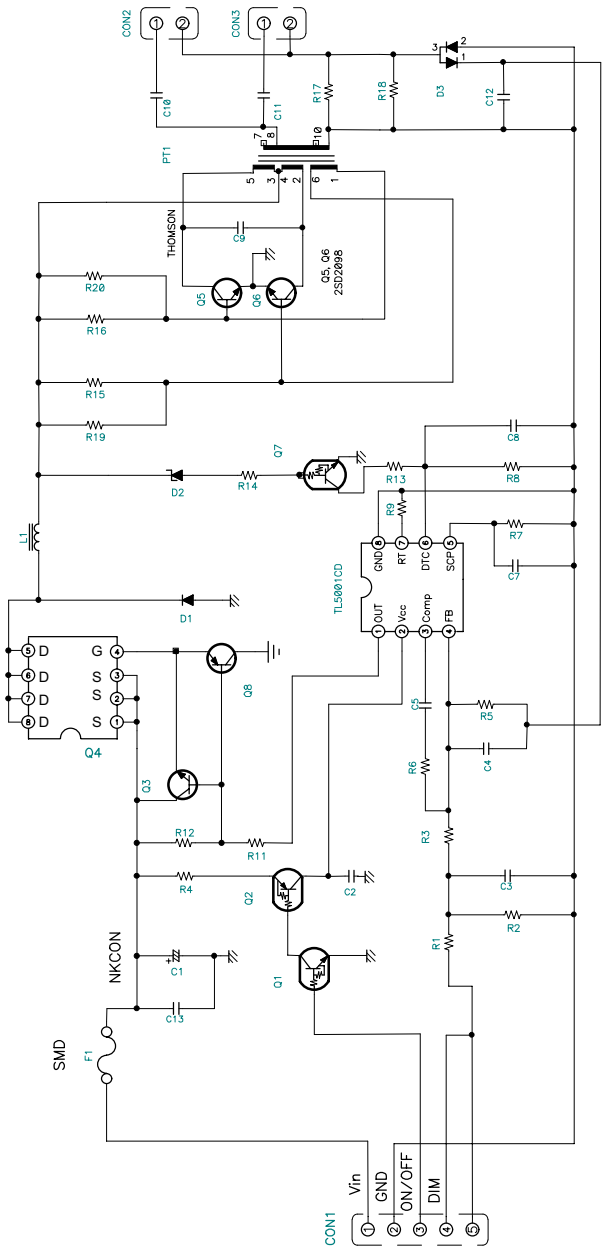
6. FUNCTION LOAD CIRCUIT:



PIN	SYMBOL
1	Vin 12V
2	GND
3	ON/OFF
4	Dimming
5	Dimming

TROUBLE SHOOTING OF SIP-Hannstar INVERTER (DIVTL0068-D21- -)

7.CIRCUIT DIAGRAM:



8.PART LIST

8-1 COMPONENTS LIST:

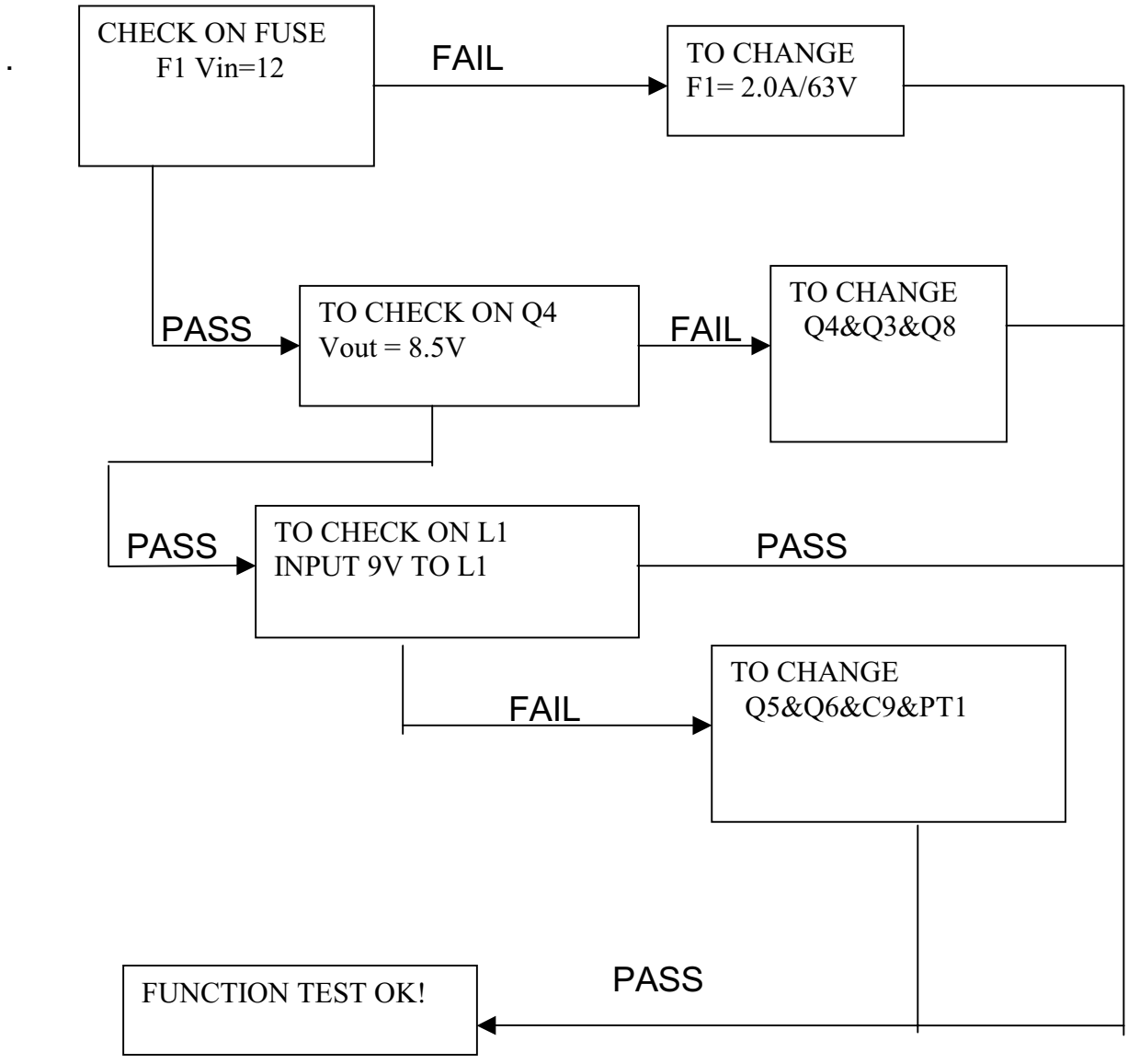
NO.	REF.	PART NAME	PART NUMBER	QTY	DESCRIPTION	REMARK
1.	CON1	CONNECTOR	S5B-PH-SM3-TB	1	JST	
2.	CON2,3	〃	SM02(8.0)B.BHS-1-TB GLSM02(8.0)-WH2	2	JST GLE	
3.	R1	RESISTOR	0603 30KΩ 5%	1	YAGEO,TDK	
4.	R2	〃	0603 5.1KΩ 5%	1	YAGEO,TDK	
5.	R3,4	〃	0603 2.2KΩ 5%	2	YAGEO,TDK	
6.	R6	〃	0603 0Ω 5%	1	YAGEO,TDK	
7.	R8	〃	0603 68KΩ 5%	1	YAGEO,TDK	
8.	R9	〃	0603 33KΩ 5%	1	YAGEO,TDK	
9.	R11	〃	0603 470Ω 5%	1	YAGEO,TDK	
10.	R12	〃	0603 3.9KΩ 5%	1	YAGEO,TDK	
11.	R13	〃	0603 4.7KΩ 5%	1	YAGEO,TDK	
12.	R14,5	〃	0603 47KΩ 5%	2	YAGEO,TDK	
13.	R17,18		0805 1KΩ 5%	2	YAGEO,TDK	
14.	R15,16.19,20	〃	1206 2KΩ 5%	4	YAGEO,TDK	
15.	Q1	TRANSIST0R	DTC144WKA	1	ROHM	
16.	Q2	〃	DTA144WKA	1	ROHM	
17.	Q3	〃	SST3904 MMBT3904	1 1	ROHM MOTOROLA	
18.	Q4	〃	CEM9435A SI9435DY	1 1	CET VISHAY	
19.	Q5,6	〃	2SD2098 2SD2150	2	ROHM	
20.	Q7	〃	DTC143EKA	1	ROHM	
21.	Q8	〃	SST3906 MMBT3906	1 1	ROHM MOTOROLA	
22.	C1	CAPACITOR	DIP NKCON 150μF/30V DIP OSCON 10μF/25V	1 1	NAKAMA SANYO	
23.	C2,3,12	〃	0805 X7R 0.1 μF/25V	3	TDK,PHILIPS,YAGEO	
24.	C4	〃	0805 X7R 0.01μF/25V	1	TDK,PHILIPS,YAGEO	

8-2 COMPONENTS LIST:

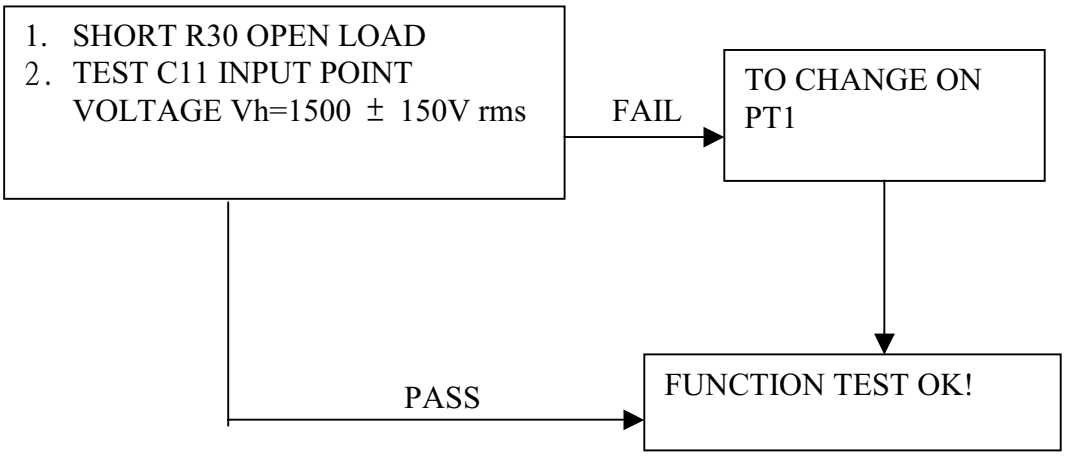
NO.	REF.	PART NAME	PART NUMBER	QTY	DESCRIPTION	REMARK
25.	C5,8	CAPACITOR	0805 Y5V 1 μF/25V	2	TDK,PHIPLS,YAGEO	
26.	C7	〃	22μF/6.3V	1	LELON	
27	C9	〃	FILM-CAP 0.18 μF/100V FILM-CAP 0.18 μF/100V	1	ARCOTRONICS TAIWAN TAI	
28.	C10,11	〃	22PF/3KV 5%	2	TDK	
29.	D1	DIODE	RB060L40 B240 SFPB-74	1 1 1	ROHM DIODS SANKEN	
30.	D2	〃	RLZ9.1B	1	ROHM	
31.	D3	〃	DAN217 DA204K BAV99-7	1	ROHM ROHM DIODES	
32.	I.C	I.C	SMD TL5001CDR	1	TI	
33.	F1	FUSE	2.0A/63V DC 2.0A/63V DC 2.3A/63V DC	1	BUSSMAN LITTLE ROHM	Attachment 3 Attachment 3-1
34.	L1	COIL	150μH 8% 150μH 8%	1	YAO SHENG 竑赫	Attachment 1
35.	PT1	TRANS	YST-1207	1	YAO SHENG	Attachment 2
36.	PCB	PCB	QPWBGL958IDG---	1	DM,CY,EISO	

9. TROUBLE SHOOTING

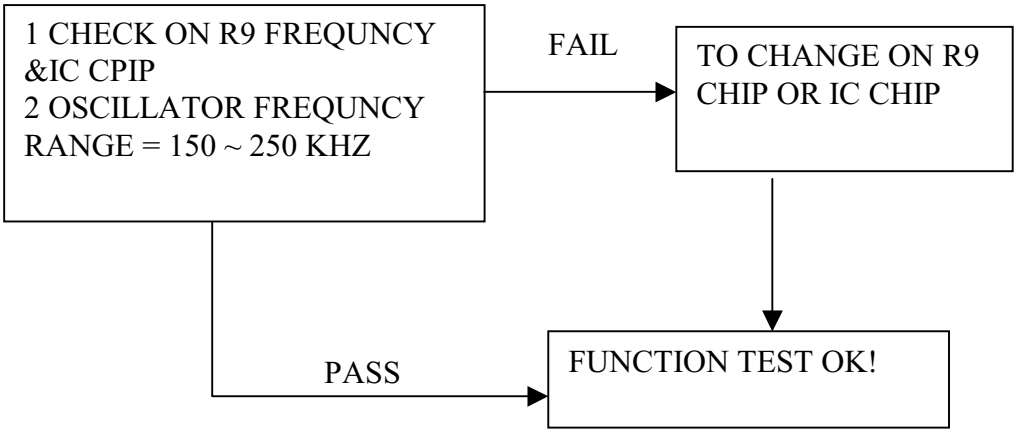
9-1 NO POWER:



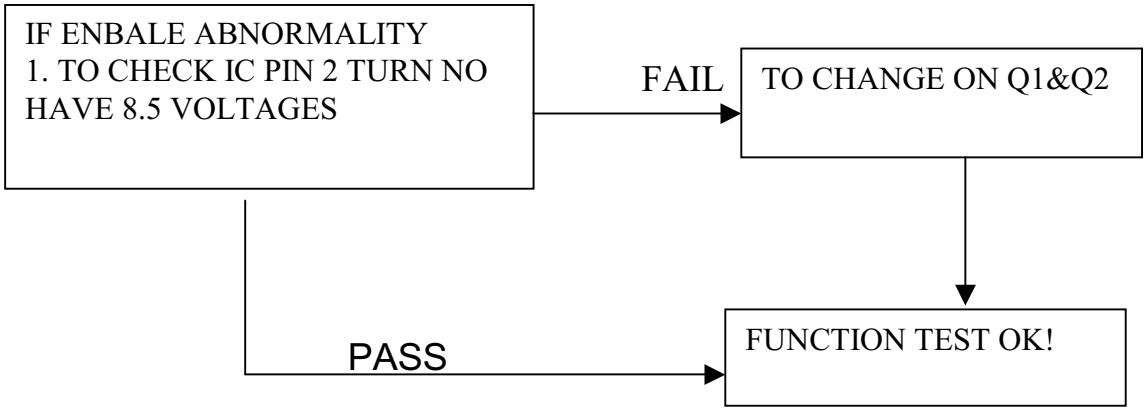
9-2 HIGHT VOLTAGE PROTECTION:



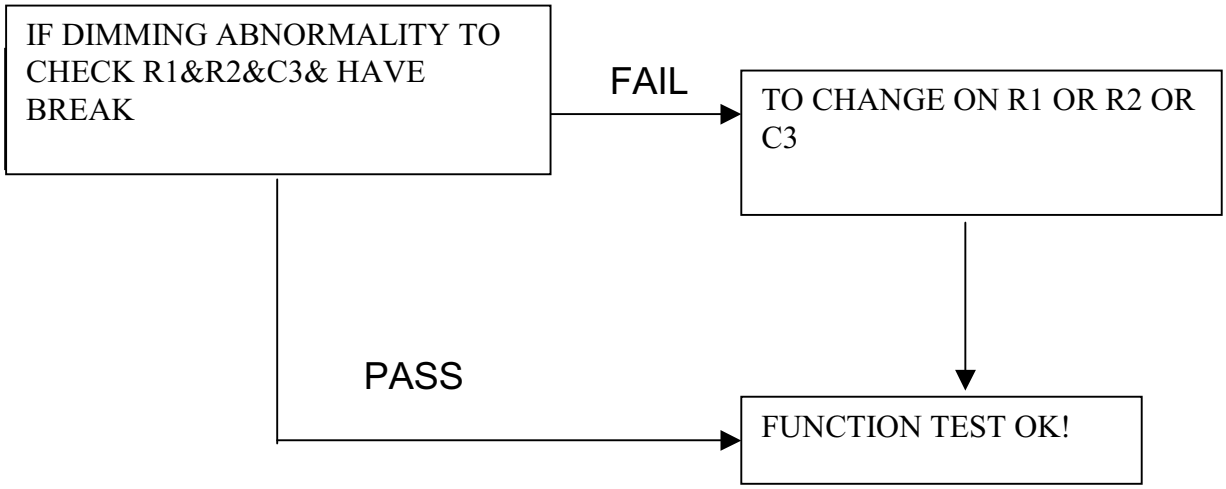
9-3 OUTPUT CURRENT ABNORMALITY:



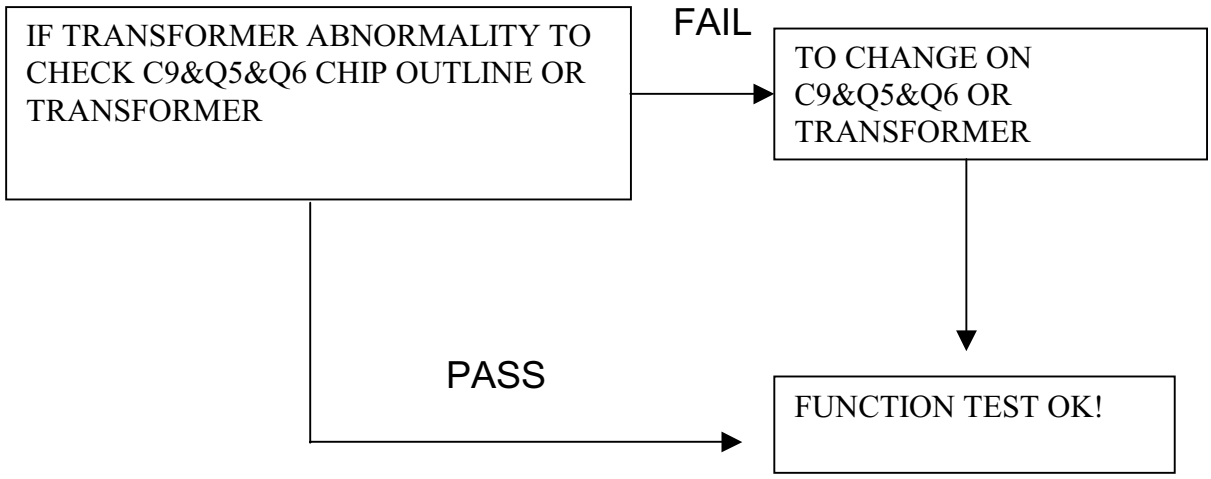
9-4. ENBALE ABNORMALITY:



9-5 DIMMING CONTROL ABNORMALITY:



9-6 TRANSFORMER ABNORMALITY:

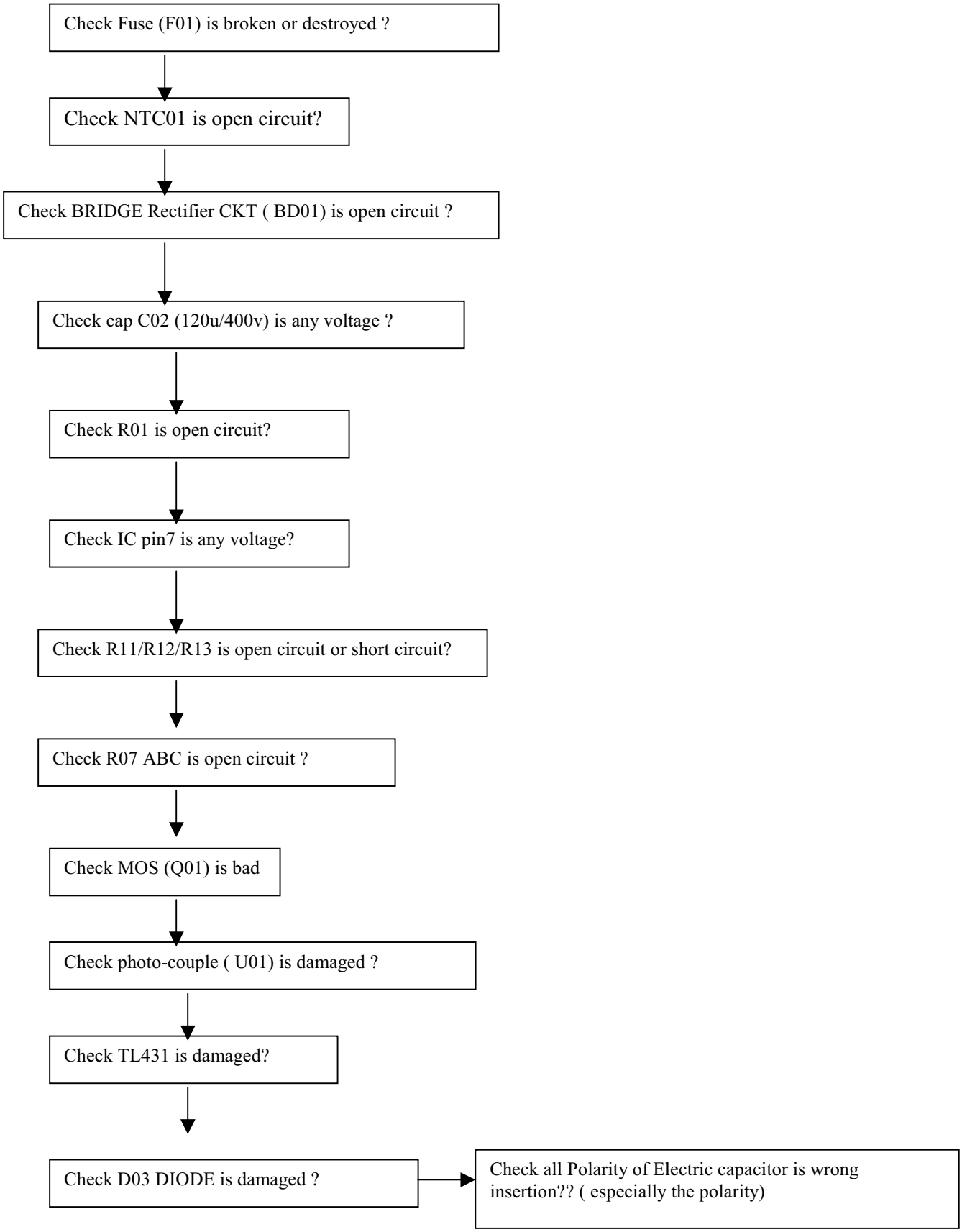


10. INSTRUMENTS FOR TEST:

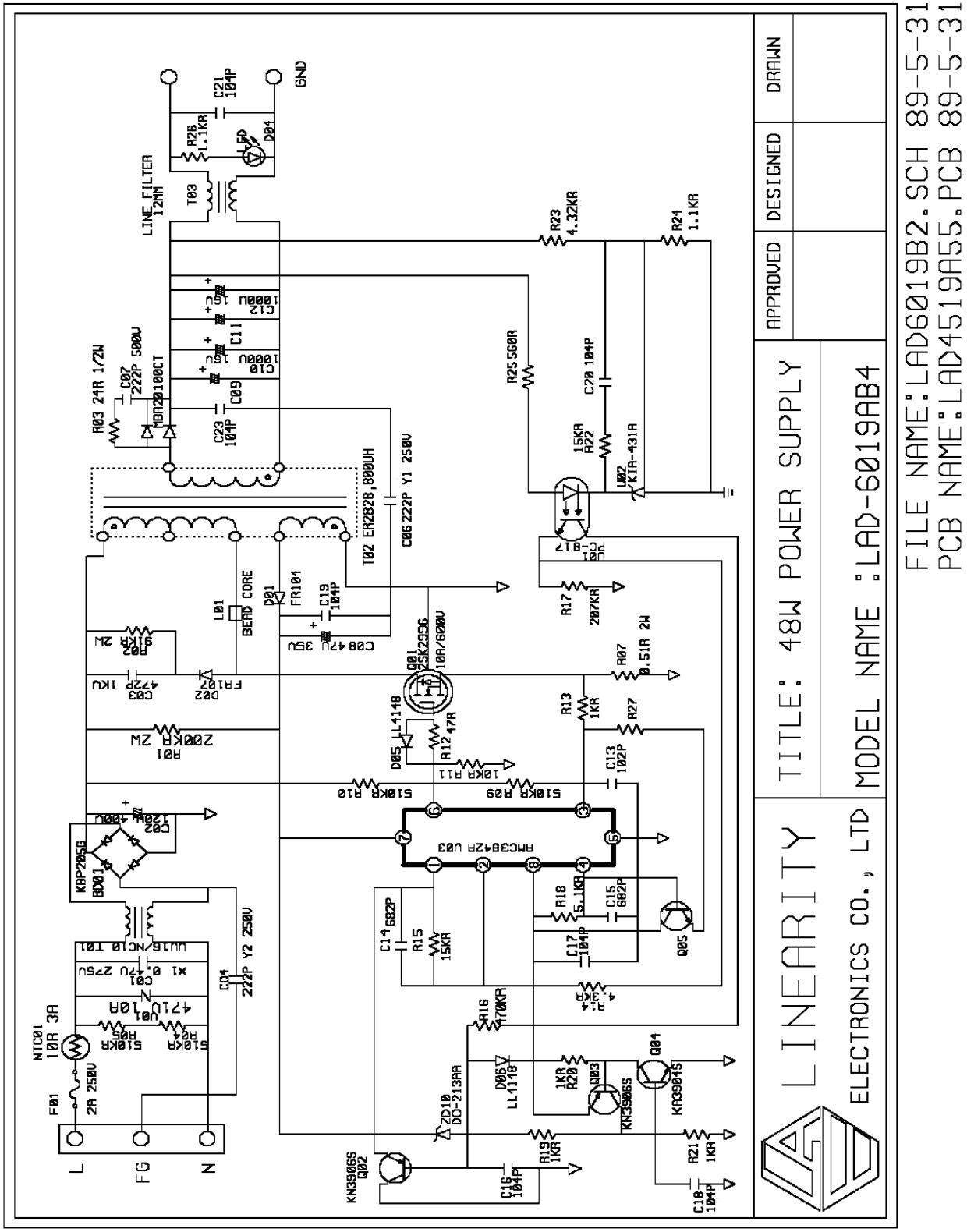
1. DC POWER SUPPLY	GPS-3030D
2. AC VTVM	VT:-181E
3. DIGITAL MULTIMERTER	MODEL-34401
4. HIGHTVOLT PROB	MODEL-1137A
5.SCOPE	MODEL-V-6545
6. AC mA METER	MODEL-2016 (YOKOGAWA)

6 C). ADAPTER-MODULE Trouble shooting chart

The following spec & block-diagram is offer by LINEARITY –COMPANY model 6019AB4 , for External Adapter **part number : 80AL15-4-LI**



I.) Adapter Schematic



III. ADAPTER BOM LIST (PART no. 80AL15-4-LI)

No.	Location	Specification	Unit	Q'ty	Type#
80AL15-4-LI SIEMENSE		110*62*14.75+LED (3 PIN)	PCS	1	HJ-211
		110*62*17.05(3PIN)	PCS	1	HJ-211
		CABLE UL 1185 #18 5.5*2.5*10*180cm	PCS	1	
		LABEL	PCS	1	
	B01	SOCKET PCB MOUNT	PCS	1	RF-190
80AL15-4A-LI AOC		110*62*14.75+LED(3 PIN)	PCS	1	HJ-211
		110*62*17.05(3 PIN)	PCS	1	HJ-211
		CABLE UL 1185 #18 5.5*2.5*10*180cm	PCS	1	
		LABEL	PCS	1	
	B01	SOCKET PCB MOUNT	PCS	1	SS-120
80AL15-4B-LI AOC		110*62*14.75+LED(3 PIN)	PCS	1	HJ-211
		110*62*17.05(3 PIN)	PCS	1	HJ-211
		CABLE UL 1185 #18 5.5*2.5*10*180cm	PCS	1	
		LABEL	PCS	1	
	B01	SOCKET PCB MOUNT	PCS	1	SS-120
1		SILICONE GREASE	PCS	0.007	SE9184
		SILICONE GREASE	PCS	0	KE4560G
2		TUBING	PCS	1	
3	D01	DIODE FAST,DO-41,400V/1A	PCS	1	FR104
	D01	CORE RH 3.5*5.0*1.3	PCS	1	T6-2000ui
	SUB	CORE RH 3.5*5*1.3	PCS	0	K5B
4	D02	DIODE FAST,DO-41,400V/1A	PCS	1	FR107
	D02	CORE RH 3.5*5.0*1.3	PCS	1	T6-2000ui
	SUB	CORE RH 3.5*5*1.3	PCS	0	K5B
5	D03	DIODE SCHOTTKY,TO-220,100V/20A	PCS	1	MBR20100CT
	SUB1	DIODE SCHOTTKY,TO-220,100V/10A	PCS	0	MBR10100CT
	SUB2	DIODE SCHOTTKY TO-220 100V/10A	PCS	0	SF10SC9
	D03	13mm*18.5mm, 0.45mm	PCS	1	TO-220
	D03	6D*2.8mm*3.0mm	PCS	1	SW06006
6	D04	DIODE LED	PCS	1	HB5-133
	D04	LED HOLDER 2PIN, 4.8*9, UL	PCS	1	
7	D05	DIODE NORMAL,DO-213AA	PCS	1	LL4148
8	D06	DIODE NORMAL,DO-213AA	PCS	1	LL4148
9	U01	IC PHOTO-COUPLE,DIP	PCS	1	PC-817
	SUB1	IC PHOTO-COUPLE,DIP	PCS	0	TCET1103
	SUB2	IC PHOTO-COUPLE,DIP	PCS	0	KPC-817
	SUB3	IC PHOTO-COUPLE,DIP	PCS	0	E113898
10	U02	IC HTL,DIP	PCS	1	KA431AZ
	SUB1	IC HTL,DIP,150mA/37V	PCS	0	KIA-431A
	SUB2	IC HTL,DIP	PCS	0	AP431V
	SUB3	IC HTL,DIP	PCS	0	TL431A

No.	Location	Specification	Unit	Q'ty	Type#
11	U03	IC NORMAL,SMD	PCS	1	AMC3842A
12	BD01	DIODE BRIDGE 2A 800V KBP	PCS	1	KBP206G
	SUB	DIODE BRIDGE, 2A/600V,KBP,	PCS	0	KBP206
13	Q01	TRANSISTOR MOS,9A/600V,TO-220F	PCS	1	2SK2645
	SUB1	TRANSISTOR MOS.SC-67,10A/600V	PCS	0	2SK2996
	SUB2	TRANSISTOR MOS.TO-220F,7A/600V	PCS	0	FS7KM-12
14	T01	LINE FILTER UU16/NC10,17mH(0.5D*50T)	PCS	1	
15	T02	X'FORMER ER2828,800uH	PCS	1	
16	T03	LINE FILTER 12mm,180uH(12*4*6,0.8D)	PCS	1	
17	F01	FUSE MICRO TIME LAG 2A/250V	PCS	1	SR-5
	SUB1	FUSE MICRO TIME LAG 2A/250V	PCS	0	MRT
	SUB2	FUSE MICRO TIME LAG 2A/250V	PCS	0	MST
	SUB3	FUSE MICRO TIME LAG 2A/250V	PCS	0	166050
18	L01	BEAD CORE 3.5D*4.7*0.8,60Ω	PCS	1	R5
	SUB	BEAD CORE 3.5D*4.7*0.8,60Ω	PCS	0	A6
19	H01	HENT SINK 89*2.5*20,L形,2孔1PIN(7,PIN)	PCS	1	
	H01	SCREW 3D*10	PCS	1	
	H01	SCREW NUT, 3D*5.4	PCS	1	
	H01	TYPE, PE, 34mm, 1L, MY9Y	M	0.15	
	SUB	TYPE PE, 34mm, 1L, 1350Y	M	0	
20	H02	HENT SINK 89*2.5*20,L形,2孔1PIN(7PIN)	PCS	1	
	H02	SCREW 3D*10	PCS	1	
	H02	SCREW NUT, 3D*5.4	M	1	
	H02	TYPE PE,34mm,1L MY9YY	MA	0.3	
	SUB	TYPE PE, 34mm, 1L, 1350Y	M	0	
21	ZD01	D0IDE ZENER,18V,1/2W,DO-213AA	PCS	1	TZMC18
22	Q02	TRANSISTOR PNP,SOT-23,200mA/100-300	PCS	1	KN3906S
23	Q03	TRANSISTOR PNP,SOT-23 200-400V	PCS	1	KTC1504S
24	Q04	TRANSISTOR NPN,SOT-23,200mA/100-300	PCS	1	KN3904S
25	V01	VARISTOR 1/4W,7D,470V,10A	PCS	1	TVR07471
	SUB	VARISTOR 1/4W,7D,470V,10A	PCS	0	V07K300
26	C01	CAPACITOR 0.47u ± 20% 275V	PCS	1	PCX2 355M
	SUB1	CAPACITOR 0.47u ± 20% 275V	PCS	0	MPX
	SUB2	CAPACITOR 0.47u ± 20% 275V	PCS	0	B81130 EMI
	SUB3	CAPACITOR 0.47u ± 10% 275V	PCS	0	SX1
	SUB4	CAPACITOR 0.47u ± 10% 275V	PCS	0	CTX
	SUB5	CAPACITOR 0.47u ± 10% 275V	PCS	0	KNB1530
	SUB6	CAPACITOR 0.47u ± 10% 275V	PCS	0	HQX
	SUB7	CAPACITOR 0.47u ± 10% 275V	PCS	0	MPX
	SUB8	CAPACITOR 0.47u ± 10% 275V	PCS	0	MPX

No.	Location	Specification	Unit	Q'ty	Type#
27	C02	CAPACITOR 120u,20%,400V(18*36)	PCS	1	SEK
	SUB1	CAPACITOR 120u,20%,400V(18*36)	PCS	0	KM
	SUB2	CAPACITOR 120u,20%,400V(18*36)	PCS	0	TK
28	C03	CAPACITOR 472P,20%,1KV(KINK)	PCS	1	EM8472MH
	SUB	CAPACITOR 472P,20%,1KV(KINK)	PCS	0	
29	C04	Y2 CAPACITOR 222P,20%,250V,DE1007E222M	PCS	1	KH
	SUB1	Y2 CAPACITOR 222P 20% 400V	PCS	0	AC
	SUB2	Y2 CAPACITOR 222P,20%,250V,ECKATS222	PCS	0	TS
	SUB3	Y2 CAPACITOR 222P 20% 400V	PCS	0	CS
	SUB4	Y2 CAPACITOR 222P 20% 400V 5SF222MT252A77	PCS	0	SF
	SUB5	Y2 CAPACITOR 222P 10% 250V	PCS	0	CS
	SUB6	Y1 CAPACITOR 222P,20% 250V	PCS	0	KX
	SUB7	Y1 CAPACITOR 222P 20% 400V AH12E222ML0	PCS	0	AH
	SUB8	Y1 CAPACITOR 222P, 20%,400	PCS	0	CD
	SUB9	Y1 CAPACITOR 222P 20% 400V 5SE222MT402A97	PCS	0	SE
	SUB10	Y1 CAPACITOR 222P 10% 250V	PCS	0	CD
	SUB11	Y1 CAPACITOR 222P 10% 250V	PCS	0	NA
	C04	BEAD CORE RH 3.5*5.0*1.3	PCS	1	T6-2000ui
	SUB	BEAD CORE RH 3.5*5*1.3	PCS	0	K5B
30	C06	Y1 CAPACITOR 222P,20% 250V	PCS	1	KX
	SUB1	Y1 CAPACITOR 222P 20% 400V AH12E222ML0	PCS	0	AH
	SUB2	Y1 CAPACITOR 222P, 20%,400	PCS	0	CD
	SUB3	Y1 CAPACITOR 222P 20% 400V 5SE222MT402A97	PCS	0	SE
	SUB4	Y1 CAPACITOR 222P 10% 250V	PCS	0	CD
	SUB12	Y1 CAPACITOR 222P 10% 250V	PCS	0	NA
	C06	BEAD CORE RH 3.5*5.0*1.3	PCS	1	T6-2000ui
	SUB	BEAD CORE RH 3.5*5*1.3	PCS	0	K5B
31	C07	CAPACITOR 222P,20%,500V(KINK)	PCS	1	EC5222MH
	SUB	CAPACITOR 222P,20%,500V (KINK)	PCS	0	
32	C08	CAPACITOR 47u,20%,35V	PCS	1	SEK
	SUB1	CAPACITOR 47u,20%,35V(6*11)	PCS	0	KM
	SUB2	CAPACITOR 47u,20%,35V(6*11)	PCS	0	TK
33	C10	CAPACITOR 1000u,20%,16V (10*19)	PCS	1	SC
	SUB	CAPACITOR 1000u,20%,16V (10*20)	PCS	0	WL
34	C11	DIODE ZENER,5.6V,1W,DO-41	PCS	1	1N4744A
35	C12	CAPACITOR 1000u,20%,16V (10*19)	PCS	1	SC
	SUB	CAPACITOR 1000u,20%,16V (10*20)	PCS	0	WL
36	C13	CAPACITOR SMD,102P,10%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,102P,10%,50V	PCS	0	0805

No.	Location	Specification	Unit	Q'ty	Type#
37	C14	CAPACITOR SMD,682P,10%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,682P,10%,50V	PCS	0	0805
38	C15	CAPACITOR SMD,682P,10%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,682P,10%,50V	PCS	0	0805
39	C16	CAPACITOR SMD,104P,+80%-20%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,104P,+80%-20%,50V	PCS	0	0805
40	C17	CAPACITOR SMD,104P,+80%-20%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,104P,+80%-20%,50V	PCS	0	0805
41	C18	CAPACITOR SMD,104P,+80%-20%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,104P,+80%-20%,50V	PCS	0	0805
42	C19	CAPACITOR SMD,104P,+80%-20%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,104P,+80%-20%,50V	PCS	0	0805
43	C20	CAPACITOR SMD,104P,+80%-20%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,104P,+80%-20%,50V	PCS	0	0805
44	C21	CAPACITOR SMD,104P,+80%-20%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,104P,+80%-20%,50V	PCS	0	0805
45	C23	CAPACITOR SMD,104P,+80%-20%,50V	PCS	1	0805
	SUB	CAPACITOR SMD,104P,+80%-20%,50V	PCS	0	0805
46	NTC01	RESISTOR 10D, 10Ω,3A,20%	PCS	1	SCK103
	SUB	RESISTOR 10D, 10Ω,3A,±15%	PCS	0	N10SP010
47	R01	RESISTOR 2W,200KΩ,± 5%	PCS	1	
	R01	TUBING 5D*12	PCS	1	
48	R02	RESISTOR 2W,91KΩ,± 5%	PCS	1	
49	R02	TUBING 6*15	PCS	1	
50	R03	RESISTOR 1/2W,24Ω,± 5%	PCS	1	
51	R04	RESISTOR 1206(1/4W)SMD,510KΩ,± 5%	PCS	1	
52	R05	RESISTOR 1206(1/4W)SMD,510KΩ,± 5%	PCS	1	
53	R07	RESISTOR 2W,0.51Ω,± 5%	PCS	1	
	R07	TUBING,6*15	PCS	1	
54	R09	RESISTOR 1206(1/4W)SMD,680KΩ,± 5%	PCS	1	
55	R10	RESISTOR 1206(1/4W)SMD,680KΩ,± 5%	PCS	1	

No.	Location	Specification	Unit	Q'ty	Type#
56	R11	CHIP RESISTOR 0805(1/8W)SMD,10KΩ,± 5%	PCS	1	
57	R12	CHIP RESISTOR0805(1/8W)SMD,47Ω,± 5%	PCS	1	
58	R13	CHIP RESISTOR 0805(1/8W)SMD,1KΩ,± 5%	PCS	1	
59	R14	CHIP RESISTOR 0805(1/8W)SMD,4.3KΩ,± 5%	PCS	1	
60	R15	CHIP RESISTOR 0805(1/8W)SMD,15KΩ,± 5%	PCS	1	
61	R16	CHIP RESISTOR 0805(1/8W)SMD,47KΩ,± 5%	PCS	1	
62	R17	CHIP RESISTOR 0805(1/8W)SMD2.7KΩ,± 5%	PCS	1	
63	R18	CHIP RESISTOR 0805(1/8W)SMD,5.1KΩ,± 5%	PCS	1	
64	R19	CHIP RESISTOR 0805(1/8W)SMD,1KΩ,± 5%	PCS	1	
65	R20	CHIP RESISTOR 0805(1/8W)SMD,1KΩ,± 5%	PCS	1	
66	R21	CHIP RESISTOR 0805(1/8W)SMD,1KΩ,± 5%	PCS	1	
67	R22	CHIP RESISTOR 0805(1/8W)SMD,15KΩ,± 5%	PCS	1	
68	R23	CHIP RESISTOR 0805(1/8W)SMD,4.3KΩ,± 1%	PCS	1	
69	R24	CHIP RESISTOR 0805(1/8W)SMD,1.1KΩ,± 1%	PCS	1	
70	R25	CHIP RESISTOR 0805(1/8W)SMD,560Ω,± 5%	PCS	1	
71	R26	RESISTOR 1206(1/4W)SMD,1.1KΩ,± 5%	PCS	1	
72	J01	TIN COATED 0.6mm, 20mm	PCS	1	
73	J02	TIN COATED 0.6mm,30mm	PCS	1	
74	J04	CHIP RESISTOR 0805(1/8W)SMD,0Ω,± 5%	PCS	1	
75		PCB CAM1/1oZ,T=1.6mm	PCS	1	E117266 E174757

WINBOND WFP4620D

ITEM	NAME	I/O	FUNCTION	PIN
Main-Input-Pins	OR{0:7}	In	Odd Red data OR0: LSB OR7:MSB	50,49,48,47,46,45,43,42
	OG{0:7}	In	Odd Green data OG0: LSB OG7:MSB	41,39,38,37,36,35,34,33
	OB{0:7}	In	Odd Blue data OB0: LSB OB7:MSB	32,31,30,29,27,26,25,24
	ER{0:7}	In	Even Red data ER0: LSB ER7:MSB	85,84,83,82,81,79,78,77
	EG{0:7}	In	Even Green data EG0: LSB EG7:MSB	76,75,74,73,72,71,70,69
	EB{0:7}	In	Even Blue data EB0: LSB EB7:MSB	67,66,65,63,62,61,60,59
	DISPE	In		23
	DHS	In	Horizontal Sync	56
	DVS	In	Vertical Sync	55
	Odd-CLK	In	System Clock,Negative edge trigger	86
	Even-CLK	In	System Clock,Negative edge trigger	51
X-Driver Control Signal (Source –IC)	OR{0:5}	Out	Pixel data bus	22,21,20,19,17,16
	OG{0:5}	Out		14,13,12,10,9,7
	OB{0:5}	Out		6,5,4,3,1,144
	ER{0:5}	Out		130,129,128,127,125,124
	EG{0:5}	Out		122,121,120,119,118,117
	EB{0:5}	Out		115,114,112,111,110,109
	STH	Out	Start-Pulse	141
	LOAD	Out	Output Timing Signal	142
	ORVS	Out	Data Inversion Control signal for Odd-Pixel Data, When Add18=Low, ORVS and ERVS are the same output	143
	ERVS	Out	Data Inversion Control signal for Even-Pixel Data, When Add18=Low, ORVS and ERVS are the same output	135
	CPH1	Out	System Clock, Rising edge Trigger	139
	CPH2	Out	System Clock, Rising edge Trigger	132
	POL	Out	Polarity Inversion Signal	
Y-Driver Control Signal (Gate-IC)	STV1	Out	1st Scanning Start Pulse	108
	STV2	Out	2nd Scanning Start Pulse	107
	CPV	Out	Row Clock	106
	OE	Out	Output Enable, Low Active	105
Reset	PWON	In	Power-On reset	101
	NSHUT	Out	Shut-Down Signal	104
	CHRG1	Out(3-state)	Pull-Low	103
	CHRG2	Out(3-state)	Pull-Low	102
Test-Pin	TEST	In	Normal-Operating=L	88
	SCAN	In	Normal-Operating=L	89
	NRSET	In	Normal-Operating=H	54
Power	VDD		3.3V	2,11,18,40,68,90,113,123,131
	GND		GND	8,15,28,44,57,64,80,100,116, 126,136,140

Mode-Setup (Extra-Function setting)	DRVS	In (with Schmitt)	Data-Inversion On/Off control L=No-Inverse,H=Inverse	96
	ADD18	In (with Schmitt)	Data Inversion Control Signal L=2 Pixels Data Inversion (36 bit) H=1 Pixels Data Inversion (18 bit)	99
	FRC	In (with Schmitt)	FRC ON/OFF Control L=No-FRC, H=FRC	95
	G0	In (with Schmitt)	Gate-Phase Adjustment (G1,G0)= (L,L) →5us (L,H)→4.5us (H,L) →4.0us (H,H) →3.0us	93
	G1	In (with Schmitt)		94
	GD0	In (with Schmitt)	Gate-output Control (GD1,GD0)= (L,L) →2.0us (L,H)→ 1.5us (H,L) →1.0us (H,H) →0.5us	91
	GD1	In (with Schmitt)		92
	LD0	In (with Schmitt)	Load-Pulse-width Control (LD1,LD0)= (L,L) →0.28us (L,H)→0.6us (H,L) →2.0us (H,H) →Test mode	98
	LD1	In (with Schmitt)		97
	MLCNG1	In (with Schmitt)	Input Date Format Setup MLCNG1= L → MX41 format MLCNG1= H →TEST mode	137
Mode-Setup (Extra-Function setting)	OECHNG	In (with Schmitt)	Odd/Even bus exchange control OECHNG= L →Disable OECHNG= H →Enable	87
	MLCHG2	In (with Schmitt)	MSB/LSB bus exchange control MLCHG2= L →Disable MLCHG2= H →Enable	53
	RBCHNG	In (with Schmitt)	RED/Blue bus exchange control RBCHNG= L →Disable RBCHNG= H →Enable	134
	CPSTP	In (with Schmitt)	CPH output control CPSTP=L Disable CPSTP=H Enable	133
	PTRN	In (with Schmitt)	Embedded Pattern Generator L=Normal operating H=Active	52

GMZAN1

The gmZAN1device utilizes Genesis' patented third-generation Advanced Image Magnification technology as well as a proven integrated ADC/PLL to provide excellent image quality within a cost effective SVGA/XGA LCD monitor solution.
As a pin-compatible replacement for the gmB120, the gmZAN1 incorporates all of the gmB120 features plus many enhanced features; including 10-bit gamma correction, Adaptive Contrast Enhancement (ACE) filtering, Sync On Green (SOG), and an enhanced OSD.

1.1 Features

- Fully integrated 135MHz 8-bit triple-ADC, PLL, and pre-amplifier
- GmZ2 scaling algorithm featuring new Adaptive Contrast Enhancement (ACE)
- On-chip programmable OSD engine
- Integrated PLLs
- 10-bit programmable gamma correction
- Host interface with 1 or 4 data bits
- Pin-compatible with gmB120

Integrated Analog Front End

- Integrated 8-bit triple ADC
- Up to 135MHz sampling rates
- No additional components needed
- All color depths up to 24-bits/pixel are supported

High-Quality Advanced Scaling

- Fully programmable zoom
- Independent horizontal / vertical zoom
- Enhanced and adaptive scaling algorithm for optimal image quality
- Recovery Mode / Native Mode

Input Format

- Analog RGB up to XGA 85Hz
- Support for Sync On Green (SOG)
- Support for composite sync modes

Output Format

- Support for 8 or 6-bit panels (with high quality dithering)
- One or two pixel output format

Built In High-Speed Clock Generator

- Fully programmable timing parameters
- On-chip PLLs generate clocks for the on-chip ADC and pixel clock from a single reference oscillator

Auto-Configuration / Auto-Detection

- Phase and image positioning
- Input format detection

Operation Modes

- Bypass mode with no filtering
- Multiple zoom modes:
  - With filtering
  - With adaptive (ACE) filtering

Integrated On-Screen Display

- On-chip character RAM and ROM for better customization
- External OSD supported for greater flexibility
- Supports both landscape and portrait fonts
- Many other font capabilities including: blinking, overlay and transparency

1.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 1 : Analog-to-Digital Converter

PIN #	Name	I/O	Description
77	ADC_VDD2		Digital power for ADC encoding logic. Must be bypassed with 0.1uF capacitor to pin 78 (ADC_GND2)
78	ADC_GND2		Digital GND for ADC encoding logic. Must be directly connected to the digital system ground plane.
79	ADC_VDD1		Digital power for ADC clocking circuit. Must by passed with 0.1uF capacitor to pin 80 (ACD_GND1).
80	ADC_GND1		Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
81	SUB_GNDA		Dedicated pin for substrate guard ring that protects the ADC reference system. Must be directly connected to the analog system ground plane.
82	ADC_GNDA		Analog ground for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be directly connected to analog system ground plane.
84	ADC_VDDA		Analog power for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be bypassed with 0.1uF capacitor to pin 82 (ADC_GNDA).
83	Reserved		For internal testing purpose only. Do not connect.
85	ADC_BGNDA		Analog ground for the blue channel. Must be directly connected to the analog system ground plane.
88	ADC_BVDDA		Analog power for the blue channel. Must be bypassed with 0.1uF capacitor to pin 85(BGNDA).
86	BLUE-	I	Negative analog input for the Blue channel.
87	BLUE+	I	Positive analog input for the Blue channel.
89	ADC_GGNDA		Analog ground for the green channel. Must be directly connected to the analog system ground plane.
92	ADC_GVDDA		Analog power for the green channel. Must be bypassed with 0.1uF capacitor to pin 89 (ADC_GGNDA).
90	GREEN-	I	Negative analog input for the Green channel.
91	GREEN+	I	Positive analog input for the Green channel.
93	ADC_RGNDA		Analog ground for the red channel. Must be directly connected to the analog system ground plane.
96	ADC_RVDDA		Analog power for the red channel. Must be bypassed with 0.1uF capacitor to pin 93 (ADC_RGNDA).
94	RED-	I	Negative analog input for the Red channel.
95	RED+	I	Positive analog input for the Red channel.

Table 2 : Host Interface (HIF) / External On-Screen Display

PIN #	Name	I/O	Description
98	HFS	I	Host Frame Sync. Frames the packet on the serial channel.
103	HCLK	I	Clock signal input for the 3-wire serial communication.
99	HDATA	I/O	Data signal for the 3-wire serial communication.
100	RESETn	I	Resets the gmZAN1 chip to a known state when low.
101	IRQ	O	Interrupt request output.
115	OSD-HREF	O	HSYNC output for an external OSD controller chip.
116	OSD-VREF	O	VSYNC output for an external OSD controller chip.
117	OSD-Clk	O	Clock output for an external OSD controller chip.
118	OSD-Data0	I	Data input 0 from an external OSD controller chip.
119	OSD-Data1	I	Data input 1 from an external OSD controller chip.
120	OSD-Data2	I	Data input 2 from an external OSD controller chip.
121	OSD-Data3	I	Data input 3 from an external OSD controller chip.
122	OSD-FSW	I	External OSD window display enable. Displays data from external OSD controller when high.
123	MFB11	I/O	Multi-Function Bus 11. One of twelve multi-function signals MFB[11:0].
124	MFB10	I/O	Multi-Function Bus 10. One of twelve multi-function signals MFB[11:0].
102	MFB9	I/O	Multi-Function Bus 9. One of twelve multi-function signals MFB[11:0]. Also used as HDATA3 in a 4-bit host interface configuration.
104	MFB8	I/O	Multi-Function Bus 8. One of twelve multi-function signals MFB[11:0]. Also used as HDATA2 in a 4-bit host interface configuration.
105	MFB7	I/O	Multi-Function Bus 7. One of twelve multi-function signals MFB[11:0]. Also used as HDATA1 in a 4-bit host interface configuration.
106	MFB6	I/O	Multi-Function Bus 6. One of twelve multi-function signals MFB[11:0]. Internally pulled up. When externally pulled down (sampled at reset) the host interface is configured for 4 bits wide. In this configuration, MFB9:7 are used as HDATA 3:1.
107	MFB5	I/O	Multi-Function Bus 5 One of twelve multi-function signals MFB[11:0]. Internally pulled up. When externally pulled down (sampled at reset) the chip uses an external crystal resonator across pins 141 and 142, instead of an oscillator.
109	MFB4	I/O	Multi-Function Bus 4. One of twelve multi-function signals MFB[11:0].
110	MFB3	I/O	Multi-Function Bus 3. One of twelve multi-function signals MFB[11:0].
111	FMB2	I/O	Multi-Function Bus 2. One of twelve multi-function signals MFB[11:0].
112	MFB1	I/O	Multi-Function Bus 1. One of twelve multi-function signals MFB[11:0].
113	MFB0	I/O	Multi-Function Bus 0. One of twelve multi-function signals MFB[11:0].

Table 3 : Clock Recovery / Time Base Conversion

PIN #	Name	I/O	Description
125	DVDD		Digital power for Destination DDS (direct digital synthesizer). Must be bypassed with a 0.1uF capacitor to digital ground plane.
127	DAC_DGNDA		Analog ground for Destination DDS DAC. Must be directly connected to the analog system ground plane.
128	DAC_DVDDA		Analog power for Destination DDS DAC. Must be bypassed with a 0.1uF capacitor to pin 127 (DAC_DGNDA).
129	PLL_DVDDA		Analog power for the Destination DDS PLL. Must be bypassed with a 0.1uF capacitor to pin 131 (PLL_DGNDA).
130	Reserved		For testing purposes only. Do not connect.
131	PLL_DGNDA		Analog ground for the Destination DDS PLL. Must be directly connected to the analog system ground plane.
132	SUB_DGNDA		Dedicated pin for the substrate guard ring that protects the Destination DDS. Must be directly connected to the analog system ground plane.
133	SUB_SGNDA		Dedicated pin for the substrate guard ring that protects the Source DDS. Must be directly connected to the analog system ground plane.
134	PLL_SGNDA		Analog ground for the Source DDS PLL. Must be directly connected to the analog system ground.
135	Reserved		For testing purposes only. Do not connect.
136	PLL_SVDDA		Analog power for the Source DDS DAC. Must be bypassed with a 0.1uF capacitor to pin 134 (PLL_SGNDA)
137	DAC_SVDDA		Analog power for the Source DDS DAC. Must be by passed with a 0.1uF capacitor to pin 138 (DAC_SGNDA)
138	DAC_SGNDA		Analog power for the Source DDS DAC. Must be directly connected to the analog system ground.
139	SVDD		Digital power for the Source DDS. Must be bypassed with a 0.1uF capacitor to digital ground plane.
141	TCLK	I	Reference clock(TCLK) input from the 50 MHz crystal oscillator
142	XTAL	O	If using an external oscillator, leave this pin floating. If using an external crystal, connect crystal between TCLK(141) and XTAL(142). See MFB5(pin 107).
143	PLL_RVDDA		Analog power for the Reference DDS PLL. Must be bypassed with a 0.1uF capacitor to pin 144(PLL_RGNDA)
144	PLL_RGNDA		Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
145	Reserved		For testing purposes only. Do not connect.
146	SUB_RGNDA		Dedicated pin for the substrate guard ring that protects the Reference DDS. Must be directly connected to the analog system ground plane.
148	VSYNC	I	CRT Vsync input. TTL Schmitt trigger input.
149	SYN_VDD		Digital power for CRT Sync input.
150	HSYNC/CSYNC	I	CRT Hsync or CRT composite sync input. TTL Schmitt trigger input.

Table 4. TFT Panel Interface

PIN #	Name	I/O	Description				
			2pxl/clk 8bit	2pxl/clk 6-bit	1pxl/clk 8-bit	1pxl/clk 6-bit	TFT
6	PD47	O	OB1	-	-	-	
7	PD46	O	OB0	-	-	-	
9	PD45	O	OG1	-	-	-	
10	PD44	O	OG0	-	-	-	
13	PD43	O	OR1	-	-	-	
14	PD42	O	OR0	-	-	-	
15	PD41	O	EB1	-	B1	-	
16	PD40	O	EB0	-	B0	-	
17	PD39	O	EG1	-	G1	-	
19	PD38	O	EG0	-	G0	-	
20	PD37	O	ER1	-	R1	-	
22	PD36	O	ER0	-	R0	-	
23	PD35	O	OB7	OB5	-	-	
24	PD34	O	OB6	OB4	-	-	
25	PD33	O	OB5	OB3	-	-	
26	PD32	O	OB4	OB2	-	-	
27	PD31	O	OB3	OB1	-	-	
28	PD30	O	OB2	OB0	-	-	
29	PD29	O	OG7	OG5	-	-	
31	PD28	O	OG6	OG4	-	-	
32	PD27	O	OG5	OG3	-	-	
34	PD26	O	OG4	OG2	-	-	
35	PD25	O	OG3	OG1	-	-	
36	PD24	O	OG2	OG0	-	-	
37	PD23	O	OR7	OR5	-	-	
38	PD22	O	OR6	OR4	-	-	
39	PD21	O	OR5	OR3	-	-	
42	PD20	O	OR4	OR2	-	-	
46	PD19	O	OR3	OR1	-	-	
47	PD18	O	OR2	OR0	-	-	
48	PD17	O	EB7	EB5	B7	B5	
50	PD16	O	EB6	EB4	B6	B4	
51	PD15	O	EB5	EB3	B5	B3	
52	PD14	O	EB4	EB2	B4	B2	
53	PD13	O	EB3	EB1	B3	B1	
54	PD12	O	EB2	EB0	B2	B0	
55	PD11	O	EG7	EG5	G7	G5	

PIN #	Name	I/O	Description 2pxl/clk 8bit	2pxl/clk 6-bit	1pxl/clk 8-bit	1pxl/clk 6-bit	TFT
56	PD10	O	EG6	EG4	G6	G4	
57	PD9	O	EG5	EG3	G5	G3	
62	PD8	O	EG4	EG2	G4	G2	
63	PD7	O	EG3	EG1	G3	G1	
64	PD6	O	EG2	EG0	G2	G0	
66	PD5	O	ER7	EG5	R7	R5	
67	PD4	O	ER6	ER4	R6	R4	
68	PD3	O	ER5	ER3	R5	R3	
69	PD2	O	ER4	ER2	R4	R2	
70	PD1	O	ER3	ER1	R3	R1	
71	PD0	O	EG2	ER0	R2	R0	
43	PdispE	O	This output provides a panel display enable signal that is active when flat panel data is valid.				
74	PHS	O	This output provides the panel line clock signal.				
73	PVS	O	This output provides the frame start signal.				
44	PCLKA	O	This output is used to drive the flat panel shift clock.				
45	PCLKB	O	Same as PCLKA above. The polarity and the phase of this signal are independently programmable.				
75	Pbias	O	This output is used to turn on/off the panel bias power or controls backlight.				
76	Ppwr	O	This output is used to control the power to a flat panel.				

Table 5. Test Pins

PIN #	Name	I/O	Description
3	PSCAN	I	Enable automatic PCB assembly test. When this input is pulled high, the automatic PCB assembly test mode is entered. An internal pull-down resistor drives this input low for normal operation.
155	SCAN_IN1	I	Scan input 1 used for automatic PCB assembly tesing.
157	SCAN_IN2	I	Scan input 2 used for automatic PCB assembly tesing.
159	SCAN_OUT1	O	Scan output 1 used for automatic PCB assembly tesing.
160	SCAN_OUT2	O	Scan output 2 used for automatic PCB assembly tesing.
153	Reserved		
154	Reserved		

Table 6. VDD / VSS for Core Circuitry, Host Interface, and Panel/Memory Interface

PIN #	Description
65, 40, 33, 12	PVDD4~PVDD1 for panel / memory interface. Connect to +3.3V. Must be the same voltage as the CVDD's
149, 108, 58, 21, 11	SRVDD2-1, CVDD4, CVDD2-1 for core circuitry. Connect to +3.3V. Must be the same voltage as the PVDD's.
158, 151, 140, 126, 114, 72, 61, 49, 41, 30, 18, 8, 1	Digital grounds for core circuiry and panel / memory interface.

1.4 System-level Block Diagram

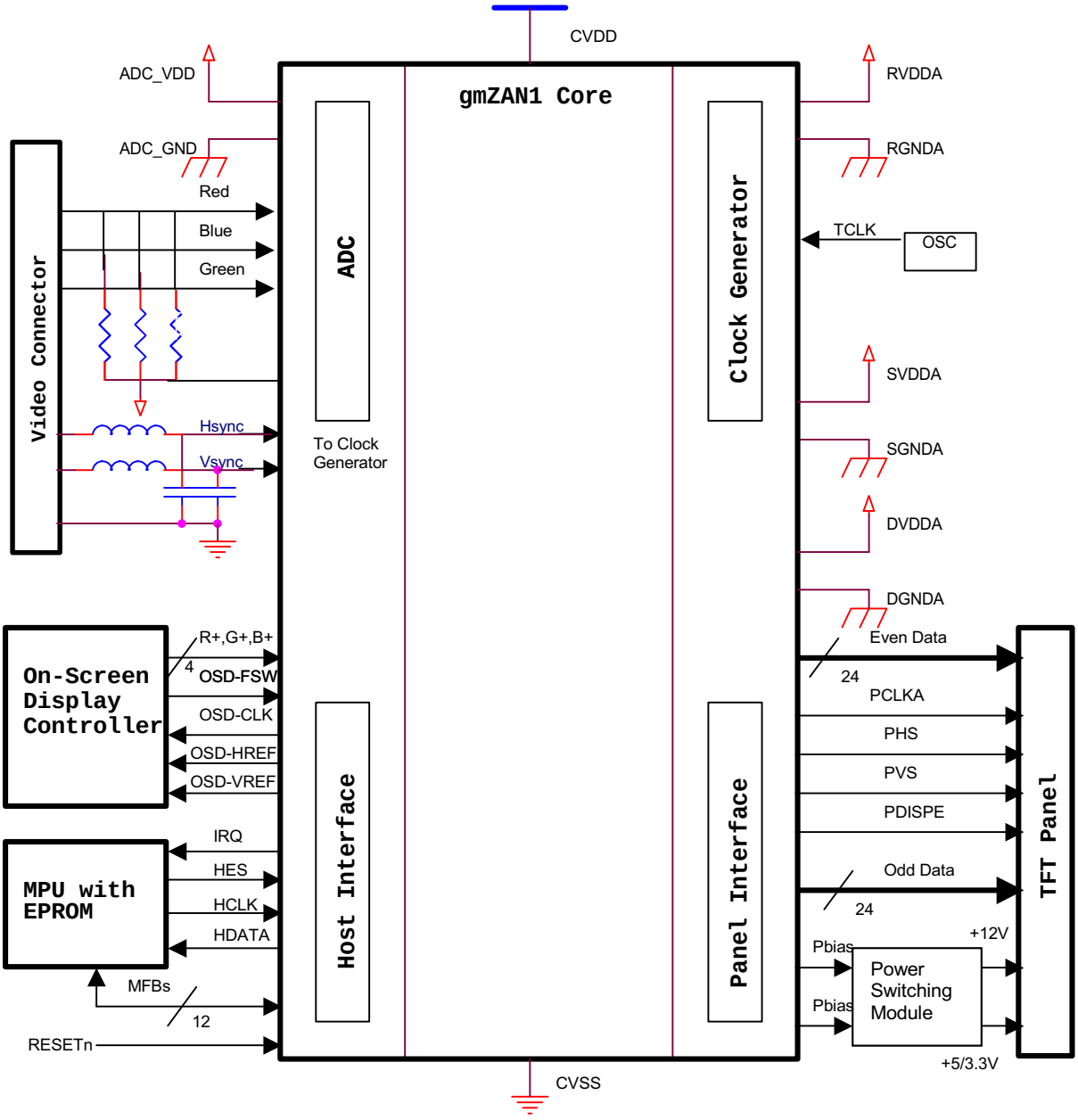


Figure 2. Typical Stand-alone Configuration

1.5 Operating Modes

The Source Clock (also called SCLK in this document) and the Panel Clock are defined as follows:

- The Source Clock is the sample clock regenerated from the input Hsync timing (called clock recovery) by SCLK DDS (direct digital synthesis) and the PLL.
- The Panel Clock is the timing clock for panel data at the single pixel per clock rate. The actual PCLK to the panel may be one-half of this frequency for double-pixel panel data format. When its frequency is different from that of source clock, the panel clock is generated by Destination Clock (or DCLK) DDS/PLL.

There are six display modes: Native, Slow DCLK, Zoom, Downscaling, Destination Stand Alone, and Source Stand Alone.
Each mode is unique in terms of:

- Input video resolution vs. panel resolution
- Source Clock frequency / Panel Clock frequency ratio
- Source Hsync frequency / Panel Hsync frequenc ratio
- Data source (analog RGB, panel background color, on-chip pattern generator

1.5.1 Native

Panel Clock frequency = Source Clock frequency
Panel Hsync frequency = Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution and the input data clock frequency is within the panel clock frequency specification of the panel being used.

1.5.2 Slow DCLK

Panel Clock frequency < Source Clock frequency
Panel Hsync frequency = Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution, but the input data clock frequency is exceeds the panel clock frequency specification of the panel being used. The panel clock is scaled to the Source Clock, and the internal data buffers are used to spread out the timing of the input data by making use of the large CRT blanking time to extends the panel horizontal display time.

1.5.3 Zoom

Panel Clock frequency > Source Clock frequency
Panel Hsync frequency > Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is less than the panel resolution. The input data clock is then locked to the pnael clock, which is at a higher frequency. The input data is zoomed to the panel resolution.

1.5.4 Downscaling

Panel Clock frequency < Source Clock frequency
Panel Hsync frequency < Input Hsync frequency
Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is greater than the panel resolution, to provide enough of a display to enable the user to recover to a supported resolution. The input clock is operated at a frequency less than that of the input pixel rate(under-sampled horizontally) and the scaling filter is used to drop input lines. In this mode, zoom scaling must be disabled

1.5.5 Destination Stand Alone

Panel Clock = DCLK in open loop (not locked)
Panel Hsync frequency = DCLK frequency / (Destination Htotal register value)
Panel Vsync frequency = DCLK frequency / (Dest. Htotal register value * Dest. Vtotal register value)

This mode is used when the input is changing or not available. The OSD may still be used as in all other display modes and stable panel timing signals are produced. This mode may be automatically set when the gmZAN1 detects input timing changes that could cause out- of-spec operation of the panel.

1.5.6 Source Stand Alone

Panel Clock = DCLK in open loop (not locked to input Hsync)
Panel Hsync frequency = SCLK frequency / (Source Htotal register value)
Panel Vsync frequency = SCLK frequency / (Source Htotal register value *Source Vtotal register value)

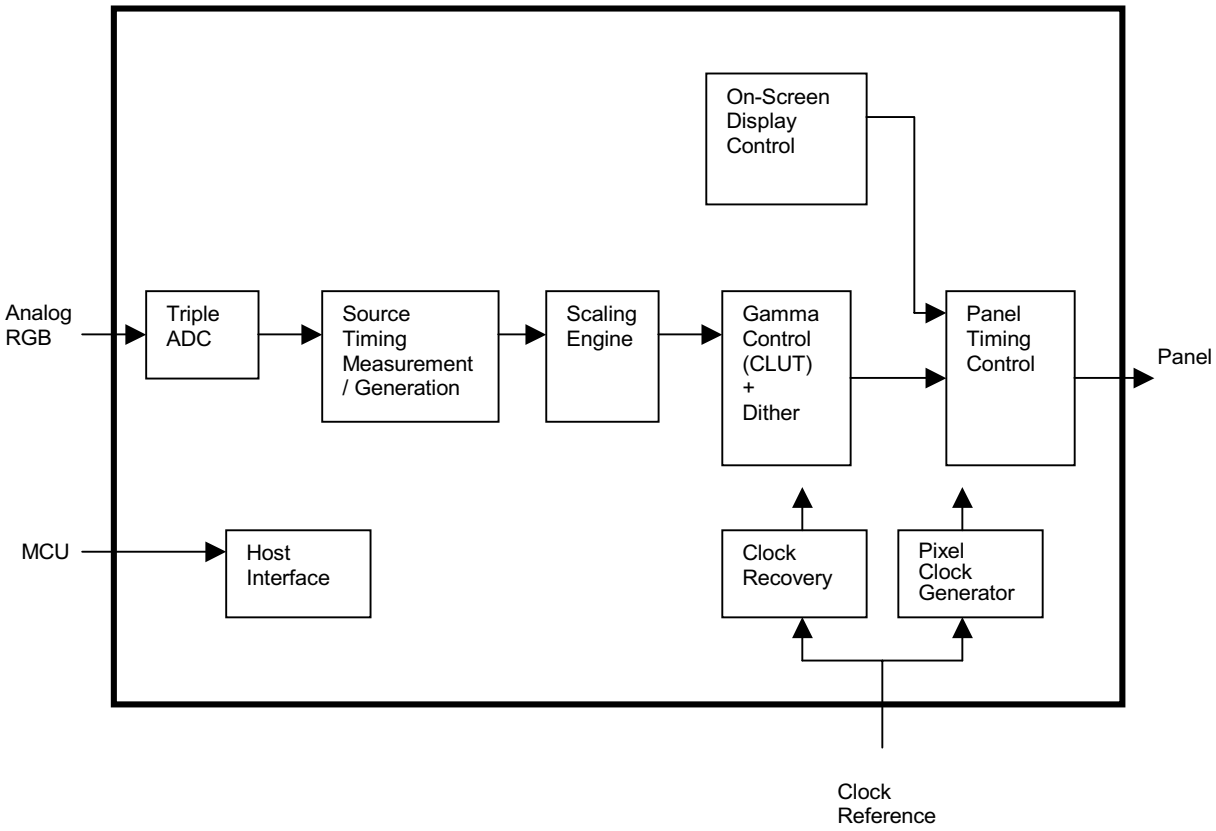
This mode is used to display the pattern generator data. This mode may be useful for testing an LCD panel on the manufacturing line (color temperature calibration, etc.).

2. FUNCTIONAL DESCRIPTION

Figure 3 below shows the main functional blocks inside the gmZAN1

2.1 Overall Architecture

Figure 3. Block Diagram for gmZAN1



2.2 Clock Recovery Circuit

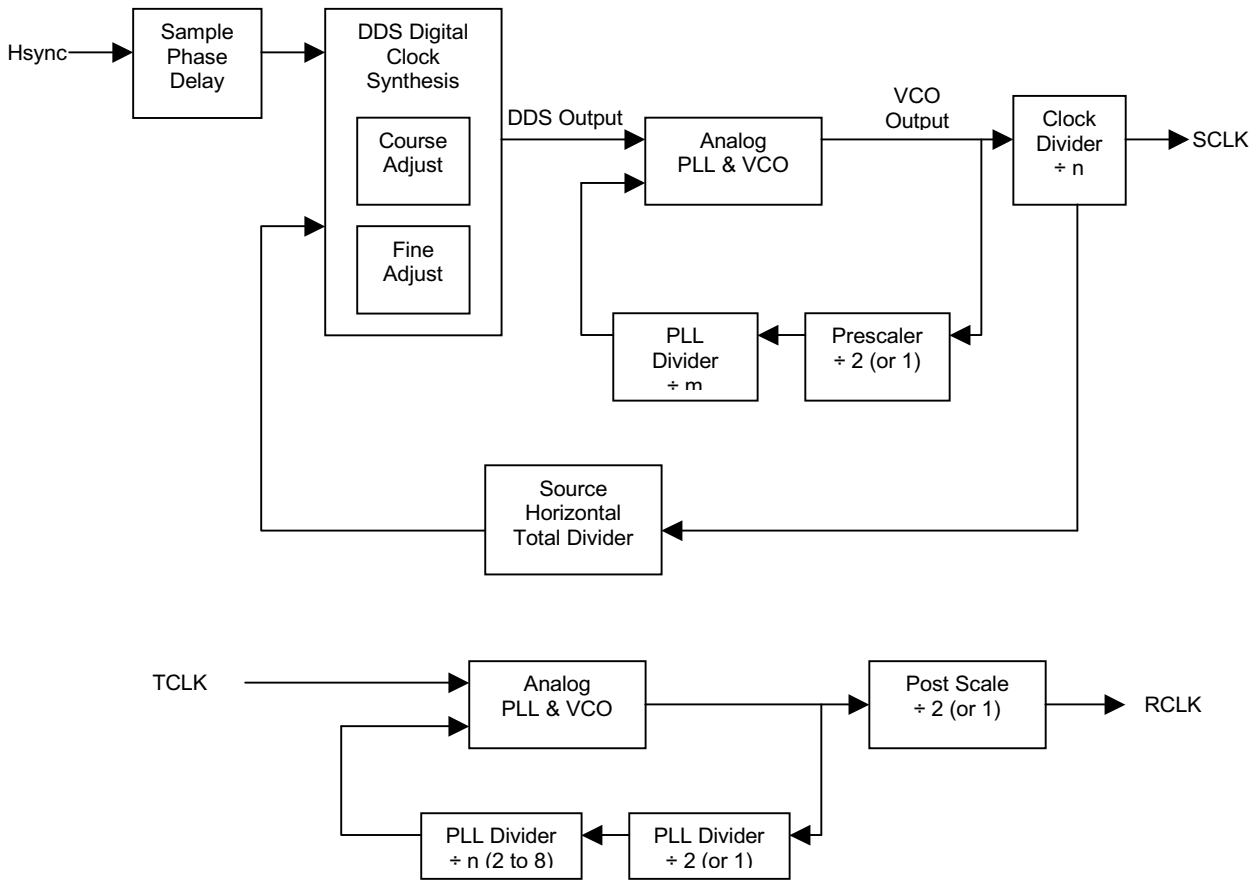
The gmZAN1 has a built-in clock recovery circuit. This circuit consists of a digital clock synthesizer and an analog PLL. The clock recovery circuit generates the clock used to sample analog RGB data (SCLK or source clock). This circuit is locked to the HSUNC of the incoming video signal. The RCLK generated from the TCLK input is used as a reference clock.

The clock recovery circuit adjusts the SCLK period so that the feedback pulse generated every SCLK period multiplied by the Source Horizontal Total value (as programmed into the registers) locks to the rising edge of the Hsync input. Even though the initial SCLK frequency and the final SCLK frequency are as far apart as 60MHz , locking can be achieved in less than 1ms across the operation voltage/temperature range.

The SCLK frequency (1/SCLK period) can be set to the range of 10-to-135 MHz. Using the DDS (direct digital synthesis) technology the clock recovery circuit can generate any SCLK clock frequency within this range.

The pixel clock (DCLK or destination clock) is used to drive a panel when the panel clock is different from SCLK (or SCLK/2). It is generated by a circuit virtually identical to the clock recovery circuit. The difference is that DCLK is locked to SCLK while SCLK is locked to the Hsync input. DCLK frequency divided by N is locked to SCLK frequency divided by M. The value M and N are calculated and programmed in the register by firmware. The value M should be close to the Source Htotal value.

Figure 4. Clock Recovery Circuit



The table below summarizes the characteristics of the clock recovery circuit.

Table 7. Clock Recovery Characteristics

	Minimum	Typical	Maximum
SCLK Frequency	10MHz		135 MHz
Sampling Phase Adjustment		0.5 ns/step, 64 steps	

Patented digital clock synthesis technology makes the gmZAN1 clock circuits very immune to temperature/voltage drift.

2.2.1 Sampling Phase Adjustment

The ADC sampling phase is adjusted by delaying the Hsync input at the programmable delay cell inside the gmZAN1. The delay value can be adjusted in 64 steps, 0.5 ns/step. The accuracy of the sampling phase is checked by the gmZAN1 and the "score" can be read in a register. This feature will enable accurate auto-adjustment of the ADC sampling phase.

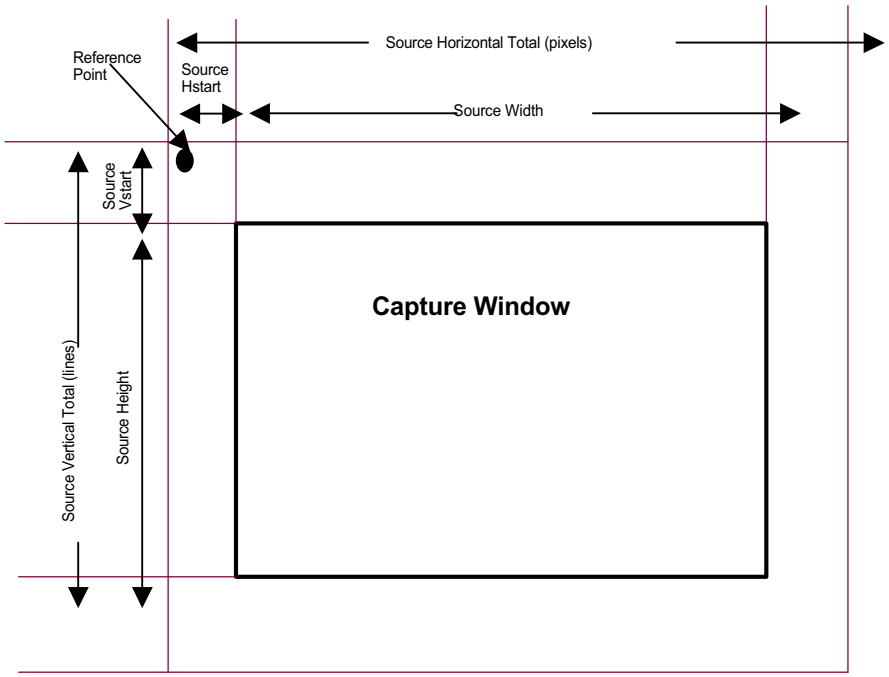
2.2.2 Source Timing Generator

The STG module defines a capture window and sends the input data to the data path block. The figure below shows how the window is defined.
For the horizontal direction, it is defined in SCLKs (equivalent to a pixel count). For the vertical direction, it is defined in lines.
All the parameters in the figure that begin with "Source" are programmed into the gmZAN1 registers.
Note that the vertical total is solely determined by the input.
The reference point is as follows:

- The first pixel of a line: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line of a frame: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

The gmZAN1 also supports the use of analog composite sync and digital sync signals as described in Section 2.3.2

Figure 5. Capture Window



2.3 Analog-to-Digital Converter

2.3.1 Pin Connection

The RGB signals are to be connected to the gmZAN1 chip as described in Table 8 and Table 9.

Table 8. Pin Connection for RGB Input with Hsync/Vsync

GmZAN1 Pin Name (Pin Number)	CRT Signal Name
Red+(#95)	Red
Red- (#94)	N/A (Tie to Analog GND for Red on the board)
Green+(#91)	Green
Green- (#90)	N/A (Tie to Analog GND for Green on the board)
Blue+(#87)	Blue
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)
HSYNC/CS (#150)	Horizontal Sync
VSYNC (#148)	Vertical Sync

Table 9. Pin Connection for RGB Input with Composite Sync

GmZAN1 Pin Name (Pin Number)	CRT Signal Name
Red+(#95)	Red
Red- (#94)	N/A (Tie to Analog GND for Red on the board)
Green+(#91)	Green When using Sync-On-Green this signal also carries the sync pulse.
Green- (#90)	N/A (Tie to Analog GND for Green on the board)
Blue+(#87)	Blue
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)
HSYNC/CS (#150)	Digital composite sync. Not applicable for Sync-On-Green

The gmZAN1 chip has three ADC's (analog-to-digital converters), one for each color (red, green, and blue). Table 10 summarizes the characteristics of the ADC.

Table 10. ADC Characteristics

	MIN	TYP	MAX	NOTE
RGB Track & Hold Amplifiers				
Band Width		160MHz		
Settling Time to 1/2%		8.5ns		Full Scale Input = 0.75V, BW=160MHz(*)
Full Scale Adjust Range @ R,G,B Inputs	0.45V		0.95V	
Full Scale Adjust Sensitivity		+/-1 LSB		Measured @ ADC Output (**)
Zero Scale Adjust Range				For a larger DC offset from an external video source, the AC coupling feature is used to remove the offset.
Zero Scale Adjust Sensitivity		+/-1 LSB		Measured @ ADC Output
ADC+RGB Track & Hold Amplifiers				
Sampling Frequency (fs)	20MHz		110MHz	
DNL			+/- 0.9LSB	fs = 80 MHz
INL		+/- 1.5LSB		fs = 80 MHz
Channel to Channel Matching		+/- 0.5LSB		
Effective Number of Bits (ENOB)		7 Bits		fin = 1MHz, fs=80 MHz Vin= -1db below full scale=0.75V
Power Dissipation		400mW		fs=110 MHz, Vdd=3.3V
Shut Down Current			100uA	

(*) Guaranteed by design (**) Independent of full scale R,G,B input

The gmZAN1 ADC has a built-in clamp circuit. By inserting series capacitors (about 10 nF) the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

2.3.2 Sync. Signal Support

The gmZAN1 chip supports digital separate sync (Hsync/Vsync), digital composite sync, and analog composite sync (also known as sync-on-green). All sync types are supported without external sync separation / extraction circuits.

Digital Composite Sync
The types of digital composite sync inputs supported are:
- OR/AND type: No Csync pulses toggling during the vertical sync period
- XOR type: Csync polarity changes during the vertical sync period

The gmZan1 provides enough sync status information for the firmware to detect the digital composite sync type.

Sync-On-Green (Analog Composite Sync)
The voltage level of the sync tip during the vertical sync period can be either –0.3V or 0V

2.3.3 Display Mode Support

A mode calculation utility (MODECALC.EXE) provided by Genesis Microchip may be run before compilation of the firmware to determine which input modes can be supported. Refer to firmware documents for more details.

2.4 Input Timing Measurement

As described in section 2.2.2 above, input data is sent from the analog-to-digital converter to the source timing generator (STG) block. The STG block defines a capture window (Figure5).

The input timing measurement block consists of the source timing measurement (STM) block and interrupt request (IRQ) controller. Input timing parameters are measured by the STM block and stored in registers. Some input conditions will generate an IRQ to an external micro-controller. The IRQ generating conditions are programmable.

2.4.1 Source Timing Measurement

When it receives the active CRT signal (R,G,B and Sync signals) the Source Timing Measurement unit begins measuring the horizontal and vertical timing of the incoming signal using the sync signals and TCLKi as a reference. Horizontal measurement occurs by measuring a minimum and a maximum value for each parameter to account for TCLKi sampling granularity. The measured value is updated every line. Vertical parameters are measured in terms of horizontal lines. The trailing edge of the Hsync input is used to check the polarity of the Vsync input.
The table below lists all the parameters that may be read in the source timing measurement (STM) registers of the gmZAN1.

Table 11. Input Timing Parameters Measured by the STM Block

Parameter	Unit	Updated at:
HSYNC Missing	N/A	Every 4096 TCLKs and every 80ms (2-bits)
VSYNC Missing	N/A	Every 80ms
HSYNC/VSYNC Timing Change	N/A	When the horizontal period delta or the vertical period delta to the previous line / frame exceeds the threshold value (programmable).
HSYNC Polarity	Positive/Negative	After register read
VSYNC Polarity	Positive/Negative	Every frame
Horizontal Period Min/Max	TCLKs and SCLKs	After register read
HSYNC High Period Min/Max	TCLKs	After register read
Vertical Period	Lines	Every frame
VSYNC High Period	Lines	Every frame
Horizontal Display Start	SCLKs	Every frame
Horizontal Display End	SCLKs	Every frame
Vertical Display Start	Lines	Every frame
Vertical Display End	Lines	Every frame
Interlaced Input Detect	N/A	Every frame
CRC Data/Line Data	N/A	Every frame
CSYNC Detect	N/A	Every 80ms

The display start/end registers store the first and the last pixels/lines of the last frame that have RGB data above a programmed threshold.
The reference point of the STM block is the same as that of the source timing generator (STG) block:

- The first pixel: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

The CRC data and the line data are used to detect a test pattern image sent to the gmZAN1 input port.

2.4.2 IRQ Controller

Some input timing conditions can cause the gmZAN1 chip to generate an IRQ. The IRQ-generating conditions are programmable, as given in the following table.

Table 12. IRQ-Generation Conditions

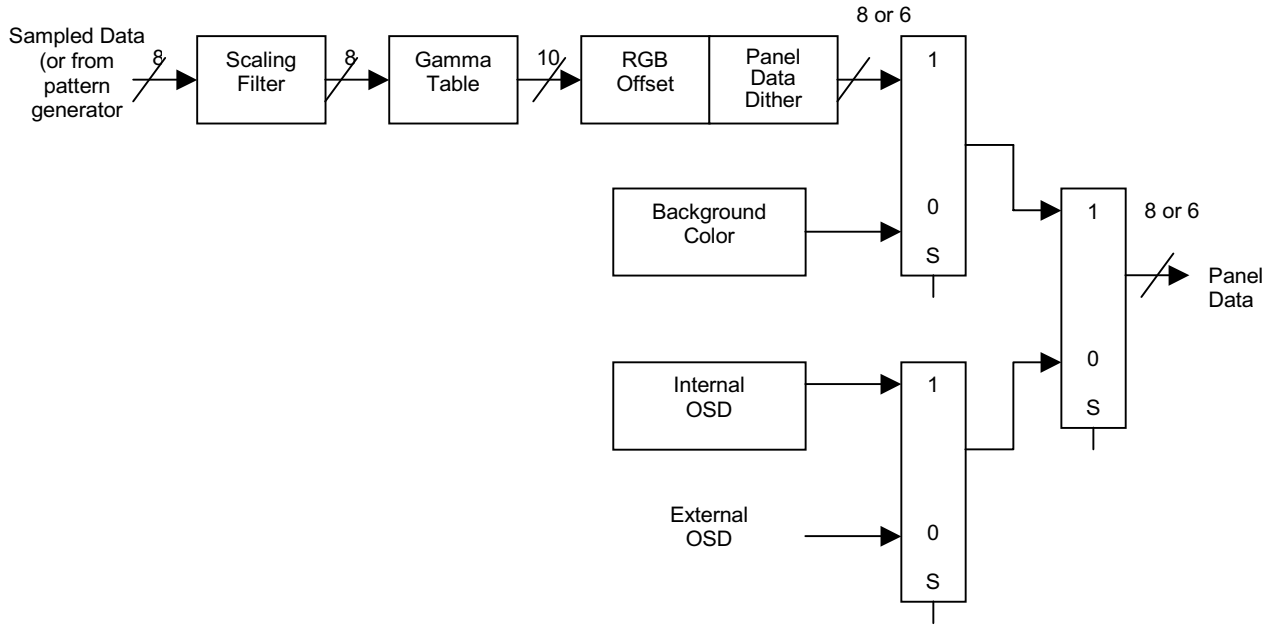
IRQ Event	Remark
Timing Event	One of the three events: ● Leading edge of Vsync input, ● Panel line count (the line count is programmable), ● Every 10ms Only one event may be selected at a time.
Timing Change	Any of the following timing changes: ● Sync loss, ● DDS tracking error beyond threshold, ● Horizontal/vertical timing change beyond threshold Threshold values are programmable.

Reading the IRQ status flags will not affect the STM registers.
Note that if a new IRQ event occurs while the IRQ status register is being read, the IRQ signal will become inactive for minimum of one TCLK period and then get re-activated. The polarity of the IRQ signal is programmable.

2.5 Data Path

The data path block of gmZAN1 is shown in Figure 6.

Figure 6. gmZAN1 Data Path



2.5.1 Scaling Filter

The gmZAN1 scaling filter uses an advanced adaptive scaling technique proprietary to Genesis Microchip Inc. and provides high quality scaling of real time video and graphics images. This is Genesis' third generation scaling technology that benefits from the expertise and feedback gained by supporting a wide range of solutions and applications.

2.5.2 Gamma Table

The gamma table is used to adjust the RGB data for the individual display characteristics of the TFT panel. The overall gamma of the display may be set, as well as separate corrections for each of the three display channels. In addition, the gamma table may be used for contrast, brightness, and white balance (temperature) adjustments. The lookup table has an 8-bit input (256 different RGB entries) and produces a 10-bit output.

2.5.3 RGB Offset

The RGB offsets provide a simple shift (positive or negative) for each of the three color channels. This may be used as a simple brightness adjustment within a limited range. The data is clamped to zero for negative offsets, and clamped to FFh for positive offsets. This adjustment is much faster than recalculating the gamma table, and could be used with the OSD user controller to provide a quick brightness adjust. An offset range of plus 127*4 to minus 127*4 is available.

2.5.4 Panel Data Dither

For TFT panels that have fewer than eight bits for each R,G,B input, the gmZAN1 provides ordered and random dithering patterns to help smoothly shade colors on 6-bit panels.

2.5.5 Panel Background Color

A solid background color may be selected for a border around the active display area. The background color is most often set to black.

2.6 Panel Interface

The gmZAN1 chip interfaces directly with all of today's commonly used active matrix flat panels with 640x480, 800x600 and 1024x768 resolutions. The resolution and the aspect ratio are NOT limited to specific values.

2.6.1 TFT Panel Interface Timing Specification

The TFT panel interface timing parameters are listed in Table 13 below. Refer to three timing diagrams of Figure 7 and Figure 8 for the timing parameter definition. All aspects of the gmZAN1 interface are programmable. For horizontal parameters, Horizontal Display Enable Start, Horizontal Display Enable End, Horizontal Sync Start and Horizontal Sync End are programmable. Vertical Display Enable Start, Vertical Display Enable End, Vertical Sync Start and Vertical Sync End are also fully programmable.
In order to maximize panel data setup and hold time, the panel clock (PCLKA, PCLKB) output skew is programmable. In addition, the current drive strength of the panel interface pins is programmable.

Table 13. gmZAN1 TFT Panel Interface Timing

Signal Name			Min	Typical	Max	Unit
PVS	Period	t1	0	16.67	2048 -	lines ms
	Frequency			60	-	Hz
	Front porch	t2	0		2048	lines
	Back porch	t3	0		2048	lines
	Pulse width	t4	0		2048	lines
	PdispE	t5	0	Panel height	2048	lines
	Disp. Start from VS	t6	0		2048	lines
	PVS set up tp PHS	t18	1		2048	PCLK *1
	PVS hold from PHS	t19	1		2048	PCLK *1
PHS	Period	t7	0		2048 [1024	PCLK *1
	Front porch	t8	0		2048	PCLK *1
	Back porch	t9	0		2048	PCLK *1
	Pulse width	t10	0		2048	PCLK *1
	PdispE	t11	0	Panel width	2048 [1024]	PCLK *1
	Disp. Start fom HS	t12	0		2048	PCLK *1
PCLKA, PCLKB*4	Frequency	t13			120 [60]	MHz
	Clock (H) *2	t14	DCLK/2-3 [DCLK-3]		DCLK/2-2 [DCLK-2]	ns
	Clock (L) *2	t15	DCLK/2-3 [DCLK-3]		DCLK/2-2 [DCLK-2]	ns
	Type		-	One pxl/clock [two pxl/clock]	-	
Data	Set up *3	t16	DCLK/2-5 [DCLK-5]		DCLK/2-2 [DCLK-2]	ns
	Hold *3	t17	DCLK/2-5 [DCLK-5]		DCLK/2-2 [DCLK-2]	ns
	width		3 bits	18 bits [36 bits]	24 bits [48 bits]	bits/pixel

NOTE: Numbers in [ ] are for two pixels/clock mode.

NOTE: The drive current of the panel interface signals is programmable as shown in Table 1. The drive current is to be programmed through the API upon chip initialization. Output current is programmable from 2 mA to 20mA in increments of 2 mA. Drive strength should be programmed to match the load presented by the cable and input of the panel. Values shown are based on a loading of 20pF and a drive strength of 8 mA.

NOTE *1: The PCLK is the panel shift clock.

NOTE *2: The DCLK stands for Destination Clock (DCLK) period. Is equal to:

-PCLK period in one pixel/clock mode,

-twice the PCLK period in two pixels/clock mode.

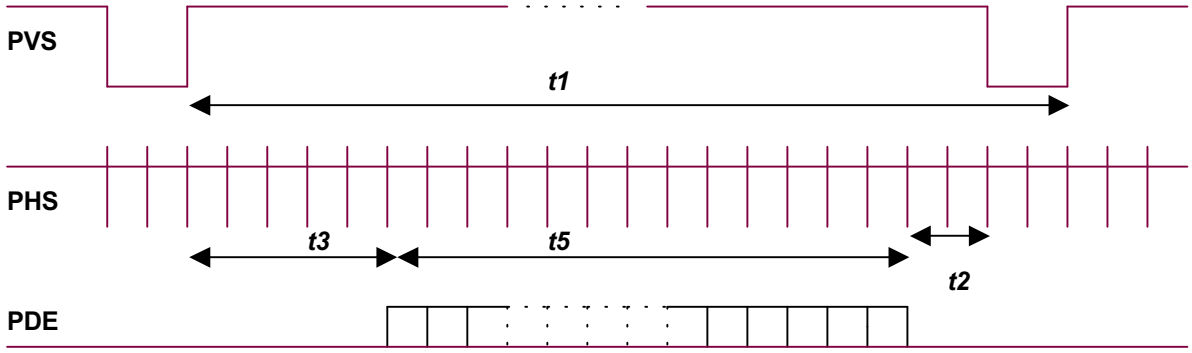
NOTE *3: The setup/hold time spec. for PCLK also applies to PHS and PdispE. The setup time (t16) and the hold time (t17) listed in this table are for the case in which no clock-to-data skew is added. The PVS/PHS/PdispE/Pdata signals are asserted on the rising edge of the PCLK. The polarity of the PCLK and its skew are programmable. Clock to Data skew can be adjusted in sixteen 800-ps increments. In combination with the PCLK polarity inversion, the clock-to-data phase can be adjusted in total of 31 steps.

NOTE *4: The polarity of the PCLKA and the PCLKB are independently programmable.

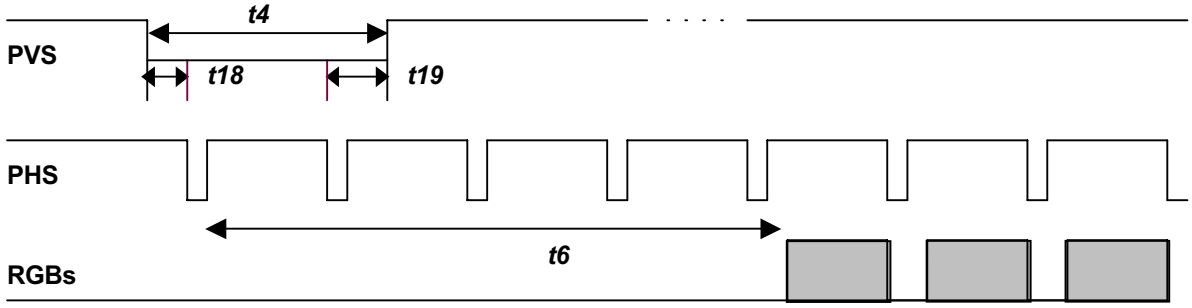
The micro controller must have all the timing parameters of the panel used for the monitor. The parameters are to be stored in a non-volatile memory. As can be seen from this table, the wide range of timing programmability of the gmZAN1 panel interface makes it possible to support various kinds of panels known today:

Figure 7. timing Diagrams of the TFT Panel Interface (One pixel per clock)

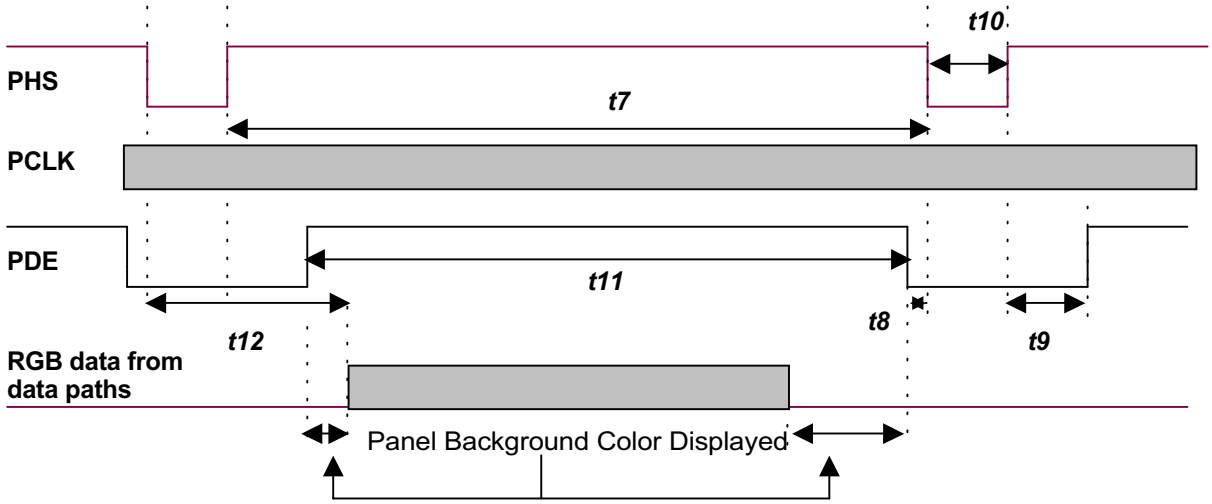
(a) Vertical size in TFT



(b) Vsync width and display position in TFT



(c) Horizontal size in TFT



(d) Hsync width in TFT

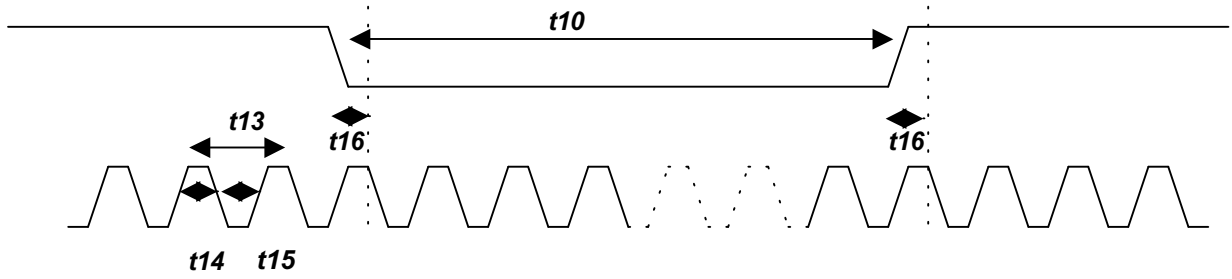
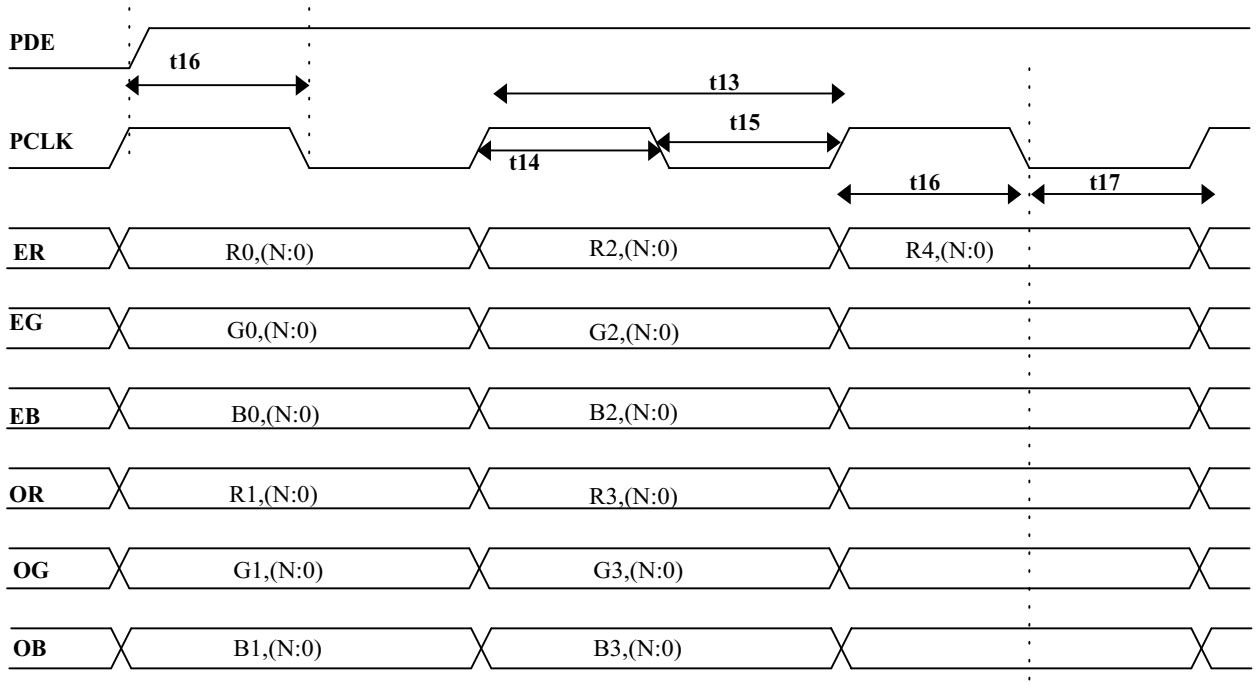
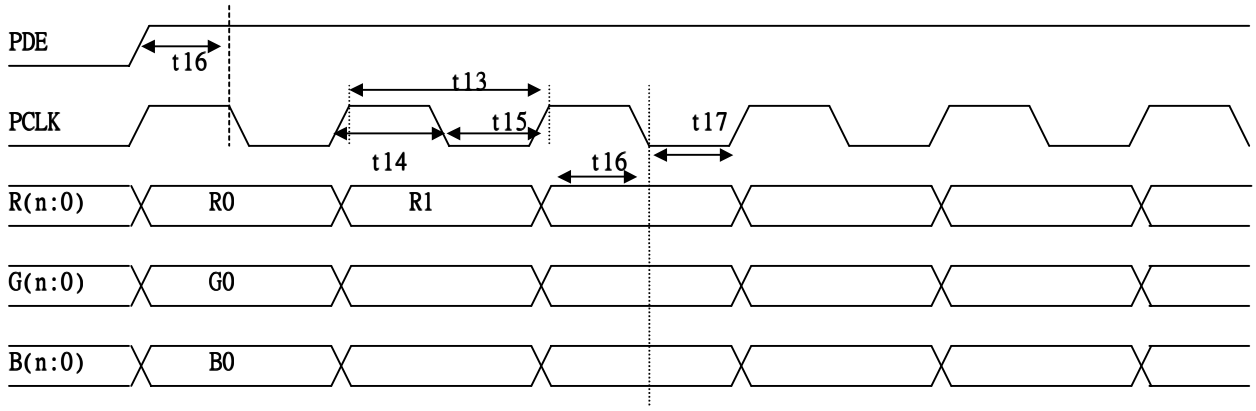


Figure 8. Data latch timing of the TFT Panel Interface

(a) Two pixel per clock mode in TFT



(b) One pixel per clock mode in TFT



2.6.2 Power Manager

LCD panels require logic power, panel bias power, and control signals to be sequenced in a specific order, otherwise severe damage may occur and disable the panel permanently. The gmZAN1 has a built in power sequencer (Power Manager) that prevents this kind of damage.
The Power Manager controls the power up/down sequences for LCD panels within the four states described below. See the timing diagram Figure 9.

2.6.2.1 State 0 (Power Off)

The Pbias signal and Ppower signal are low (inactive). The panel controls and data are forced low. This is the final state in the power down sequence. PM is kept in state 0 until the panel is enabled.

2.6.2.2 State 1 (Power On)

Intermediate step 1. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is forced low (inactive).

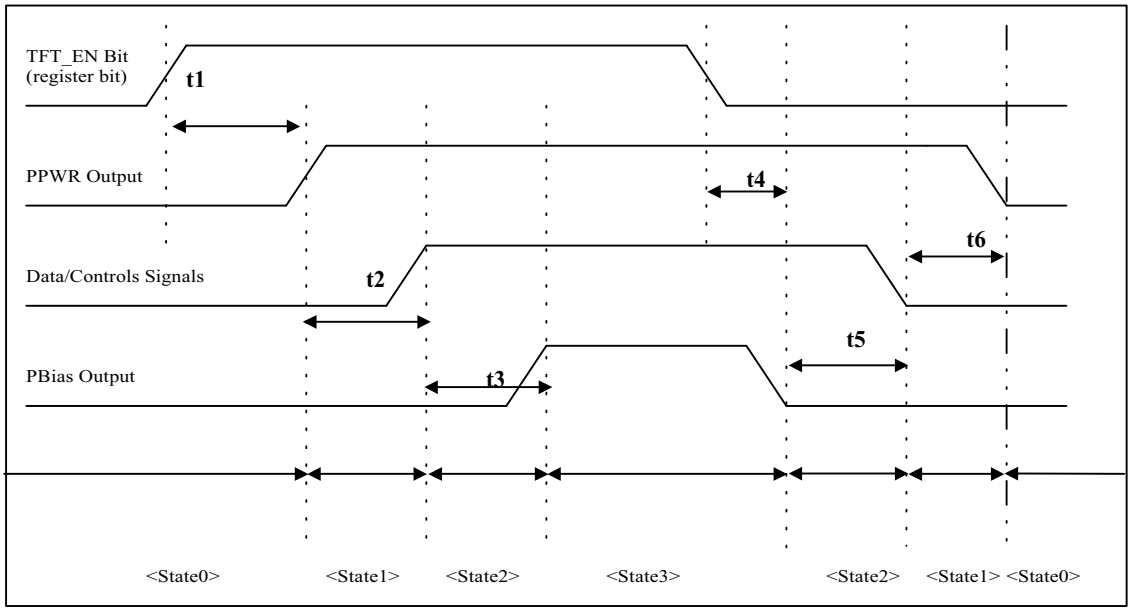
2.6.2.3 State 2 (Panel Drive Enabled)

Intermediate step 2. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is active.

2.6.2.4 State 3 (Panel Fully Active)

This is the final step in the power up sequence, with Ppower and Pbias high (active), and the panel interface active. PM is kept in this state until the internal TFT_Enable signal controlled by Panel Control register is disabled. The panel can be disabled through either an API call under program control or automatically by the gmZAN1 to prevent damage to the panel.

Figure 9. Panel Power Sequence



In Figure 9 above, t2=t6 and t3=t5. t1,t2,t3 and t4 are independently programmable from one to eight steps in length. The length of each step is in the range of 511 * X* (TCLKi cycle) or (TCLKi cycle) * 32193 *X, where X is any positive integer value equal to or less than 256. TCLKi is the reference clock to the gmZAN1 chip, and ranges from 14.318 MHz to 50 MHz in frequency. This programmability provides enough flexibility to meet a wide range of power sequencing requirements by various panels.

2.6.3 Panel Interface Drive Strength

As mentioned previously, the gmZAN1 has programmable output pads for the TFT panel interface. Three groups of panel interface pads (panel clock, data, and control) are independently controllable and are programmed using API calls. See the API reference manual for details.

Table 14. Panel Interface Pad Drive Strength

Value (4 bits)	Drive Strength in mA
0	Outputs are in tri-state condition
1	2mA
2	4mA
3	6mA
4	8mA
5	10mA
6	12mA
7	14mA
8	16mA
9	18mA
10,11,12,13,14,15	20mA

2.7 Host Interface

The host microcontroller interface of the gmZAN1 has two modes of operation: gmB120 compatible mode, and a 4-bit serial interface mode.

- GmB120 compatible mode-Four signals consisting of 1 data bit, a frame synchronization signal, a clock signal and an Interrupt Request signal (IRQ). This mode is entered when a pull-down resistor is not connected to MFB6(pin number 106).
- 4-bit serial interface mode-Same as gmB120 compatible mode with the addition of three data bits so that four data bits are transferred on each clock edge. This mode is entered when a (10K ohm) pull-down resistor is connected to MFB6(pin number 106).

When the chip is configured for 4-bit host interface, MFB9:7 are used as HDATA3:1 and HDATA is used as HDATA0. For instruction, Read Data, or Write Data, the data order is D3:0, D7:4, D11:8, The burst mode operation then uses three clocks (instead of twelve) for each 12-bit data (or address) transmission.

In both modes, a reset pin sets the chip to a known state when the pin is pulled low. The RESETn pin must be low for at least 100ns after the CVDD has become stable (between +3.15V and +3.45V) in order to reset the chip to a known state.

The gmZAN1 chip has an on-chip pull-down resistor in the HFS input pad. No external pull-up is required. The signal stays low until driven high by the microcontroller.

2.7.1 Serial Communication Protocol

In the serial communication between the microcontroller and the gmZAN1, the microcontroller always acts as an initiator while the gmZAN1 is always the target. The following timing diagram describes the protocol of the serial channel of the gmZAN1 chip.

Figure 10. Timing Diagram of the gmZAN1 Serial Communication

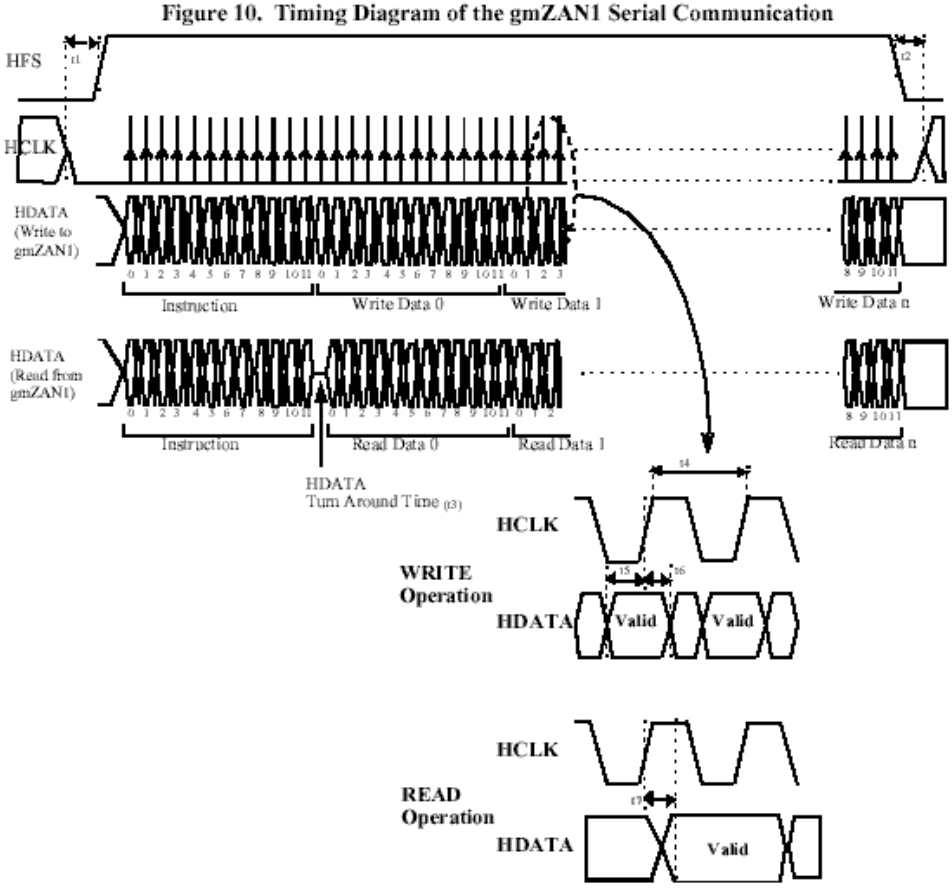


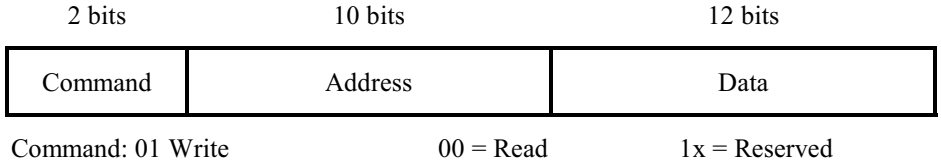
Table 15 summarizes the serial channel specification of the gmZAN1. Refer to Figure 10 for the timing parameter definition.

Table 15. gmZAN1 Serial Channel Specification

Parameter	Min.	Typ.	Max.
Word Size (Instruction and Data)	---	12 bits	---
HCLK low to HFS high (t1)	100 ns		
HFS low to HCLK inactive (t2)	100 ns		
HDATA Write to Read Turnaround Time (t3)	1 HCLK cycle		1 HCLK cycle
HCLK cycle (t4)	100 ns		
Data in setup time (t5)	25 ns		
Data in hold time (t6)	25 ns		
Data out valid (t7)	5 ns		10

In the read operation, the microcontroller (Initiator) issues an instruction lasting 12 HCLKs. After the last bit of the command is transferred to the gmZAN1 on the 12th clock, the microcontroller must stop driving data before the next rising edge of HCLK at which point the gmZAN1 will start driving data. At the 13th rising edge of HCLK, the gmZAN1 will begin driving data.

Figure 11. Serial Host Interface Data Transfer Format



Note that when the chip is configured for a 4-bit host interface, MFB9:7 are used as HDATA 3:1 and HDATA is used as HDATA0. The command and address information are transferred as Address 1:0+Command1:0, Address5:2 and Address9:6. The data information is transferred as Data3:0,Data 7:4, Data 11:8. Thus, in this mode the HDATA pin carries Command0, Address2, Address6, Data0, Data4 and Data8.
On the gmZAN1 reference design board, the microcontroller toggles the HCLK and HDATA lines under program control. Genesis Microchip provides API calls to facilitate communication between the microcontroller and the gmZAN1. Refer to the API reference manual for details.

2.7.2 Multi-Function Bus (MFB)

The Multi-Function Bus provides additional 12 pins that are used as general purpose input and output (GPIO) pins. Each pin can be independently configured as input or output.
MFB pins 9 through 5 have special functions:

- When a 10K ohm pull-down resistor is connected to MFB6 (MFB6 has an internal pull-up resistor) MFB9:7 are used as host data bits HDATA3:1.
- When a 10K ohm pull-down resistor is connected to MFB5 (MFB5 has an internal pull-up resistor) a crystal can be placed between XTAL and TCLK instead of using an external oscillator for the TCLK input.

Note that all pins on the multi-function bus MFB11:0 are internally pulled-up.

2.8 On-Screen Display Control

The gmZAN1 chip has a built-in OSD (On-Screen Display) controller with an integrated font ROM. The chip also supports an external OSD controller for monitor vendors to maintain a familiar user interface.
The internal and external OSD windows may be displayed anywhere the panel Display Enable is active, regardless of whether the panel would otherwise display panel background color or active data.

2.8.1 OSD Color Map

Both the internal and external OSD display use a 16 location SRAM block for the color programming. Each color location is a twelve-bit value that defines the upper four bits of each of the 8 bit Red, Blue and Green color components as follows:

- D3:0 Blue; D7:4 of blue component of color
- D7:4 Green; D7:4 of green component of color
- D11:8 Red; D7:4 of red component of color

To extend the 4-bit color value programmed to the full 8 bits the following rule is applied: if any of the upper four color bits are a "1", then R (G, B) data 3:0=1111b, otherwise R (G, B) data 3:0=0000b

2.8.2 On-Chip OSD Controller

The internal OSD uses a block of SRAM of 1536x12 bits and a ROM of 1024x12 bits. The SRAM is used for both the font data and the character-codes while the ROM is used to store the bit data for 56 commonly used characters. The font data is for 12 pixel x 18 line characters, one bit per pixel. The font data starts at address zero. The character-codes start at any offset (with an address resolution of 16) that is greater than the last location at which font data has been written . It is the programmer's responsibility to ensure that there is no overlap between fonts and character-codes. This implementation results in a trade-off between the number of unique fonts on-screen at any one time and the total number of characters displayed. For example, one configuration would be 98 font maps (56 fonts in ROM and 42 fonts in SRAM) and 768 characters (e.g. in a 24x32 array).

The on-chip OSD of the gmZAN1 can support a portrait mode (in which the LCD monitor screen is rotated 90 degrees). In this portrait mode, all the fonts must be loaded in the SRAM, because the ROM stores fonts for a landscape mode (typical orientation) only. The font size in the portrait mode is 12 pixels by 12 lines. As is the case in landscape mode, the SRAM is divided into a font storage area and a character code storage area. For example, 64 fonts can be stored in RAM and an OSD window of 768 characters (such as 24x32) can still be displayed.

The first address of SRAM to be read for the first character displayed (upper left corner of window)is also programmable, with an address resolution of 16 (8-bits as the top bits of the 12-bit SRAM address). The character-code is a 12-bit value used as follows:

- D6:0 font-map select, this is the top seven bits of the address for the first line of font bits
- D8:7 Background color, 00=bcolor0, 01=bcolor1, 10=bcolor2, 11=transparent background
- D10:9 Foreground color (0, 1, 2 or 3)
- D11 Blink enable if set to 1, otherwise no blink

Although the OSD color map has room for sixteen colors, only seven are used by the internal OSD: three background colors and four foreground colors.

The blink rate is based on either a 32 or 64 frame cycle and the duty cycle may be selected as 25/75/50/50% or 75/25%. The 2-bit foreground and background attributes directly select the color (there is no indirect "look-up", i.e. there is no TMASK function). The 2560 addresses of the ROM/SRAM are mapped as 10 segments of 256 contiguous addresses each, to the OSD memory page of 100h-1FFh in the host interface. A 4-bit register value selects the segment to map to the host R/W page.

The character cell height and width are programmable from 5-66 pixels or 2-65 lines. The X/Y offset of the font bit-map upper-left pixel relative to the upper-left pixel of the character cell is also programmable from 0-63 (pixels or lines). The OSD window height and width in characters/rows is programmable from 1-64.

The Start X/Y position for the upper left corner of the OSD window is programmable (in panel pixels and lines) from 0-2047. There is an optional window border (equal width on all four sides of the window) or a window shadow (the window bottom and right side) the border is a solid color that is selected by an SRAM location as RGB444. The border width may be set as 1, 2, 4 or 8 pixels/lines. These parameters are summarized in Figure 12 and Table 16.
The Font Data D11:0 for each line is displayed with bit D11 first (leftmost) and D0 last.
The reference point for the OSD start is always the upper left corner of the Panel display, which is the start (leading edge) of Panel Display Enable for both Horizontal and Vertical timing.

The OSD Window start position sets the location of the first pixel of the OSD to display, including any border. That is; if the border is enabled, the start of the character display of the OSD is offset from the OSD start position by the width/height of the border.

To improve the appearance and make it easy to find the OSD window on the screen, the user may select optional shadowing (3D effect). The “Shadow” feature operates in the same manner as in the B120; that is, it produces a region of half intensity (scaler data) pixels of the same width and height as the OSD window, but offset to the right and down by 8 pixels/lines (the border width setting has no effect). OSD foreground and background colors always cover the OSD window region of the “shadow”, but transparent background pixels in the OSD will show the half intensity panel data. Therefore, it is not recommended to use both the “shadow” feature and transparent background OSD pixels together. The ”shadow” does not change the intensity of any panel background color over which it may be located. The border and shadow are mutually exclusive, only one may be selected at a time.

The OSD window is not affected by the scaling operation. The size will stay the same whether the source input data is scaled or not.

2.9 TCLK Input

The source timing is measured by using the TCLK input as a reference. Also, the reference clock to the on-chip PLLs are derived from the TCLK. It is therefore crucial to have a jitter-free clock reference.
Table 19 shows the requirements for the TCLK signal.

Table 19. TCLK Specification

Frequency	20 MHz to 50 MHz
Jitter	250 ps maximum
Rise Time (10% to 90%)	5 ns
Duty Cycle	40-60

There is also an option to use a crystal (instead of an oscillator) for the TCLK input. This option is selected by pulling down MFB5 and connecting the crystal between XTAL and TCLK.

3. ELECTRICAL CHARACTERISTICS

Table 20. Absolute Ratings

Parameter	Min.	Typ.	Max.	Note
PVDD			5.6 volts	
CVDD			5.6 volts	
Vin	Vss-0.5 volt		Vcc+0.5V	
Operating temperature	0 degree C		70 degree C	
Storage temperature	-65 degree C		150 degree C	
Maximum power consumption			~2W	

Table 21. DC Electrical Characteristic

Parameter	Min.	Typ.	Max.	Note
PVDD	3.15 volts	3.3 volts	3.47 volts	
CVDD	3.15 volts	3.3 volts	3.47 volts	
Vil (COMS inputs) Vil (TTL inputs)			0.3*CVDD 0.8 volts	
Vih (COMS inputs) Vih (TTL inputs)	0.7 * CVDD 2.0 volts		1.1*CVDD 5.0+0.5 volts	(1)
Voh	2.4 volts		CVDD	
Vol		0.2 volts	0.4 volts	
Input Current	-10 uA		10 uA	
PVDD operating supply current	0 mA		20 mA/pad @ 10pF	(2)
CVDD operating supply current	0 mA		500 mA	(3)

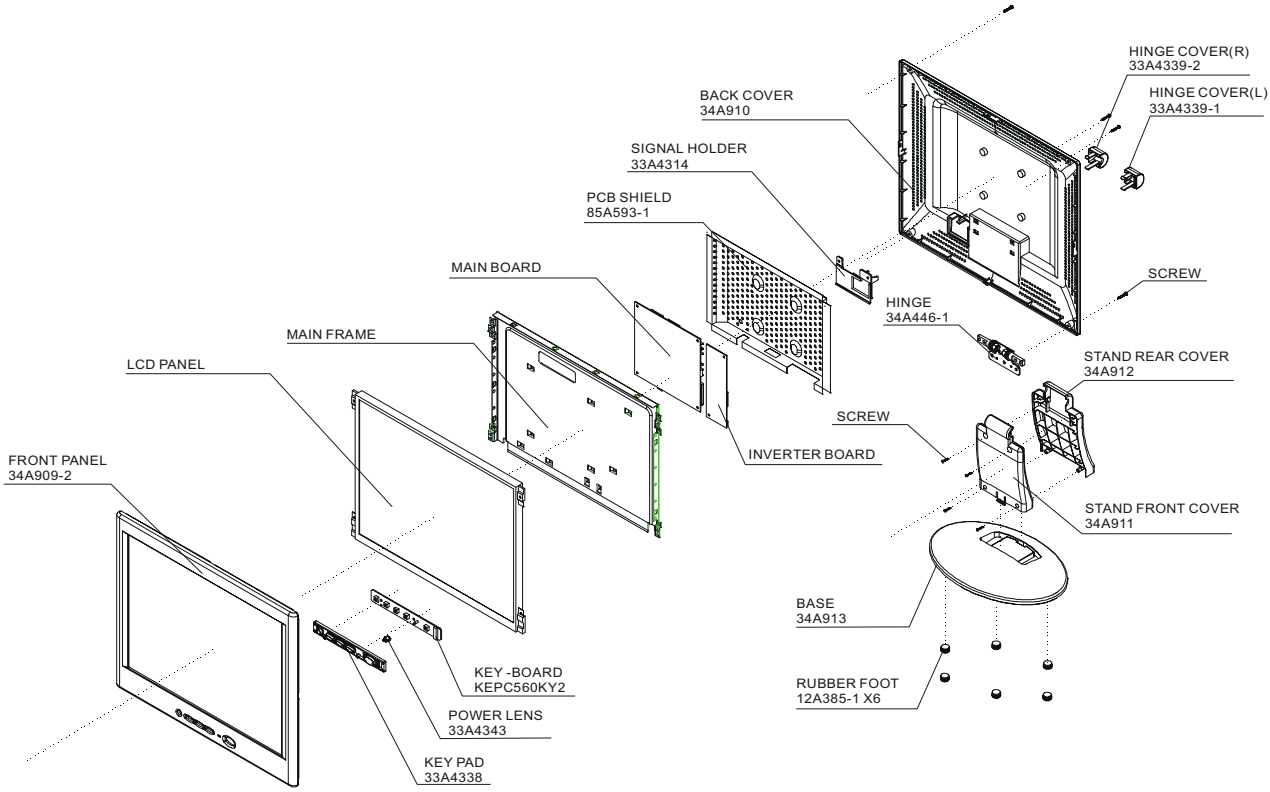
NOTE 1:5V-Tolerent TTL Input pads are as follows:

- CRT Interface: HSYNC (pin #150), VSYNC (#148)
- Host Interface: HFS (#98), HCLK (#103), HDATA (#99), RESETN (#100), MFB[11:0]: MFB11 (#123), MFB10 (#124), MFB9 (#102), MFB8 (#104), MFB7 (#105), MFB6 (#106), MFB5 (#107), MFB4 (#109), MFB3 (#110), MFB2 (#111), MFB1 (#112), MFB0 (#113)
- OSD Interface: OSD_DATA3 (#121), OSD_DATA2 (#120), OSD_DATA1 (#119), OSD_DATA0 (#118), OSD_FSW (#122)
- Non-5V-Tolerant TTL Input Pad is: TCLK(#141)

NOTE 2: When the panel interface is disabled, the supply current is 0 mA. The drive current of each pad can be programmed in the range of 2 mA to 20 mA (@capacitive loading = 10 pF)

NOTE 3: When all circuits are powered down and TCLK is stopped, the CVDD supply current becomes 0 mA.

7. MECHANICAL OF CABINET FRONT DIS-ASSEMBLY



PARTS LIST OF CABINET

LOCATION	T562KHGHJYY1N	SPECIFICATION
	CBPC562KHGY2	CONVERSION BOARD
	KEPC560KY2	KEY BOARD
	CNPC560A2	CONVERSION BOARD

12A	385	1		RUBBER FOOT
15A	5689	1		GND. CABLE CLAMP
15A	5689	2		GND CLAMP
15A	5694	2		FRAME MAIN
15A	5702	1		BRACKET HOLDER(A)
15A	5703	1		BRACKET HOLDER(B)
33A	4314	Y	L	SIGNAL HOLDER
33A	4338	Y	L	POWER KEY PAD
33A	4339	Y	1L	HINGE COVER(L)
33A	4339	Y	2L	HINGE COVER(R)
33A	4343	1		LENS
34A	909	AY	1L	FRONT PANEL
34A	910	Y	L	REAR COVER
34A	911	Y	L	STAND COVER F
34A	912	Y	L	STAND COVER B
34A	913	Y	L	BASE
37A	446	1		LCD HINGE (L501-C)
40A	155	240		ID LABEL (AX3817UT)
40A	581	695	1A	IIYAMA BAR-CODR
40A	581	695	2A	LABEL
40A	581	695	8A	STICKER (IIYAMA)
41A	401	957	1A	OWNER 'S MANUAL (AX3817UT)
44A	3231	10		MF WASHER T=9
44A	3231	11		EVA WASHER
44A	3264	1		EPS (L)
44A	3264	2		EPS (R)
44A	3264	4		CARTON (423WX158DX436H)
45A	113	1		PE BAG
45A	116	1		CLIP BAG
50A	106	1		CABLE TIE
52A	1	185	11	MIDDLE TAPE W=72mm
52A	1	208	A	ALUMINUM TAPE
52A	1	209	A	ADHESIVE TAPE 50(W)*135
52A	1	210	A	ADHESIVE TYPE
52A	1	211	A	ADHESIVE TYPE
70A	L15	10	IY	DRIVE DISK
71A	100	19		CORE W5 ZP 5×12×25
79A	L15	7	S	INVERTER BY SAMPO
80A	L15	4A	LI	ADAPTOR BY LINEARITY
85A	583	6		SOFT SHIELD
85A	593	1		PCB SHIELD
89A	173	L15	10	SIGNAL CABLE
89A	176	40	1	FFC CABLE 40P
89A	401C	18N	ISA	POWER CORD
95A	8014	5	6	HARNESS
96A	29	23	700	H.S.TUBE 0.5mm 70mm
M1A	330	4	128	SCREW M3×4
M1A	330	6	128	SCREW M3×6
M1A	330	8	128	SCREW
M1A	1740	12	128	SCREW M4×12
Q1A	330	8	120	SCREW 3×8mm
Q1A	330	8	120	SCREW 3×8mm
Q1A	340	8	128	SCREW 4×8mm
Q1A	1030	8	128	SCREW 3×8mm
750A	LCD	X82	1	SMART I.PANEL HSD150SX82A BY HA

PARTS LIST OF CONVERSION BOARD

LOCATION	CBPC562KHGY2 AI562KHGM1				SPECIFICATION CBPC562KHGH1 AUTO INS
CN804	33A	3802	4H		WAFER 4P RIGHT ANGLE PITCH
CN102	33A	3802	6H		WAFER 6P RIGHT ANGLE PITCH 2.0
CN101	33A	3802	9H		WAFER 9P RIGHT ANGLE PITCH 2.0
CN805	33A	3802	9H		WAFER 9P RIGHT ANGLE PITCH 2.0
JP101	33A	8009	2		2 PIN MIN. JUMOER
JP802	33A	8009	3		3 PIN PLUG
JP101	33A	8010	2	L	2P SHUNT MINI JUMPER
JP802	33A	8010	2	L	2P SHUNT MINI JUMPER
CN801	33A	8013	14	H	PLUG 14P 90
	40A	152	69		LABEL
U102	56A	1125	61	H6	M6759 (IIYAMA SIP)
C901	67A	305	331	6L	330UF 35V
C903	67A	305	331	6L	330UF 35V
C904	67A	305	331	6L	330UF 35V
C906	67A	305	331	6L	330UF 35V
C111	67A	309	471	3L	470UF +-20% 16V
L901	71A	55	28		BEAD P6H 7.62×5.08×6.4 BY TEC
L902	73A	253	124	L	CHOKE COIL
L101	73A	259	4		200UH +/-5%
VR801	75A	335	103		10K OHM ±30% RH06I5CI4J ALPS
U302	79A	L15M	1	CYN	DC/DC MODULE BY CYNTEC
U102	87A	202	44		IC SOCKET 44P PLCC
X101	93A	22	55		CRYSTAL 20MHz HC-49US
U802	93A	22	57		OSCILLATOR 50MHz-3.3V HALF S
CN902	95A	900	22		HARNESS

LOCATION	AI562KHGH1				SPECIFICATION
CN301	33A	3804	40		CONNECTOR
CN302	33A	3804	40		CONNECTOR
CN301	33A	8019	40		CONNECTOR 40P
CN302	33A	8019	40		CONNECTOR 40P
U801	56A	562	8		gmZAN1 PQFP-160 GENESIS
U301	56A	562	11		WFP4620D BY WINBOND
U901	56A	563	1		CHIP LM2596S-5.0 BY NS
U902	56A	563	7		AIC1084-33M TO-263 ANALO
U803	56A	1133	16		GHIP 24LC21A/SN BY MICRO
U101	56A	1133	17		AT24CO4N-10SC BY ATMEL
Q801	57A	417	4		CHIP PMBS3904 BY PHILIPS
Q803	57A	417	4		CHIP PMBS3904 BY PHILIPS
Q804	57A	417	4		CHIP PMBS3904 BY PHILIPS
Q805	57A	417	4		CHIP PMBS3904 BY PHILIPS
Q802	57A	748	1		SI2304DS BY SILICONIX SOT-23
D809	57A	754	1		BAT54C-GS08 SOT-23 TELEF
RP101	61A	125	000	8	CHIP ARRAY 0 OHM 1/16W 8P4R
RP102	61A	125	000	8	CHIP ARRAY 0 OHM 1/16W 8P4R
RP801	61A	125	103	8	CHIP ARRAY 10K OHM 1/16W 8P4R
RP802	61A	125	103	8	CHIP ARRAY 10K OHM 1/16W 8P4R
RP803	61A	125	103	8	CHIP ARRAY 10K OHM 1/16W 8P4R
JP102	61A	0603	000		CHIP 0 OHM 1/16W
JP801	61A	0603	000		CHIP 0 OHM 1/16W
JP811	61A	0603	000		CHIP 0 OHM 1/16W
L301	61A	0603	000		CHIP 0 OHM 1/16W
L302	61A	0603	000		CHIP 0 OHM 1/16W
L303	61A	0603	000		CHIP 0 OHM 1/16W
L304	61A	0603	000		CHIP 0 OHM 1/16W
L305	61A	0603	000		CHIP 0 OHM 1/16W
L306	61A	0603	000		CHIP 0 OHM 1/16W
L307	61A	0603	000		CHIP 0 OHM 1/16W
L308	61A	0603	000		CHIP 0 OHM 1/16W
L309	61A	0603	000		CHIP 0 OHM 1/16W
L805	61A	0603	000		CHIP 0 OHM 1/16W
L806	61A	0603	000		CHIP 0 OHM 1/16W
L807	61A	0603	000		CHIP 0 OHM 1/16W
L808	61A	0603	000		CHIP 0 OHM 1/16W
L810	61A	0603	000		CHIP 0 OHM 1/16W
R112	61A	0603	000		CHIP 0 OHM 1/16W
R322	61A	0603	000		CHIP 0 OHM 1/16W
R324	61A	0603	000		CHIP 0 OHM 1/16W
R326	61A	0603	000		CHIP 0 OHM 1/16W
R328	61A	0603	000		CHIP 0 OHM 1/16W
R330	61A	0603	000		CHIP 0 OHM 1/16W
R344	61A	0603	000		CHIP 0 OHM 1/16W
R346	61A	0603	000		CHIP 0 OHM 1/16W
R352	61A	0603	000		CHIP 0 OHM 1/16W
R353	61A	0603	000		CHIP 0 OHM 1/16W
R354	61A	0603	000		CHIP 0 OHM 1/16W
R355	61A	0603	000		CHIP 0 OHM 1/16W
R357	61A	0603	000		CHIP 0 OHM 1/16W
R801	61A	0603	000		CHIP 0 OHM 1/16W
R802	61A	0603	000		CHIP 0 OHM 1/16W
R804	61A	0603	000		CHIP 0 OHM 1/16W
R805	61A	0603	000		CHIP 0 OHM 1/16W
R807	61A	0603	000		CHIP 0 OHM 1/16W
R808	61A	0603	000		CHIP 0 OHM 1/16W
R832	61A	0603	000		CHIP 0 OHM 1/16W
R901	61A	0603	000		CHIP 0 OHM 1/16W
R905	61A	0603	000		CHIP 0 OHM 1/16W
R302	61A	0603	101		CHIP 100 OHM 1/16W
R812	61A	0603	101		CHIP 100 OHM 1/16W
R813	61A	0603	101		CHIP 100 OHM 1/16W
R819	61A	0603	101		CHIP 100 OHM 1/16W
R820	61A	0603	101		CHIP 100 OHM 1/16W

LOCATION	AI562KHGH1				SPECIFICATION
R821	61A	0603	101		CHIP 100 OHM 1/16W
R826	61A	0603	101		CHIP 100 OHM 1/16W
R104	61A	0603	102		CHIP 1K OHM 1/16W
R117	61A	0603	102		CHIP 1K OHM 1/16W
R119	61A	0603	102		CHIP 1K OHM 1/16W
R306	61A	0603	102		CHIP 1K OHM 1/16W
R814	61A	0603	102		CHIP 1K OHM 1/16W
R815	61A	0603	102		CHIP 1K OHM 1/16W
R105	61A	0603	103		CHIP 10K OHM 1/16W
R106	61A	0603	103		CHIP 10K OHM 1/16W
R107	61A	0603	103		CHIP 10K OHM 1/16W
R108	61A	0603	103		CHIP 10K OHM 1/16W
R109	61A	0603	103		CHIP 10K OHM 1/16W
R113	61A	0603	103		CHIP 10K OHM 1/16W
R301	61A	0603	103		CHIP 10K OHM 1/16W
R303	61A	0603	103		CHIP 10K OHM 1/16W
R304	61A	0603	103		CHIP 10K OHM 1/16W
R305	61A	0603	103		CHIP 10K OHM 1/16W
R311	61A	0603	103		CHIP 10K OHM 1/16W
R331	61A	0603	103		CHIP 10K OHM 1/16W
R333	61A	0603	103		CHIP 10K OHM 1/16W
R335	61A	0603	103		CHIP 10K OHM 1/16W
R337	61A	0603	103		CHIP 10K OHM 1/16W
R339	61A	0603	103		CHIP 10K OHM 1/16W
R341	61A	0603	103		CHIP 10K OHM 1/16W
R351	61A	0603	103		CHIP 10K OHM 1/16W
R817	61A	0603	103		CHIP 10K OHM 1/16W
R818	61A	0603	103		CHIP 10K OHM 1/16W
R822	61A	0603	103		CHIP 10K OHM 1/16W
R828	61A	0603	103		CHIP 10K OHM 1/16W
R829	61A	0603	103		CHIP 10K OHM 1/16W
R830	61A	0603	103		CHIP 10K OHM 1/16W
R831	61A	0603	103		CHIP 10K OHM 1/16W
R834	61A	0603	103		CHIP 10K OHM 1/16W
R835	61A	0603	103		CHIP 10K OHM 1/16W
R837	61A	0603	103		CHIP 10K OHM 1/16W
R838	61A	0603	103		CHIP 10K OHM 1/16W
R823	61A	0603	104		CHIP 100K OHM 1/16W
R824	61A	0603	104		CHIP 100K OHM 1/16W
R810	61A	0603	202		CHIP 2K OHM 1/16W
R811	61A	0603	202		CHIP 2K OHM 1/16W
R825	61A	0603	302		CHIP 3K OHM 5% 1/16W
R103	61A	0603	472		CHIP 4.7K OHM 1/16W
R116	61A	0603	472		CHIP 4.7K OHM 1/16W
R118	61A	0603	472		CHIP 4.7K OHM 1/16W
R827	61A	0603	511		CHIP 510 OHM 1/16W
R307	61A	0603	560		CHIP 56 OHM 1/16W
R308	61A	0603	560		CHIP 56 OHM 1/16W
R309	61A	0603	560		CHIP 56 OHM 1/16W
R310	61A	0603	560		CHIP 56 OHM 1/16W
R312	61A	0603	560		CHIP 56 OHM 1/16W
R313	61A	0603	560		CHIP 56 OHM 1/16W
R314	61A	0603	560		CHIP 56 OHM 1/16W
R315	61A	0603	560		CHIP 56 OHM 1/16W
R316	61A	0603	560		CHIP 56 OHM 1/16W
R317	61A	0603	560		CHIP 56 OHM 1/16W
R318	61A	0603	560		CHIP 56 OHM 1/16W
R319	61A	0603	560		CHIP 56 OHM 1/16W
R320	61A	0603	560		CHIP 56 OHM 1/16W
R803	61A	0603	750		CHIP 75 OHM 1/16W
R806	61A	0603	750		CHIP 75 OHM 1/16W
R809	61A	0603	750		CHIP 75 OHM 1/16W
L804	61A	1206	000		CHIP 0 OHM 1/8W
C315	65A	0603	100	31	CHIP 10PF 50V NPO
C316	65A	0603	100	31	CHIP 10PF 50V NPO

LOCATION	AI562KHGH1				SPECIFICATION
C317	65A	0603	100	31	CHIP 10PF 50V NPO
C318	65A	0603	100	31	CHIP 10PF 50V NPO
C325	65A	0603	100	31	CHIP 10PF 50V NPO
C326	65A	0603	100	31	CHIP 10PF 50V NPO
C327	65A	0603	100	31	CHIP 10PF 50V NPO
C331	65A	0603	100	31	CHIP 10PF 50V NPO
C332	65A	0603	100	31	CHIP 10PF 50V NPO
C309	65A	0603	101	32	CHIP 100PF 50V X7R
C328	65A	0603	101	32	CHIP 100PF 50V X7R
C329	65A	0603	101	32	CHIP 100PF 50V X7R
C330	65A	0603	101	32	CHIP 100PF 50V X7R
C333	65A	0603	101	32	CHIP 100PF 50V X7R
C334	65A	0603	101	32	CHIP 100PF 50V X7R
C836	65A	0603	101	32	CHIP 100PF 50V X7R
C837	65A	0603	101	32	CHIP 100PF 50V X7R
C302	65A	0603	102	32	CHIP 1000PF 50V X7R
C304	65A	0603	102	32	CHIP 1000PF 50V X7R
C306	65A	0603	102	32	CHIP 1000PF 50V X7R
C308	65A	0603	102	32	CHIP 1000PF 50V X7R
C311	65A	0603	102	32	CHIP 1000PF 50V X7R
C313	65A	0603	102	32	CHIP 1000PF 50V X7R
C320	65A	0603	102	32	CHIP 1000PF 50V X7R
C322	65A	0603	102	32	CHIP 1000PF 50V X7R
C324	65A	0603	102	32	CHIP 1000PF 50V X7R
C351	65A	0603	102	32	CHIP 1000PF 50V X7R
C353	65A	0603	102	32	CHIP 1000PF 50V X7R
C355	65A	0603	102	32	CHIP 1000PF 50V X7R
C357	65A	0603	102	32	CHIP 1000PF 50V X7R
C358	65A	0603	102	32	CHIP 1000PF 50V X7R
C846	65A	0603	102	32	CHIP 1000PF 50V X7R
C851	65A	0603	102	32	CHIP 1000PF 50V X7R
C852	65A	0603	102	32	CHIP 1000PF 50V X7R
C907	65A	0603	102	32	CHIP 1000PF 50V X7R
C830	65A	0603	103	32	CHIP 0.01UF 50V X7R
C831	65A	0603	103	32	CHIP 0.01UF 50V X7R
C832	65A	0603	103	32	CHIP 0.01UF 50V X7R
C833	65A	0603	103	32	CHIP 0.01UF 50V X7R
C834	65A	0603	103	32	CHIP 0.01UF 50V X7R
C835	65A	0603	103	32	CHIP 0.01UF 50V X7R
C106	65A	0603	104	12	CHIP 0.1UF 16V X7R
C108	65A	0603	104	12	CHIP 0.1UF 16V X7R
C301	65A	0603	104	12	CHIP 0.1UF 16V X7R
C303	65A	0603	104	12	CHIP 0.1UF 16V X7R
C305	65A	0603	104	12	CHIP 0.1UF 16V X7R
C307	65A	0603	104	12	CHIP 0.1UF 16V X7R
C310	65A	0603	104	12	CHIP 0.1UF 16V X7R
C312	65A	0603	104	12	CHIP 0.1UF 16V X7R
C314	65A	0603	104	12	CHIP 0.1UF 16V X7R
C319	65A	0603	104	12	CHIP 0.1UF 16V X7R
C321	65A	0603	104	12	CHIP 0.1UF 16V X7R
C323	65A	0603	104	12	CHIP 0.1UF 16V X7R
C337	65A	0603	104	12	CHIP 0.1UF 16V X7R
C340	65A	0603	104	12	CHIP 0.1UF 16V X7R
C342	65A	0603	104	12	CHIP 0.1UF 16V X7R
C344	65A	0603	104	12	CHIP 0.1UF 16V X7R
C346	65A	0603	104	12	CHIP 0.1UF 16V X7R
C348	65A	0603	104	12	CHIP 0.1UF 16V X7R
C349	65A	0603	104	12	CHIP 0.1UF 16V X7R
C350	65A	0603	104	12	CHIP 0.1UF 16V X7R
C352	65A	0603	104	12	CHIP 0.1UF 16V X7R
C354	65A	0603	104	12	CHIP 0.1UF 16V X7R
C356	65A	0603	104	12	CHIP 0.1UF 16V X7R
C802	65A	0603	104	12	CHIP 0.1UF 16V X7R
C803	65A	0603	104	12	CHIP 0.1UF 16V X7R
C805	65A	0603	104	12	CHIP 0.1UF 16V X7R

LOCATION	AI562KHGH1				SPECIFICATION
C806	65A	0603	104	12	CHIP 0.1UF 16V X7R
C808	65A	0603	104	12	CHIP 0.1UF 16V X7R
C809	65A	0603	104	12	CHIP 0.1UF 16V X7R
C810	65A	0603	104	12	CHIP 0.1UF 16V X7R
C811	65A	0603	104	12	CHIP 0.1UF 16V X7R
C812	65A	0603	104	12	CHIP 0.1UF 16V X7R
C813	65A	0603	104	12	CHIP 0.1UF 16V X7R
C814	65A	0603	104	12	CHIP 0.1UF 16V X7R
C816	65A	0603	104	12	CHIP 0.1UF 16V X7R
C818	65A	0603	104	12	CHIP 0.1UF 16V X7R
C819	65A	0603	104	12	CHIP 0.1UF 16V X7R
C820	65A	0603	104	12	CHIP 0.1UF 16V X7R
C821	65A	0603	104	12	CHIP 0.1UF 16V X7R
C822	65A	0603	104	12	CHIP 0.1UF 16V X7R
C823	65A	0603	104	12	CHIP 0.1UF 16V X7R
C824	65A	0603	104	12	CHIP 0.1UF 16V X7R
C826	65A	0603	104	12	CHIP 0.1UF 16V X7R
C827	65A	0603	104	12	CHIP 0.1UF 16V X7R
C828	65A	0603	104	12	CHIP 0.1UF 16V X7R
C829	65A	0603	104	12	CHIP 0.1UF 16V X7R
C838	65A	0603	104	12	CHIP 0.1UF 16V X7R
C839	65A	0603	104	12	CHIP 0.1UF 16V X7R
C840	65A	0603	104	12	CHIP 0.1UF 16V X7R
C841	65A	0603	104	12	CHIP 0.1UF 16V X7R
C847	65A	0603	104	12	CHIP 0.1UF 16V X7R
C850	65A	0603	104	12	CHIP 0.1UF 16V X7R
C902	65A	0603	104	12	CHIP 0.1UF 16V X7R
C905	65A	0603	104	12	CHIP 0.1UF 16V X7R
C104	65A	0603	330	31	CHIP 33PF 50V NPO
C105	65A	0603	330	31	CHIP 33PF 50V NPO
C845	65A	0603	330	31	CHIP 33PF 50V NPO
C848	65A	0603	390	31	CHIP 39PF 50V NPO
CP101	65A	600M	102	8T	CHIP ARRAY 1000PF 8P
CP102	65A	600M	471	8T	CHIP ARRAY 470PF 8P
CP301	65A	602K	100	8T	CHIP ARRAY 10PF 8P
CP302	65A	602K	100	8T	CHIP ARRAY 10PF 8P
CP303	65A	602K	100	8T	CHIP ARRAY 10PF 8P
CP304	65A	602K	100	8T	CHIP ARRAY 10PF 8P
CP305	65A	602K	100	8T	CHIP ARRAY 10PF 8P
CP306	65A	602K	100	8T	CHIP ARRAY 10PF 8P
CP307	65A	602K	100	8T	CHIP ARRAY 10PF 8P
CP308	65A	602K	100	8T	CHIP ARRAY 10PF 8P
CP309	65A	602K	100	8T	CHIP ARRAY 10PF 8P
C103	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C107	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C336	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C339	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C341	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C343	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C345	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C347	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C801	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C804	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C807	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C815	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C817	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C825	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C849	67A	312	220	3	SMD EC 22UF 16V 85C C SIZE
C102	67A	312	229	7	SMD EC 2.2UF 50V 85C
C109	67A	312	229	7	SMD EC 2.2UF 50V 85C
C110	67A	312	229	7	SMD EC 2.2UF 50V 85C
LP801	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP802	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP803	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP804	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM

LOCATION	AI562KHGH1				SPECIFICATION
LP805	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP806	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP807	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP808	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP809	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP810	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP811	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP812	71A	56A	121	8T	CHIP BEAD ARRAY 120 OHM
LP301	71A	56A	301	8B	CHIP BEAD ARRAY 300 OHM FCA321
LP302	71A	56A	301	8B	CHIP BEAD ARRAY 300 OHM FCA321
LP303	71A	56A	301	8B	CHIP BEAD ARRAY 300 OHM FCA321
LP304	71A	56A	301	8B	CHIP BEAD ARRAY 300 OHM FCA321
LP305	71A	56A	301	8B	CHIP BEAD ARRAY 300 OHM FCA321
LP306	71A	56A	301	8B	CHIP BEAD ARRAY 300 OHM FCA321
LP307	71A	56A	301	8B	CHIP BEAD ARRAY 300 OHM FCA321
LP308	71A	56A	301	8B	CHIP BEAD ARRAY 300 OHM FCA321
LP309	71A	56A	301	8B	CHIP BEAD ARRAY 300 OHM FCA321
L801	71A	57G	601		CHIP BEAD 600 OHM 1206
L802	71A	57G	601		CHIP BEAD 600 OHM 1206
L803	71A	57G	601		CHIP BEAD 600 OHM 1206
L310	71A	59B	121		CHIP BEAD 120 OHM 0603
L809	71A	59B	121		CHIP BEAD 120 OHM 0603
R347	71A	59B	121		CHIP BEAD 120 OHM 0603
R349	71A	59B	121		CHIP BEAD 120 OHM 0603
R816	71A	59B	121		CHIP BEAD 120 OHM 0603
D804	93A	39	146		LL5232B BY FCI
D805	93A	39	146		LL5232B BY FCI
D806	93A	39	146		LL5232B BY FCI
D807	93A	39	146		LL5232B BY FCI
D808	93A	39	146		LL5232B BY FCI
D901	93A	60	211		SMB340 BY FULL POWER
D101	93A	64	32		LL4148 SMD BY FCI
D102	93A	64	32		LL4148 SMD BY FCI
D810	93A	64	32		LL4148 SMD BY FCI
D801	93A	64	33P		BAV99 SOT-23 BY PAN JIT
D802	93A	64	33P		BAV99 SOT-23 BY PAN JIT
D803	93A	64	33P		BAV99 SOT-23 BY PAN JIT
	715A	860	1	A	TF1560SP LCD MAIN BOARD

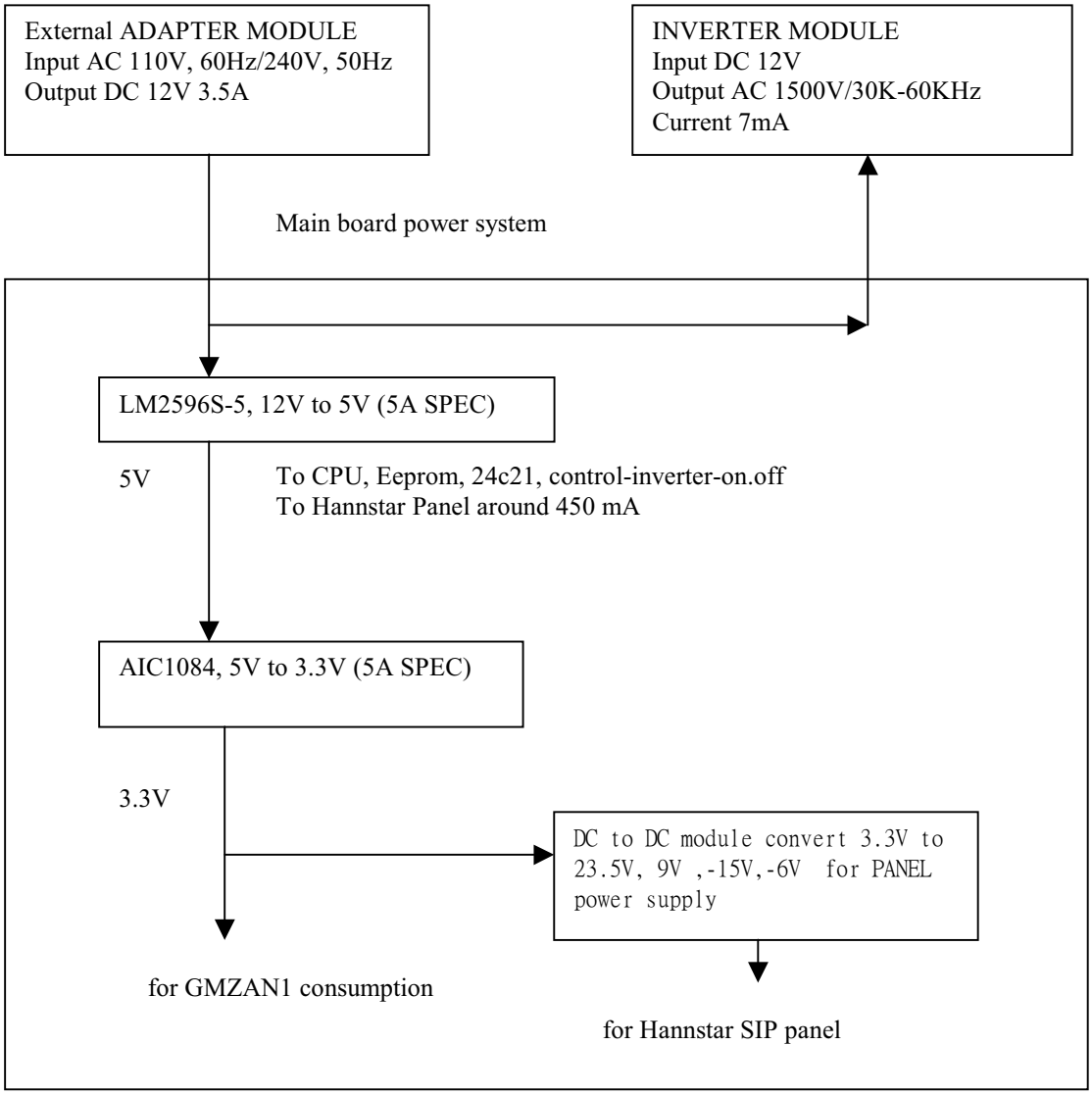
PARTS LIST OF CONVERSION BOARD

LOCATION	CNPC562A2				SPECIFICATION
J7	33A	3252	2	H	WAFER 2P 3.96mm
JP2	88A	304	1S		DC POWER JACK SCD-014A
	715A	891	1		LCD L501-A DC-IN BRD

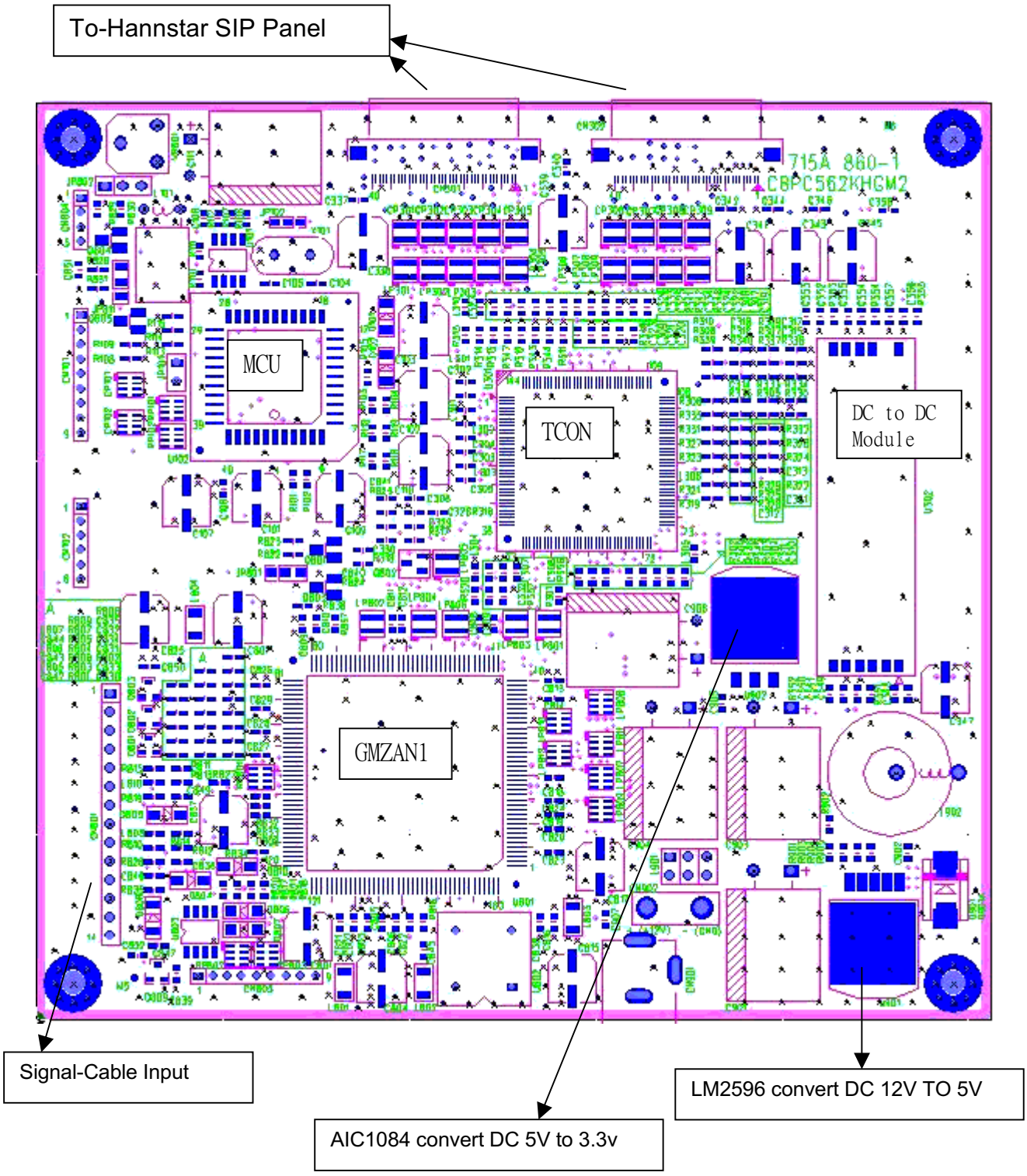
PARTS LIST OF KEY PC BOARD

LOCATION	KEPC560KY2				SPECIFICATION
Q101	57A	417	4		CHIP PMBS3904 BY PHILIPS
Q102	57A	417	4		CHIP PMBS3904 BY PHILIPS
R109	61A	602	102	52T	1K OHM 5% 1/6W
R101	61A	602	103	52T	10K OHM 5% 1/6W
R102	61A	602	103	52T	10K OHM 5% 1/6W
R103	61A	602	103	52T	10K OHM 5% 1/6W
R104	61A	602	103	52T	10K OHM 5% 1/6W
R105	61A	602	103	52T	10K OHM 5% 1/6W
R106	61A	602	103	52T	10K OHM 5% 1/6W
R107	61A	602	103	52T	10K OHM 5% 1/6W
R108	61A	602	221	52T	220 OHM ±5% 1/6W
C101	65A	0603	104	12	CHIP 0.1UF 16V
SW101	77A	600	1	G	TACT SWITCH
SW102	77A	600	1	G	TACT SWITCH
SW103	77A	600	1	G	TACT SWITCH
SW104	77A	600	1	G	TACT SWITCH
SW105	77A	600	1	G	TACT SWITCH
LED1	81A	12	1	BH	LED 3mm BL-BYG201-RR-OP-2.4%
J101	95A	90	23		TIN COATED
J102	95A	90	23		TIN COATED
J801	95A	8014	9	10	HARNESS
	715A	879	1A		LCD 15” IIYAMA KEY

9. POWER SYSTEM AND CONSUMPTION CURRENT

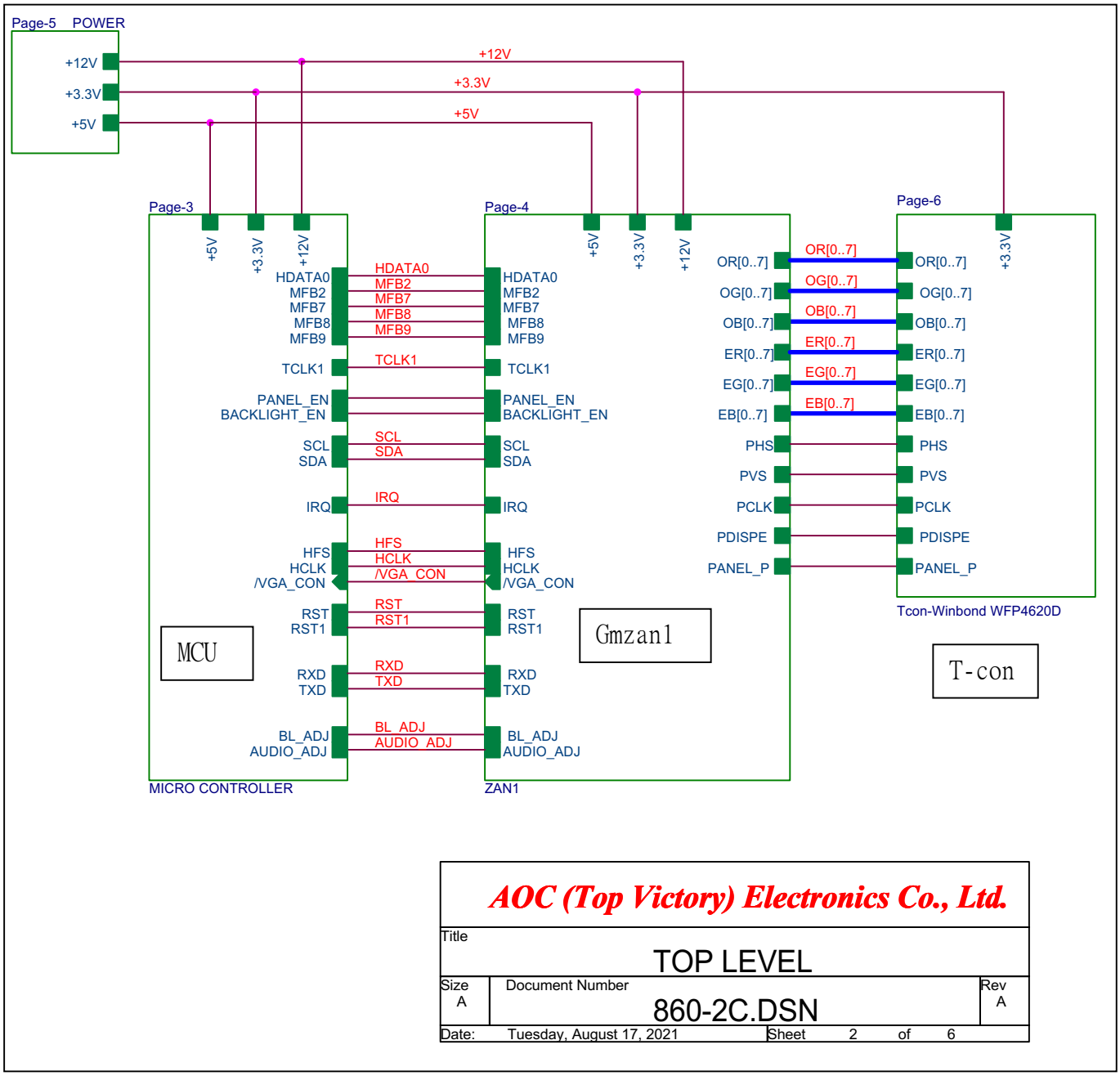


10. PCB LAYOUT

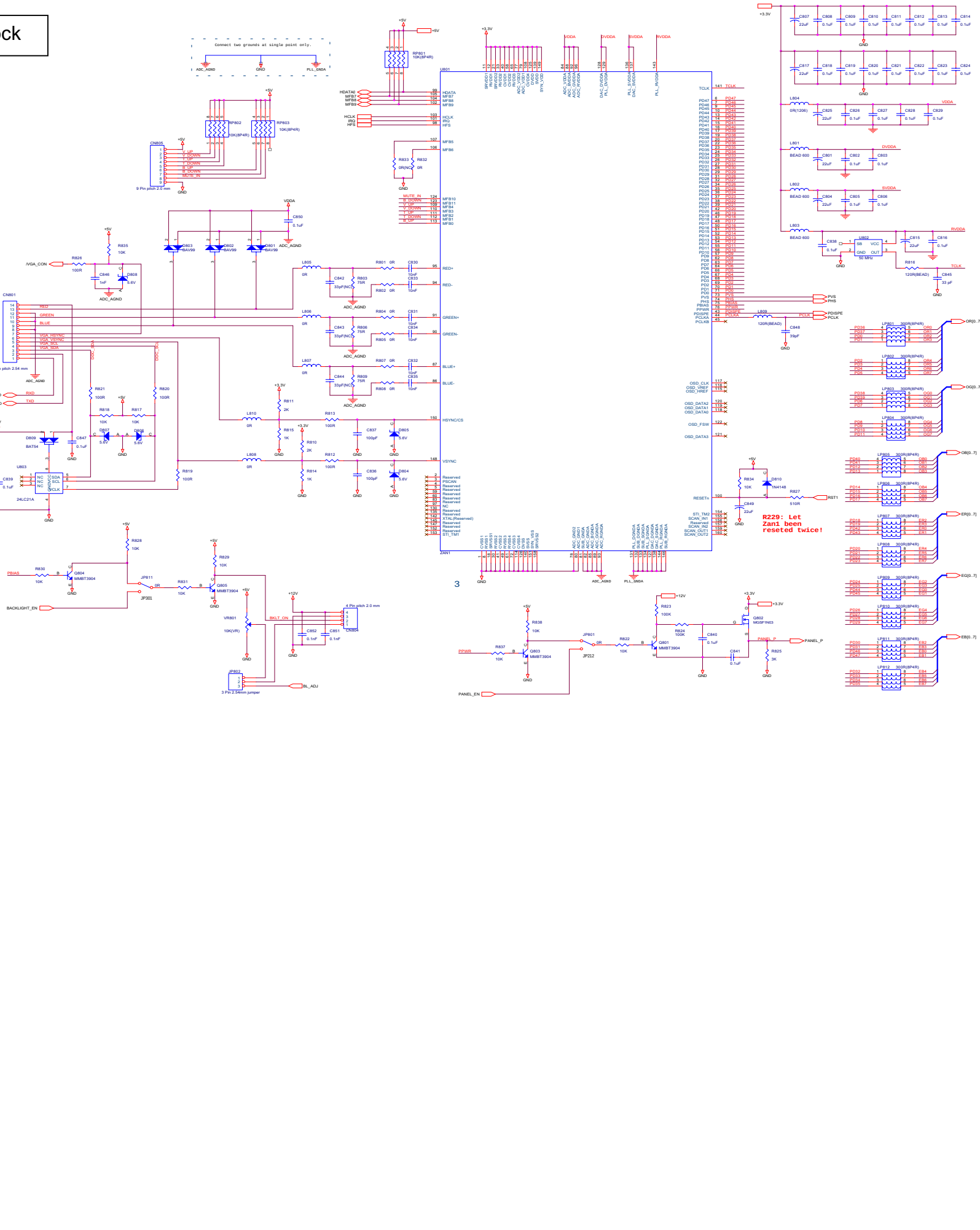


11. SCHEMATIC DIAGRAM

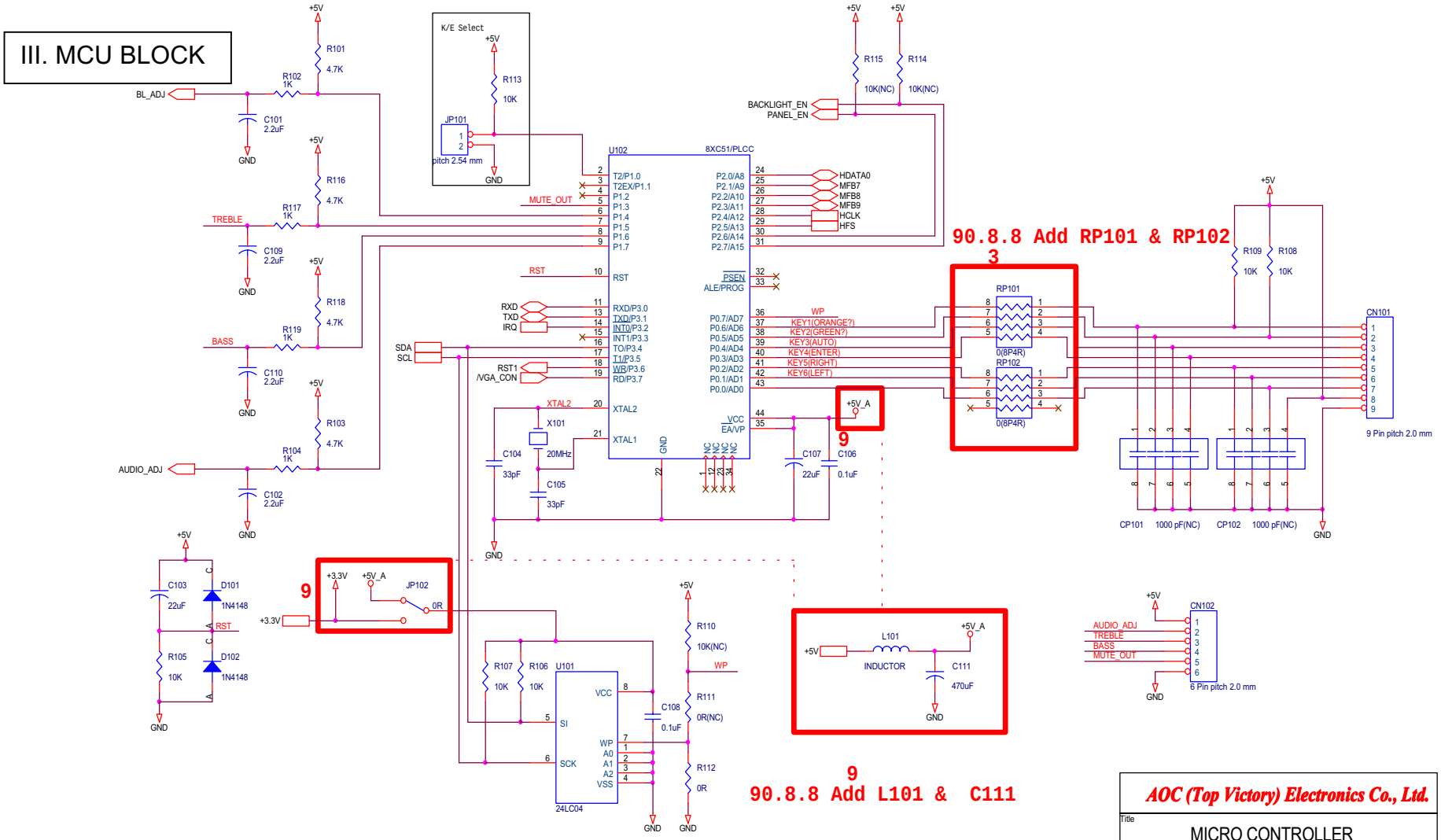
I). TOP-LEVEL FLOW



II. GMZAN1 Block



III. MCU BLOCK



AOC (Top Victory) Electronics Co., Ltd.	
Title	MICRO CONTROLLER
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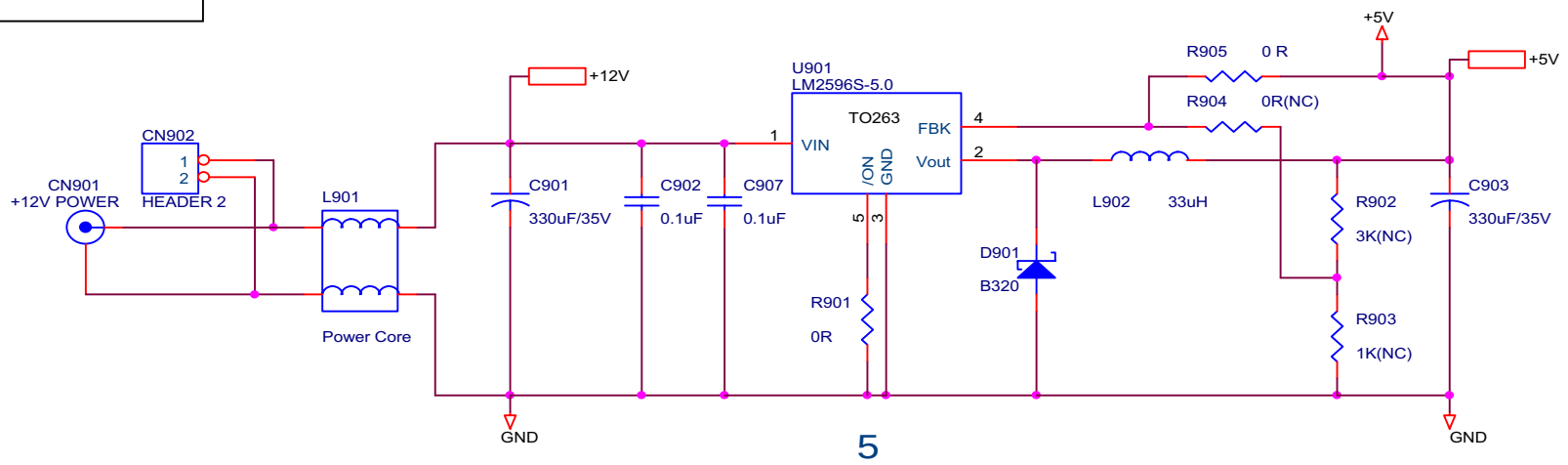
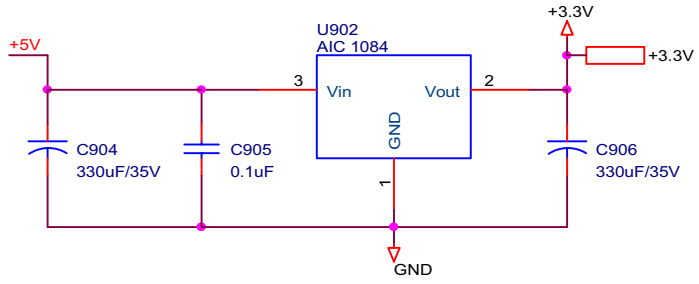
IV. POWER BLOCK

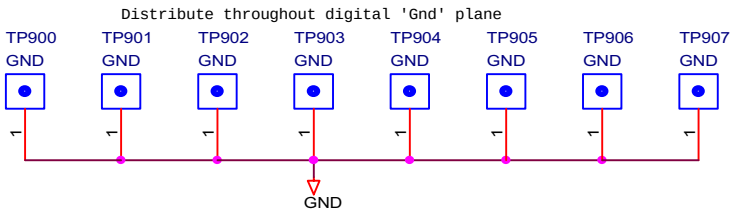


5



*10

	R901	R902	R903	R904	R905
LM2596	SHORT	OPEN	OPEN	OPEN	SHORT
CY1032	OPEN	3K	1K	SHORT	OPEN



AOC (Top Victory) Electronics Co., Ltd.

Title: POWER		
Size: A	Document Number: 860-2C.DSN	Rev: A
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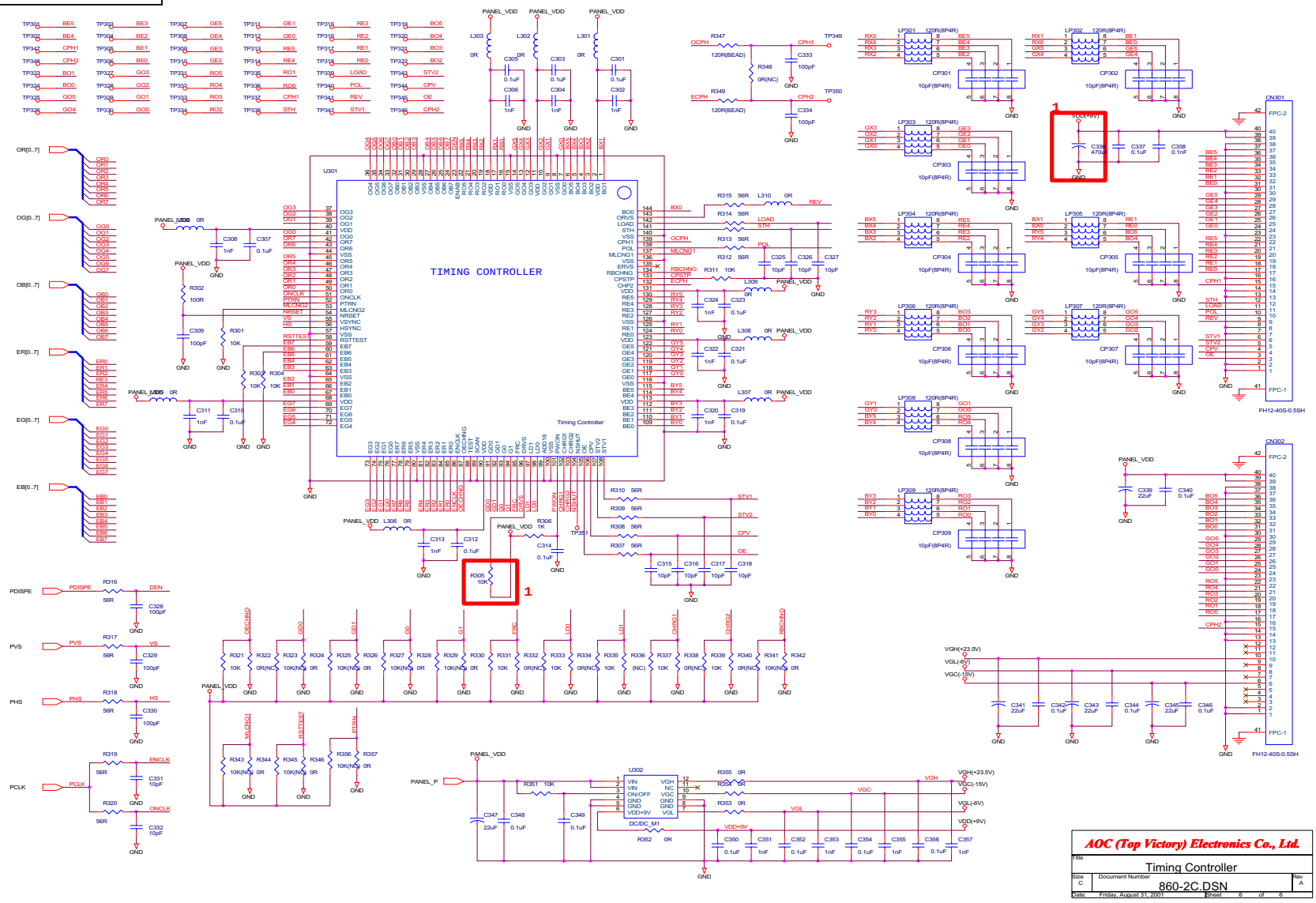
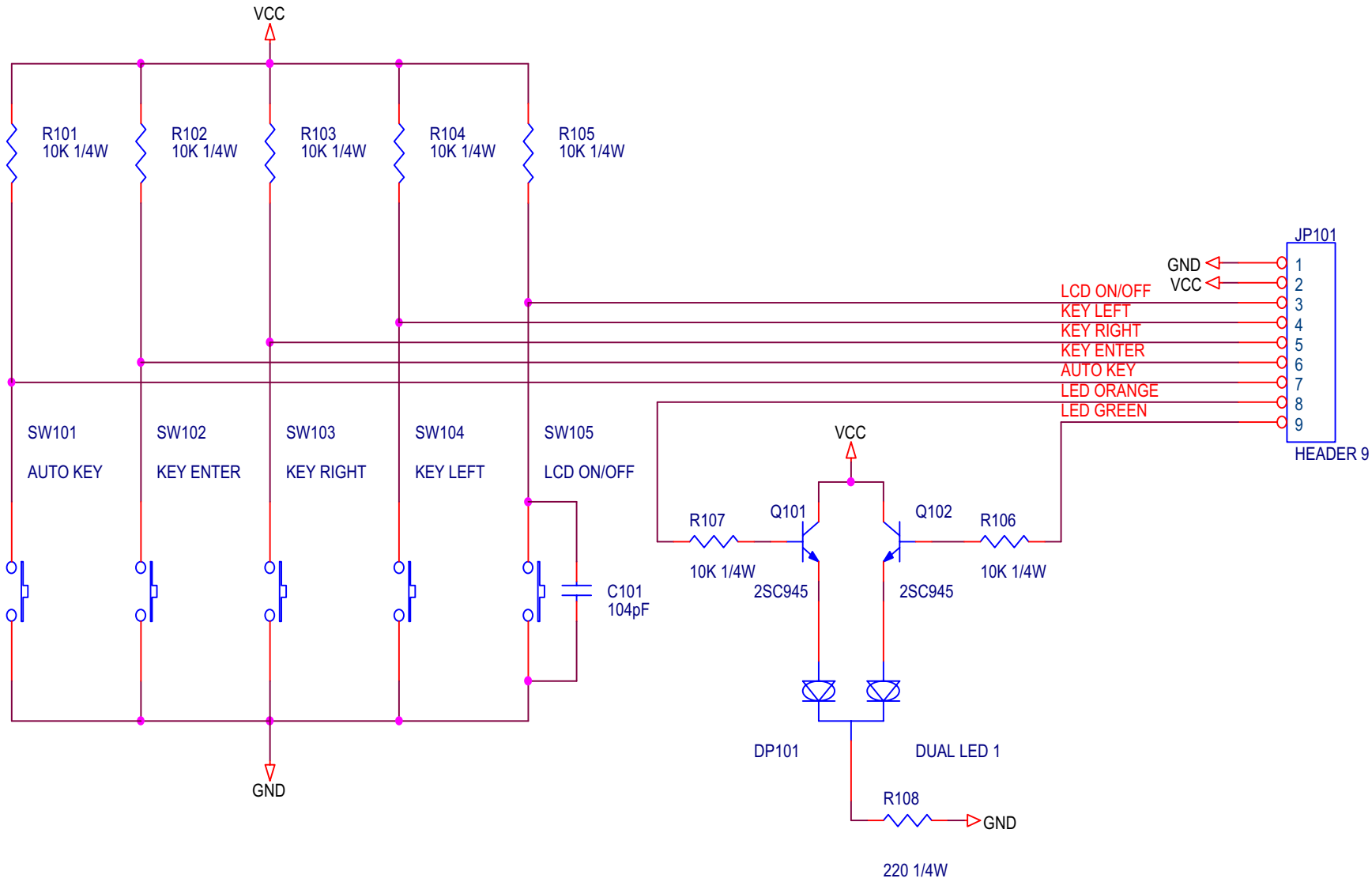
V. Timing –Controller (TCON)




VCC
R101
10K 1/4W
R102
10K 1/4W
R103
10K 1/4W
R104
10K 1/4W
R105
10K 1/4W
JP101
GND
VCC
LCD ON/OFF
KEY LEFT
KEY RIGHT
KEY ENTER
AUTO KEY
LED ORANGE
LED GREEN
1
2
3
4
5
6
7
8
9
HEADER 9
SW101
AUTO KEY
SW102
KEY ENTER
SW103
KEY RIGHT
SW104
KEY LEFT
SW105
LCD ON/OFF
C101
104pF
VCC
R107
10K 1/4W
Q101
2SC945
Q102
2SC945
R106
10K 1/4W
DP101
DUAL LED 1
R108
220 1/4W
GND
GND