ImageQuest

LM-1510A(LM-1510B)

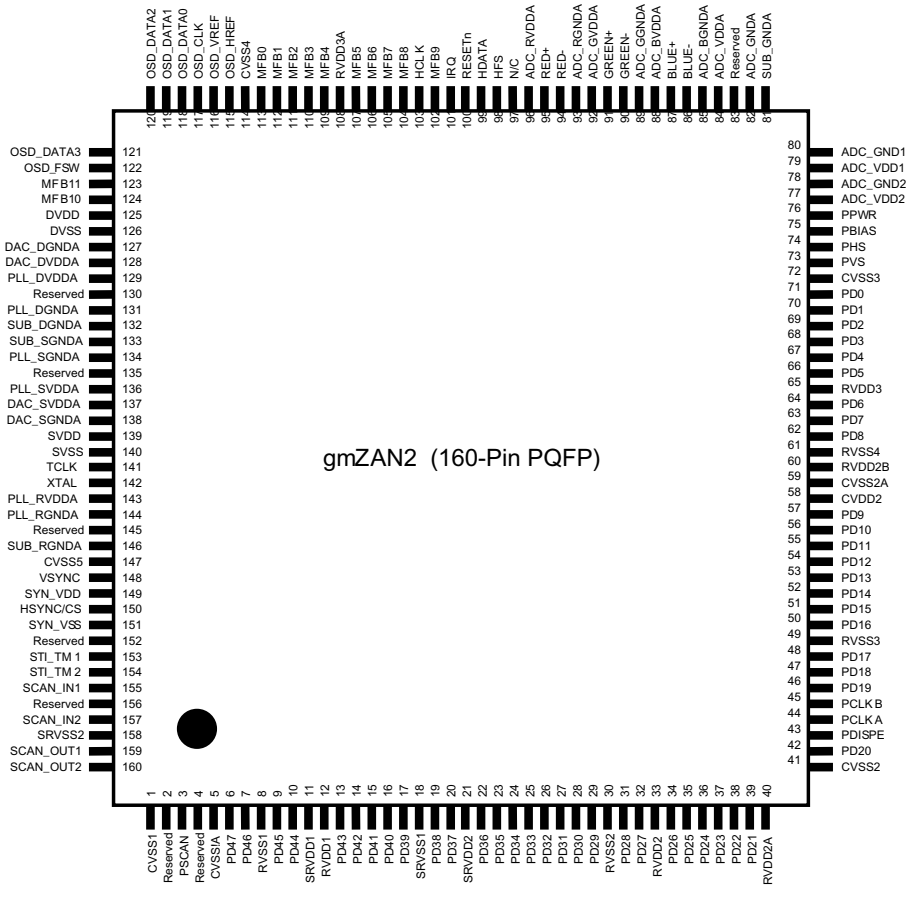
Multiscanning Color Monitor

TECHNICAL SERVICE MANUAL

HYUNDAI

Pin Out Diagram

Figure 1. gmZAN2 Pin Diagram



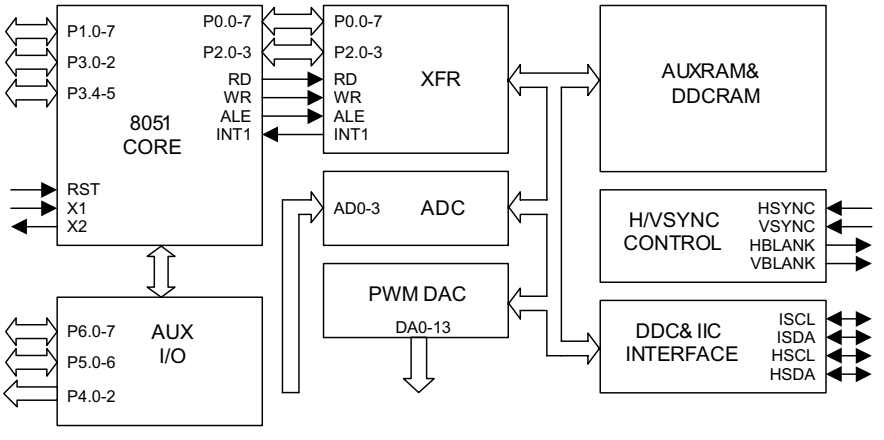
MTV312M64

- 8051 core, 12MHz operating frequency with double CPU clock option
- 0.35uM process; 5V/3.3V power supply and I/O; 3.3V core operating
- 1024-byte RAM; 64K-byte program Flash-ROM support In System Programming (ISP)
- Maximum 14 channels of PWM DAC
- Maximum 31 I/O pins
- SYNC processor for composite separation/insertion, H/V polarity/frequency check and polarity adjustment
- Built-in low power reset circuit
- Built-in self-test pattern generator with four free-running timings
- Compliant with VESA DDC1/2B/2Bi/2B+ standard
- Dual slave IIC addresses; H/W auto transfer DDC1/DDC2x data
- Single master IIC interface for internal device communication
- Maximum 4-channel 6-bit ADC
- Watchdog timer with programmable interval
- Flash-ROM program code protection selection
- 40-pin DIP, 42-pin SDIP or 44-pin PLCC package

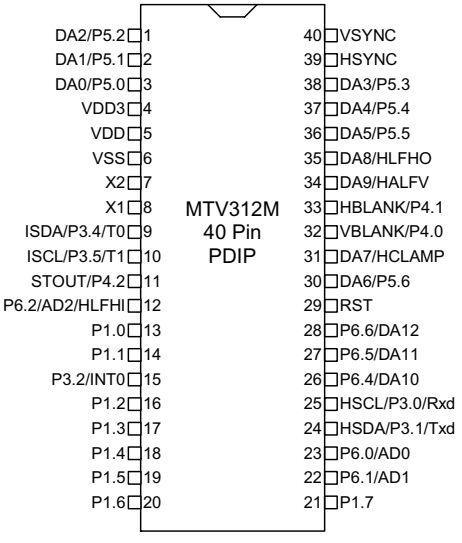
GENERAL DESCRIPTIONS

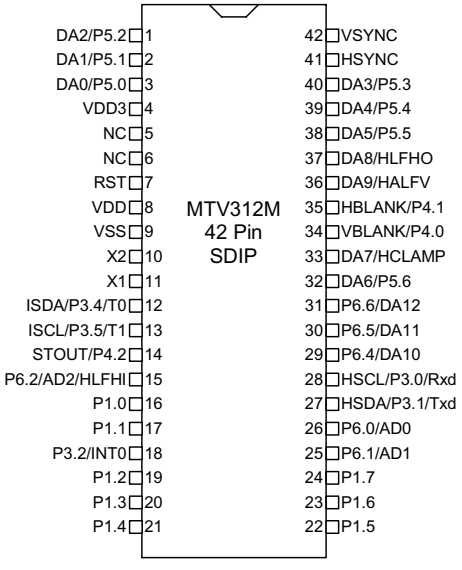
The MTV312M micro-controller is an 8051 CPU core embedded device especially tailored for CRT/LCD Monitor applications. It includes an 8051 CPU core, 1024-byte SRAM, 14 built-in PWM DACs, VESA DDC interface, 4-channel A/D converter, and a 64K-byte internal program Flash-ROM.

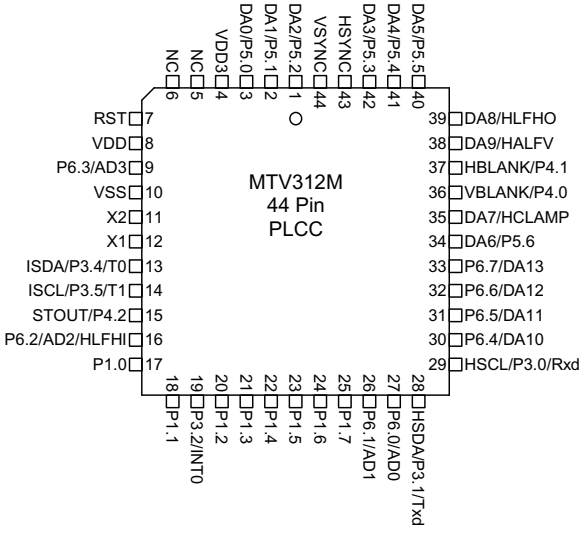
BLOCK DIAGRAM



PIN CONNECTION

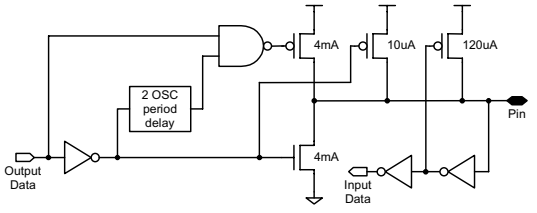




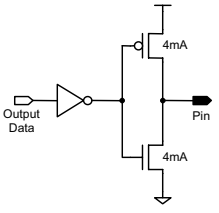


PIN CONFIGURATION

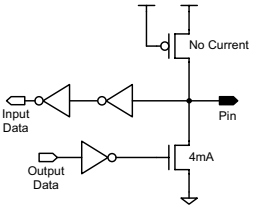
A CMOS output pin means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.
A open drain pin means it can sink at least 4mA current but only drive 10~20uA to VDD. It can be used as input or output function and needs an external pull up resistor.
A 8051 standard pin is a pseudo open drain pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 160nS when output transits from low to high, then keeps driving at 100uA to maintain the pin at high level. It can be used as input or output function. It needs an external pull up resistor when driving heavy load device.



8051 Standard Pin



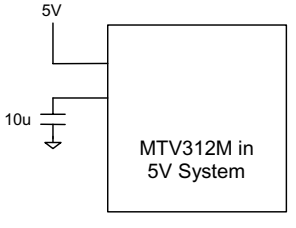
CMOS Output Pin

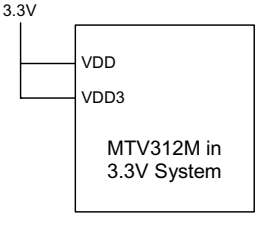


Open Drain Pin

POWER CONFIGURATION

The MTV312M can work on 5V or 3.3V power supply system.
In 5V power system, the VDD pin is connected to 5V power and the VDD3 needs an external capacitor, all output pins can swing from 0~5V, input pins can accept 0~5V input range. And ADC conversion range is 5V. However, X1 and X2 pins must be kept below 3.3V.
In 3.3V power system, the VDD and VDD3 are connected to 3.3V power, all output pins swing from 0~3.3V, HSYNC, VSYNC and open drain pin can accept 0~5V input range, other pins must be kept below 3.3V. And the ADC conversion range is 3.3V.

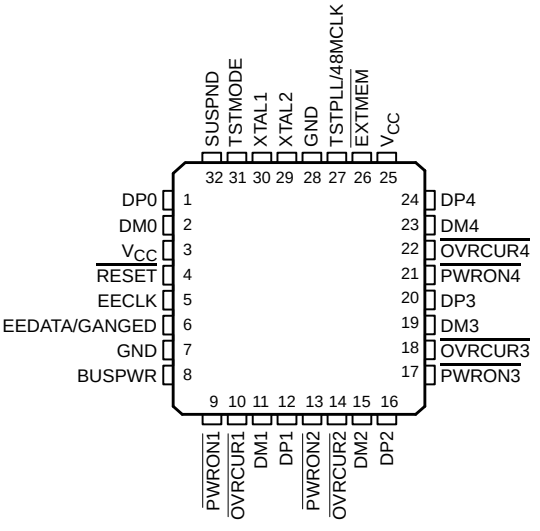




TUSB2046B/B1

- **Universal Serial Bus (USB) Version 1.1 Compliant**
- **32-Pin LQFP≤ Package With a 0.8 mm Pin Pitch**
- **3.3-V Low Power ASIC Logic**
- **Integrated USB Transceivers**
- **State Machine Implementation Requires No Firmware Programming**
- **One Upstream Port and Four Downstream Ports**
- **All Downstream Ports Support Full-Speed and Low-Speed Operations**
- **Two Power Source Modes**
  - **Self-Powered Mode**
  - **Bus-Powered Mode**
- **Power Switching and Over-current Reporting Is Provided Ganged or Per Port**
- **Supports Suspend and Resume Operations**
- **Supports Programmable Vendor ID and Product ID With External Serial EEPROM**
- **3-State EEPROM Interface Allows EEPROM Sharing**
- **Push-Pull Outputs for $\overline{\text{PWRON}}$ Eliminate the Need for External Pullup Resistors**
- **Noise Filtering on $\overline{\text{OVRCUR}}$ Provides Immunity to Voltage Spikes**
- **Package Pinout Allows 2-Layer PCB**
- **Low EMI Emission Achieved by a 6-MHz Crystal Input**
- **Migrated From Proven TUSB2040 Hub**
- **Lower Cost Than the TUSB2040 Hub**
- **Enhanced System ESD Performance**
- **Supports 6 MHz Operation Through a Crystal Input or a 48 MHz Input Clock**

VF PACKAGE
(TOP VIEW)



description

The TUSB2046B is a 3.3-V CMOS hub device that provides one upstream port and four downstream ports in compliance with the 1.1 Universal Serial Bus (USB) specification. Because this device is implemented with a digital state machine instead of a microcontroller, no firmware programming is required. Fully compliant USB transceivers are integrated into the ASIC for all upstream and downstream ports. The downstream ports support both full-speed and low-speed devices by automatically setting the slew rate according to the speed of the device attached to the ports. The configuration of the BUSPWR pin selects either the bus-powered or the self-powered mode.

description (continued)

Configuring the GANGED input determines the power switching and over-current detection modes for the downstream ports. External power management devices such as the TPS2044 are required to control the 5-V source to the downstream ports according to the corresponding values of the $\overline{\text{PWRON}}$ pin. Upon detecting any over-current conditions, the power management device sets the corresponding $\overline{\text{OVRCUR}}$ pin of the TUSB2046B to a logic low. If GANGED is high, all $\overline{\text{PWRON}}$ outputs switch together and if any $\overline{\text{OVRCUR}}$ is activated, all ports transition to power off state. If GANGED is low, the $\overline{\text{PWRON}}$ outputs and $\overline{\text{OVRCUR}}$ inputs operate on a per port basis.

The TUSB2046B provides the flexibility of using a 6-MHz or a 48-MHz clock. The logic level of the TSTMODE terminal controls the selection of the clock source. When TSTMODE is low, the output of the internal APLL circuitry is selected to drive the internal core of the chip. When TSTMODE is high, the TSTPLL/48MCLK input is selected as the input clock source and the APLL circuitry is powered down and bypassed. The internal oscillator cell is also powered down while TSTMODE is high.

Low EMI emission is achieved because the TUSB2046B is able to utilize a 6 MHz crystal input. Connect the crystal as shown in Figure 6. An internal PLL then generates the 48 MHz clock used to sample data from the upstream port and to synchronize the 12 MHz used for the USB clock. If low power suspend and resume are desired, a passive crystal or resonator must be used. However, a 6-MHz oscillator may be used by connecting the output to the XTAL1 terminal and leaving the XTAL2 terminal open. The oscillator TTL output must not exceed 3.6 V.

For 48-MHz operation, the clock can not be generated with a crystal, using the XTAL2 output, since the internal oscillator cell only supports fundamental frequency.

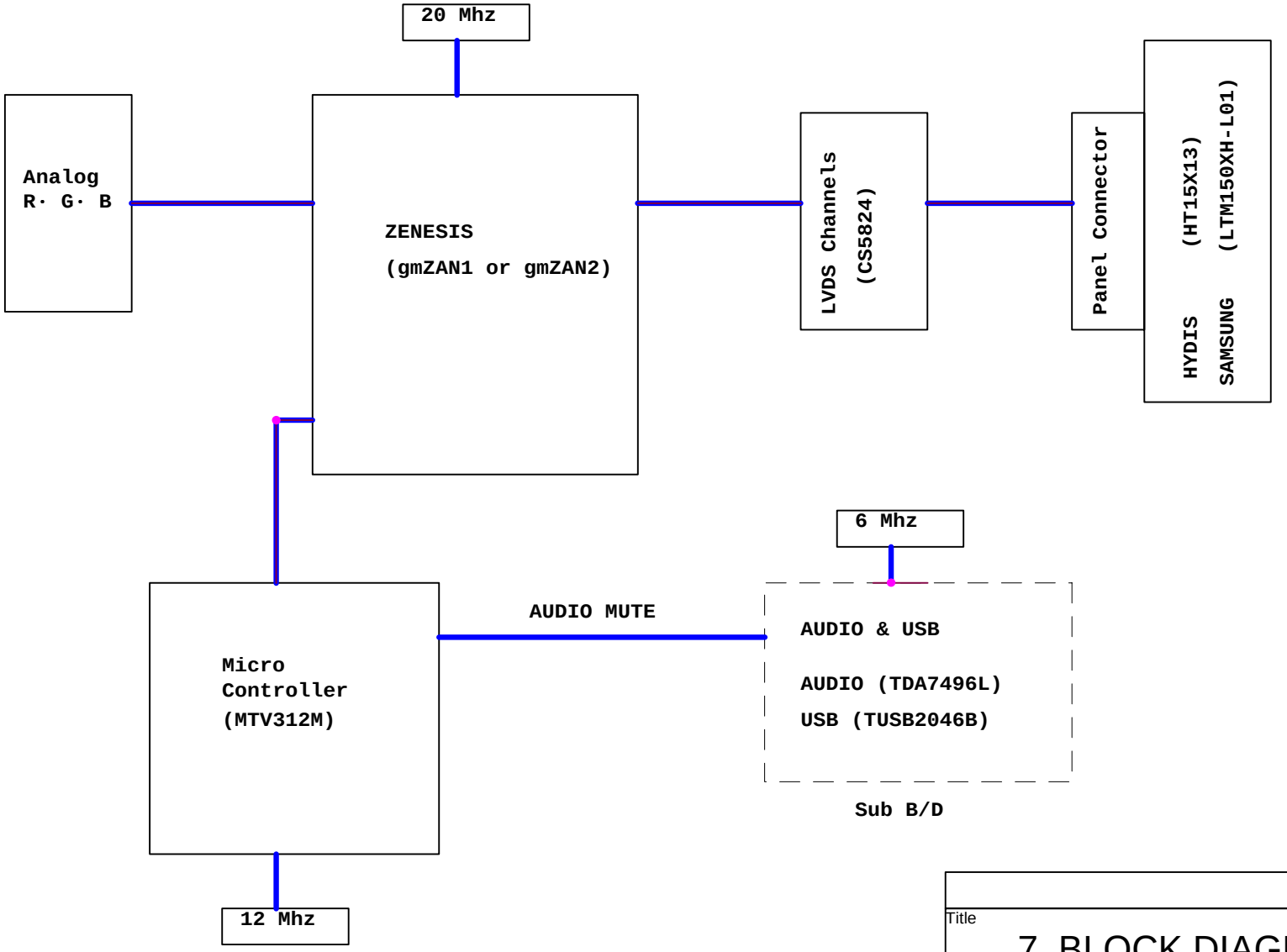
Refer to Figure 7 and Figure 8 in the *input clock configuration* section for more detailed information regarding input clock configuration.

The $\overline{\text{EXTMEM}}$ pin enables or disables the optional EEPROM interface. When the $\overline{\text{EXTMEM}}$ pin is high, the product ID (PID) displayed during enumeration is the general-purpose USB hub. For this default, pin 5 is disabled and pin 6 functions as the GANGED input pin. If custom PID and Vendor ID (VID) descriptors are desired, the $\overline{\text{EXTMEM}}$ pin must be low ($\overline{\text{EXTMEM}}$ = 0). For this configuration, pin 5 and pin 6 function as the EEPROM interface with pin 5 and pin 6 functioning as the EECLK and EEDATA, respectively. See Table 1 for a description of the EEPROM memory map.

Other useful features of the TUSB2046B include a package with a 0.8 mm pin pitch for easy PCB routing and assembly, push-pull outputs for the $\overline{\text{PWRON}}$ pins eliminate the need for pullup resistors required by traditional open collector I/Os, and $\overline{\text{OVRCUR}}$ pins have noise filtering for increased immunity to voltage spikes.

BLOCK DIAGRAM

MODEL NAME : L50C(S527B/L550B/L1510B)



Title	7. BLOCK DIAGRAM	
Size A	Document Number <Doc>	Rev B
Date: Friday, January 04, 2002	Sheet 7 of 7	

S527.29
NOISE
SOLUTION

L50C(S527B/L550B/L1510B) Schematic

CONTENTS

SCHEMATIC	SHEET
1. Contents, Revision History	1
2. gmZAN1/2	2
3. MCU(MTV312M)	3
4. LVDS & Power	4
5. AUDIO & USB	5
6. OSD	6
7. BLOCK DIAGRAM	7

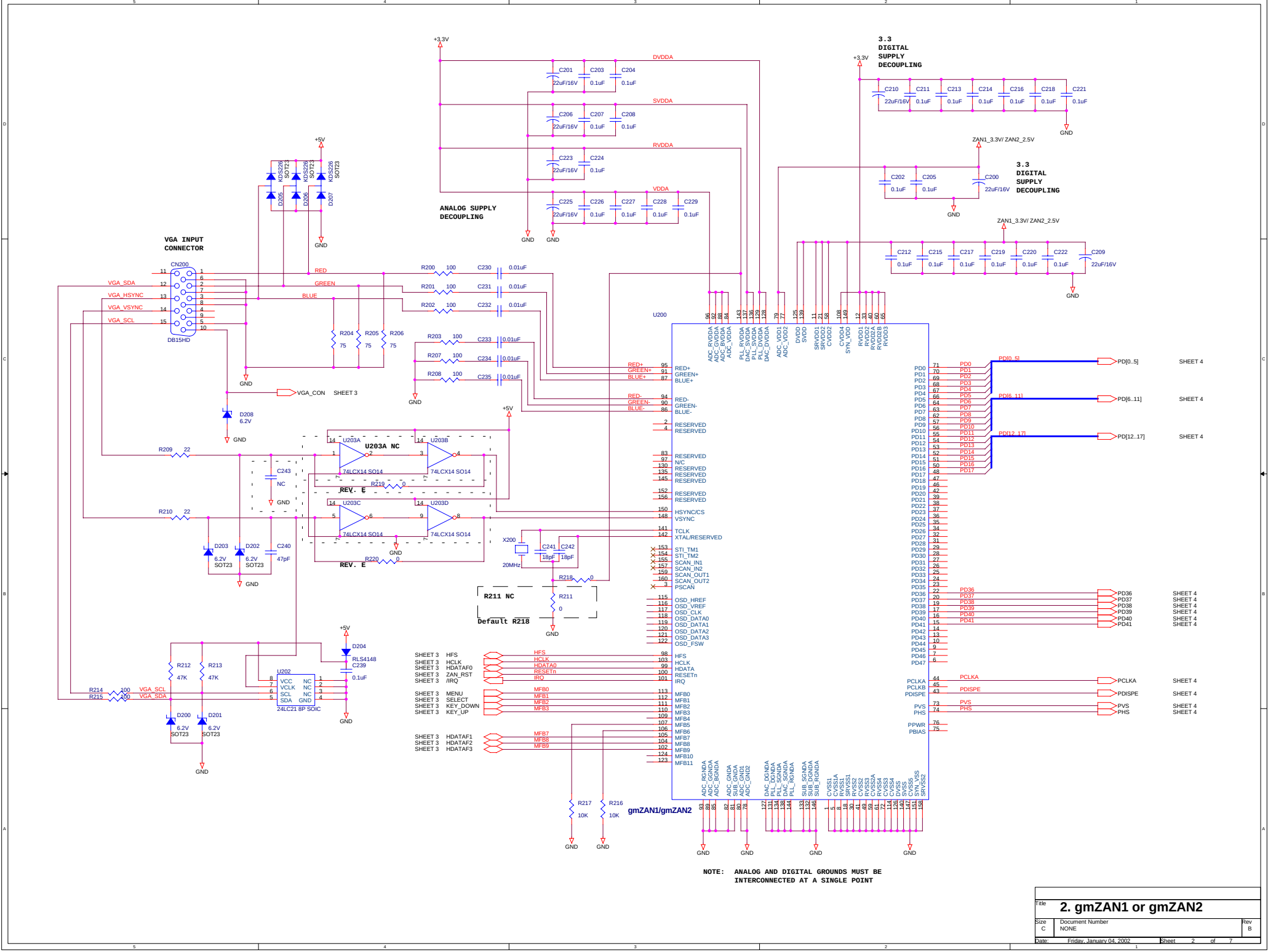
REVISION HISTORY

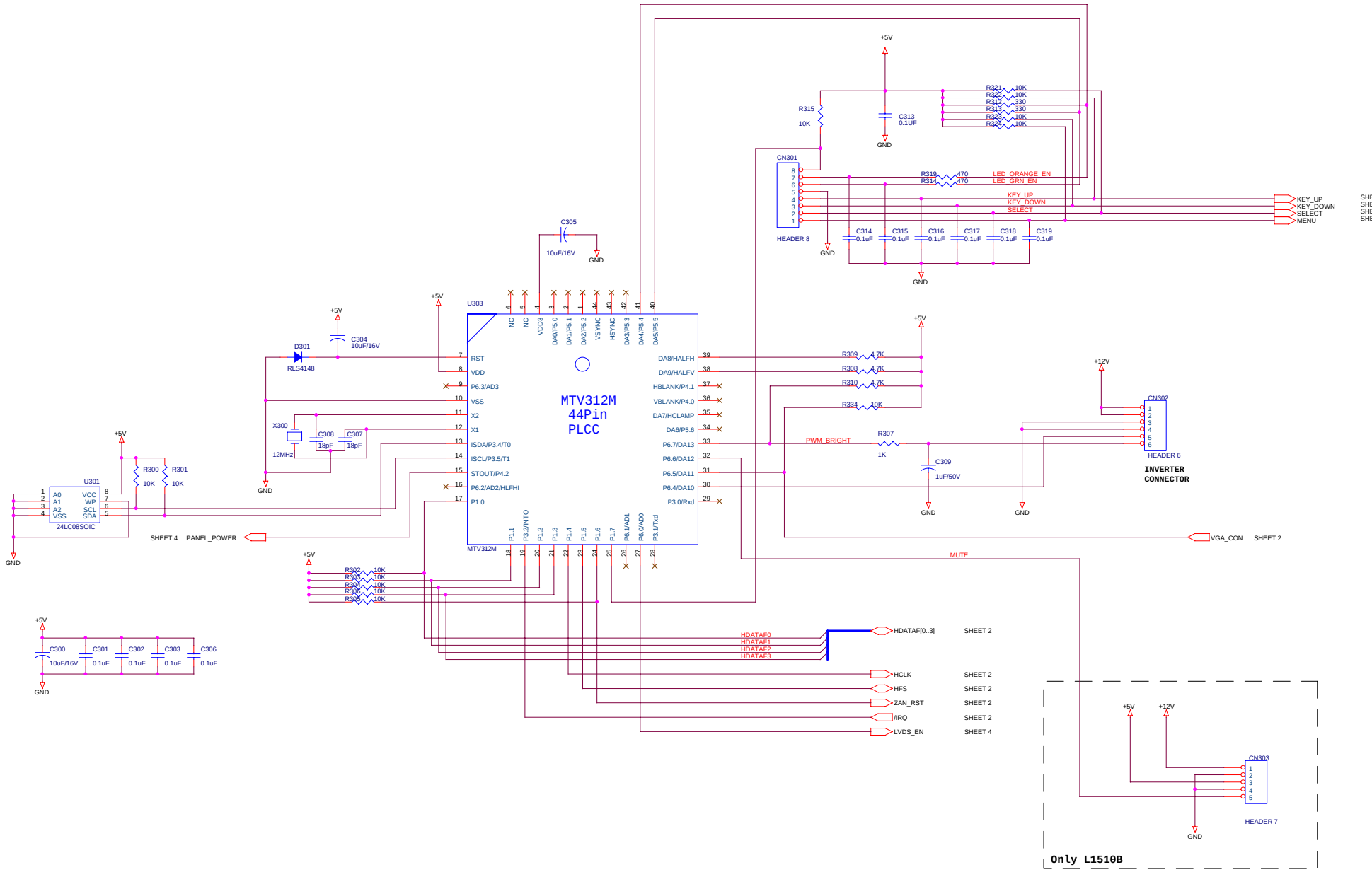
Date	Author	Ver	Comments
01.09.04	G.H.NAM	A	Initial release ver A
02.01.03	W.S.IM	B	L1510B MP

Title
1. Contents

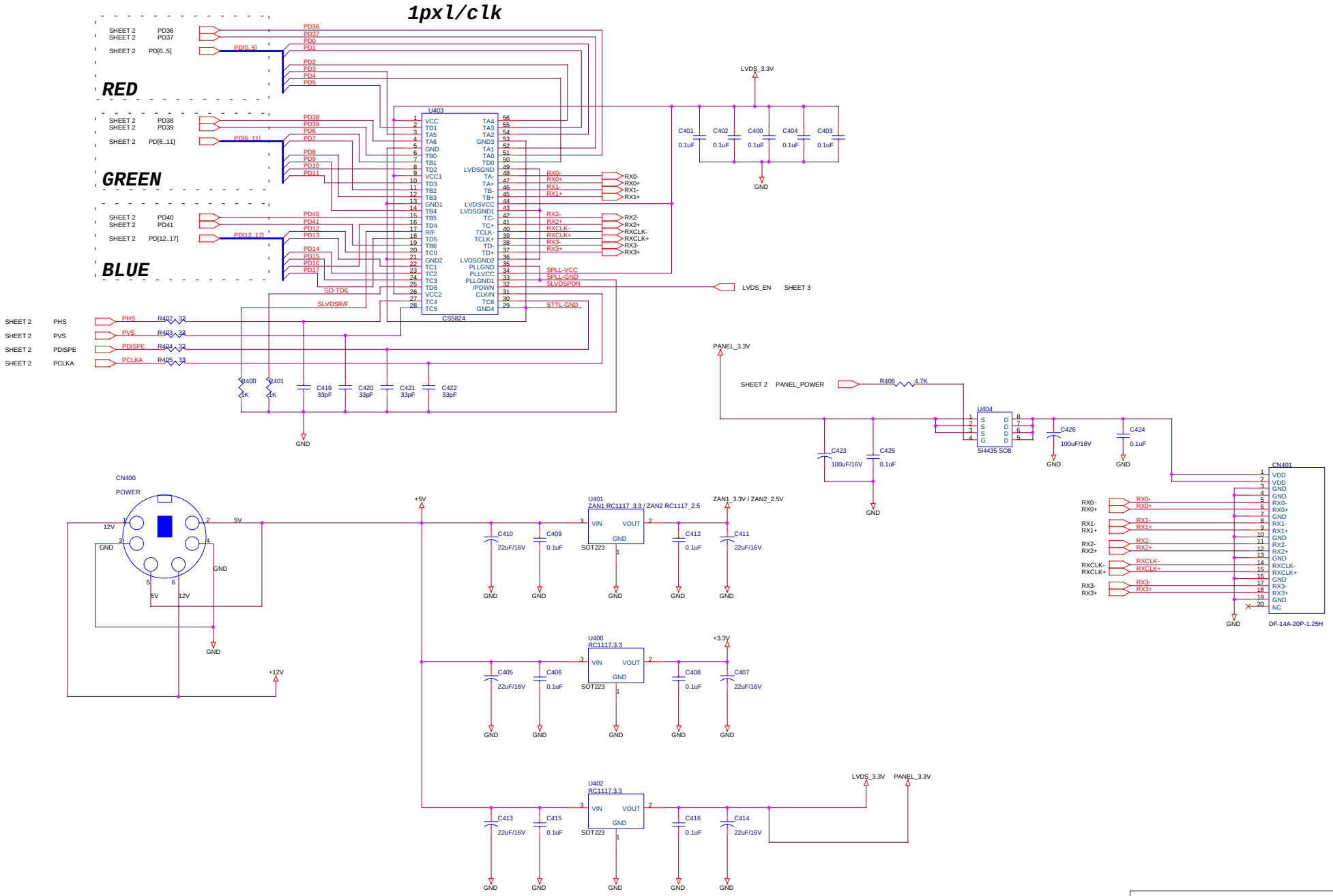
Size	Document Number	Rev
B	NONE	B

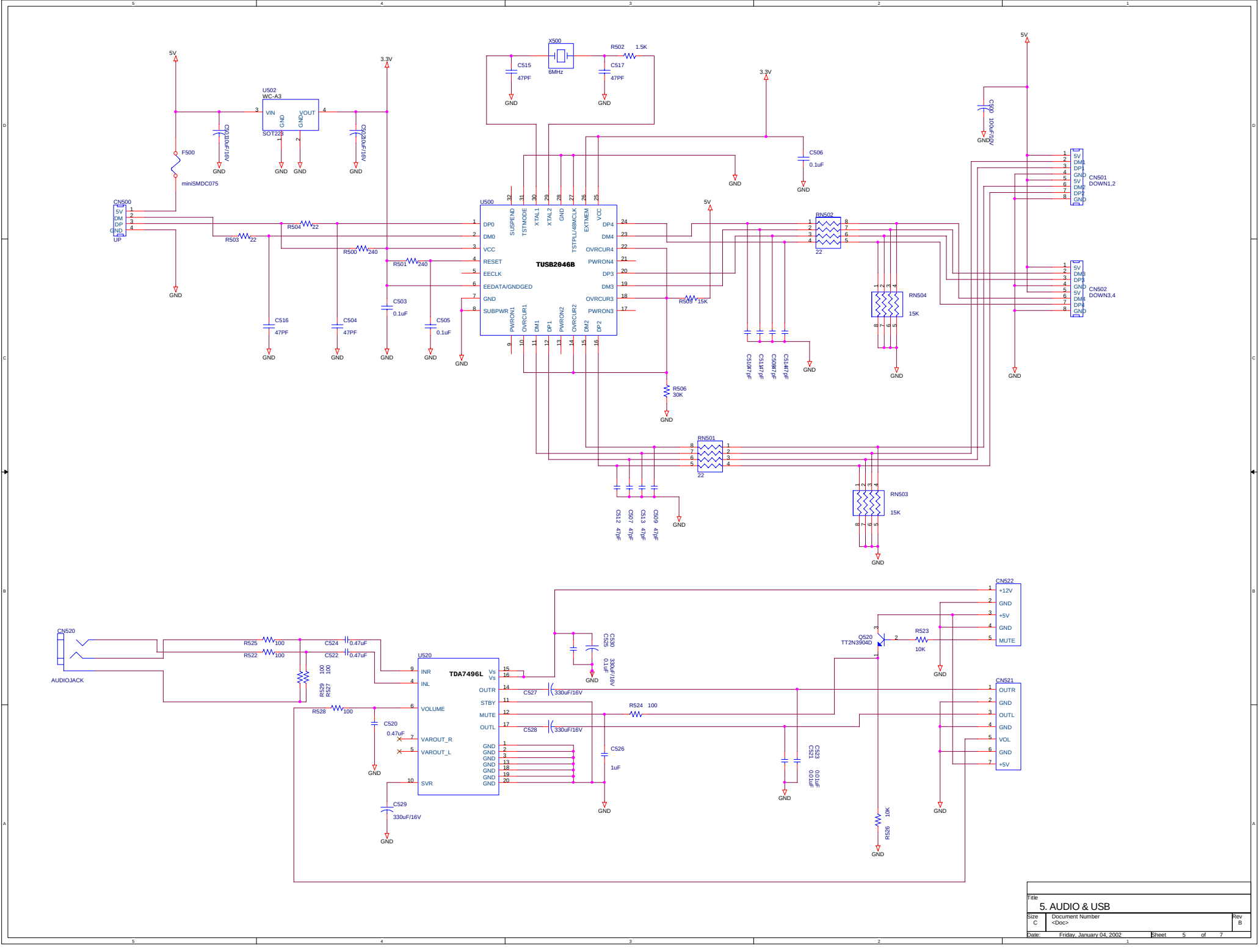
Date: Friday, January 04, 2002 Sheet 1 of 7


3.3 DIGITAL SUPPLY DECOUPLING
ANALOG SUPPLY DECOUPLING
VGA INPUT CONNECTOR
CN200
DB15HD
VGA_SDA
VGA_HSYNC
VGA_VSYNC
VGA_SCL
RED
GREEN
BLUE
VGA_CON SHEET 3
U203A NC
74LCX14 SO14
REV. E
R211 NC
Default R218
U200
gmZAN1/gmZAN2
U202
24LC21 8P SOIC
NOTE: ANALOG AND DIGITAL GROUNDS MUST BE INTERCONNECTED AT A SINGLE POINT
Title
2. gmZAN1 or gmZAN2
Size C
Document Number NONE
Rev B
Date: Friday, January 04, 2002
Sheet 2 of 7

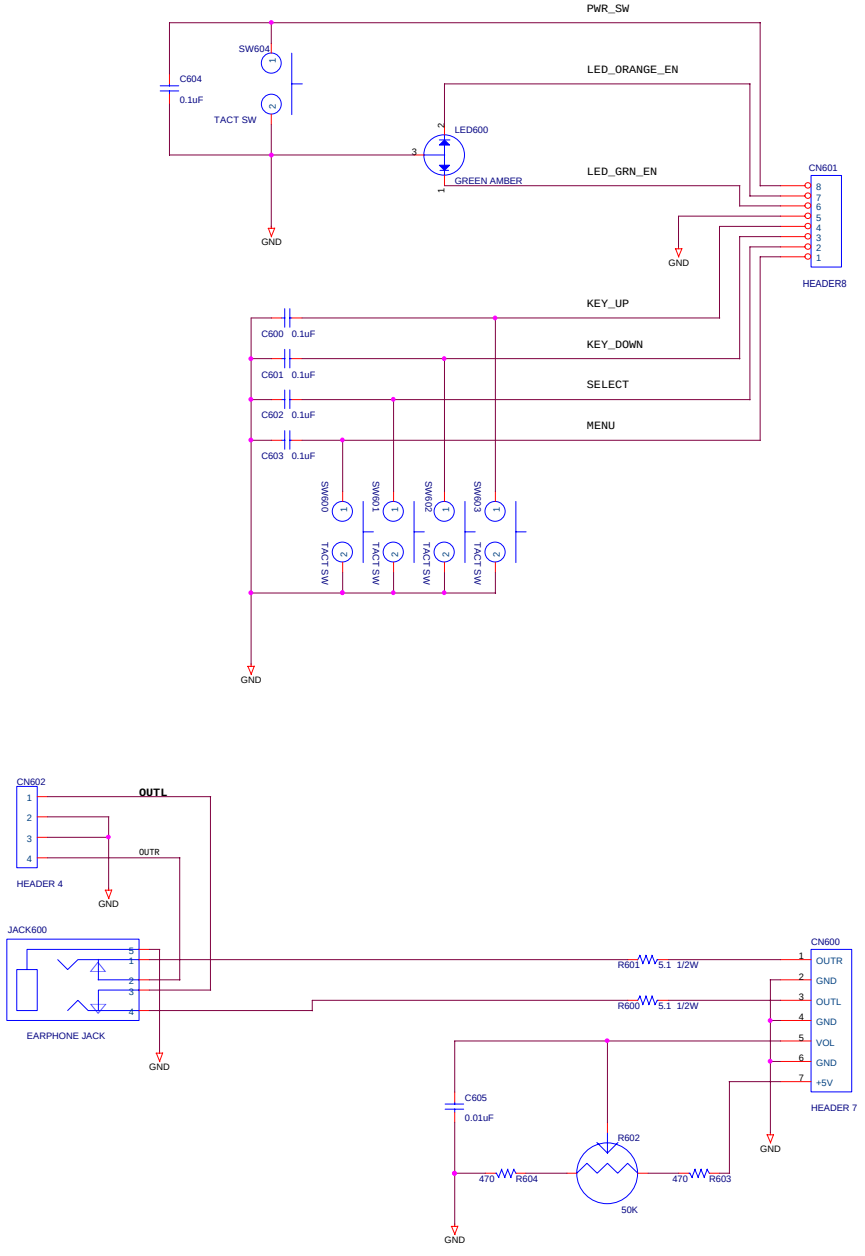


Title	3. MCU(MTV312M)	
Size C	Document Number NONE	Rev B
Date: Friday, January 04, 2002	Sheet 3 of 7	


1pxl/clk
RED
GREEN
BLUE
U403
CS5824
LVDS_3.3V
LVDS_EN
SHEET 3
PANEL_3.3V
PANEL_POWER
R406 4.7K
U404
SI4435 SO8
CN400
POWER
CN401
DF-14A-20P-1.25H
U401
ZAN1 RC1117_3.3 / ZAN2 RC1117_2.5
U400
RC1117.3.3
U402
RC1117.3.3
SOT223
+5V
+12V
+3.3V
ZAN1_3.3V / ZAN2_2.5
GND



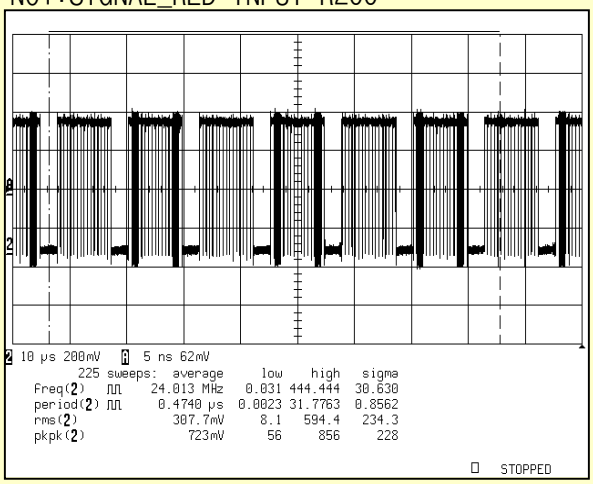
Title	5. AUDIO & USB	
Size C	Document Number <Doc>	Rev B
Date: Friday, January 04, 2002	Sheet 5 of 7	



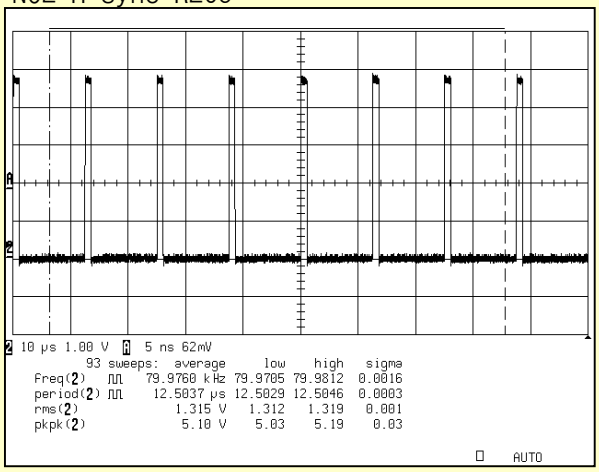
Title	<Title>	6. OSD
Size C	Document Number <Doc>	Rev B
Date: Friday, January 04, 2002	Sheet 6 of 7	

Wave Form

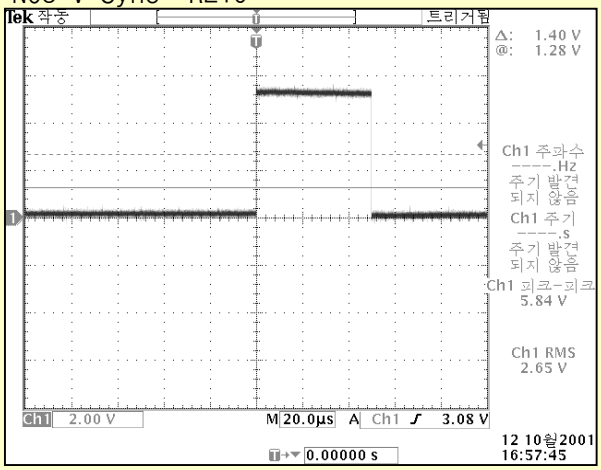
N01:SIGNAL_RED INPUT R200



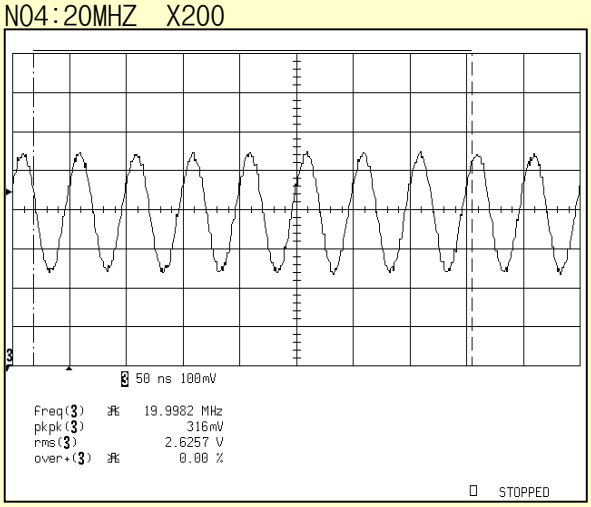
N02:H-sync R209



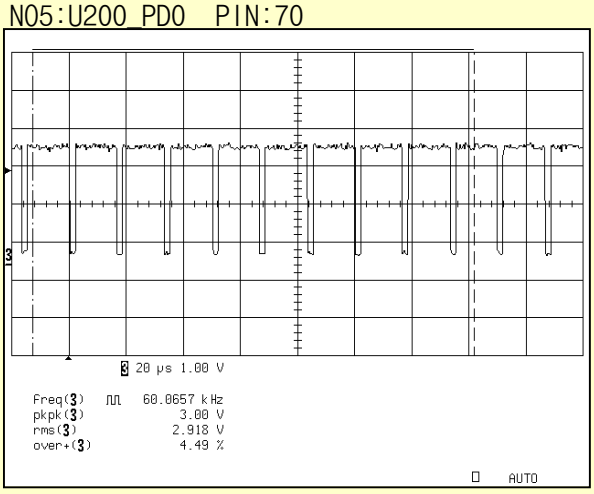
N03:V-Sync R210



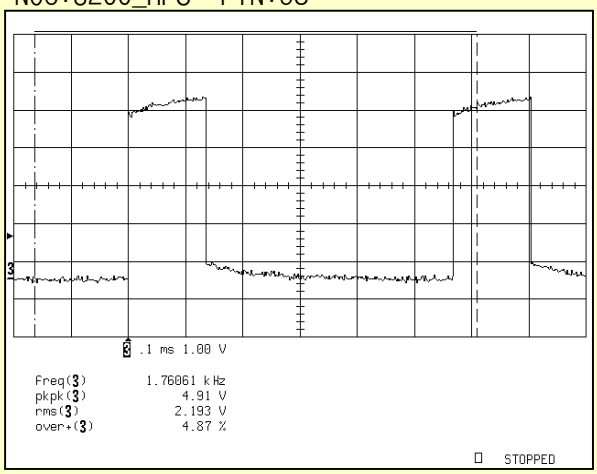
N04:20MHZ X200



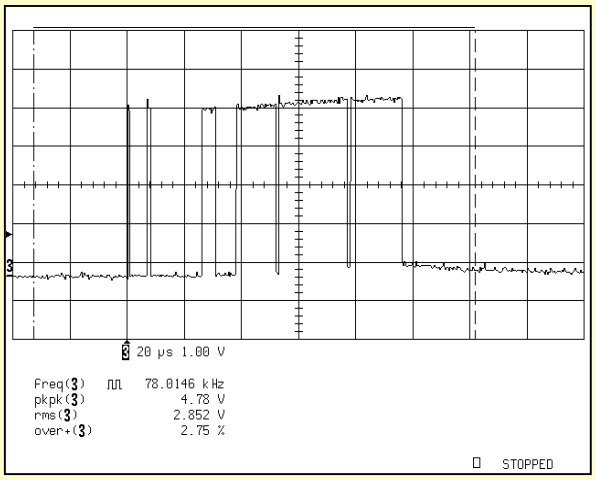
N05:U200_PD0 PIN:70



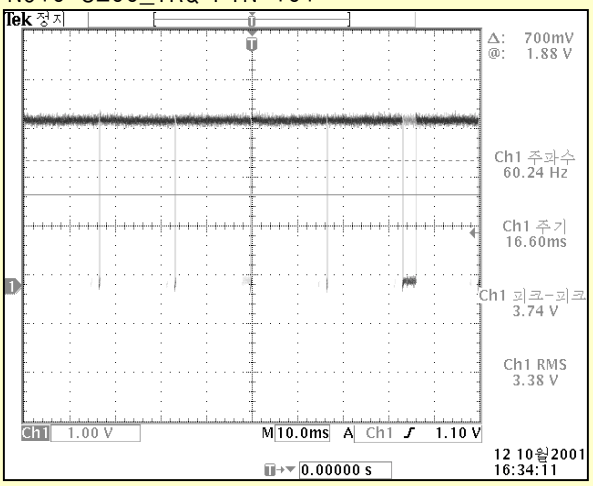
N06:U200_HFS PIN:98



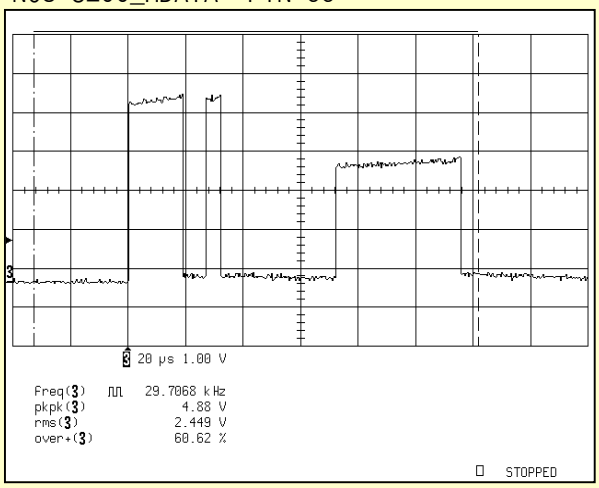
N07:U200_HCLCK PIN:103



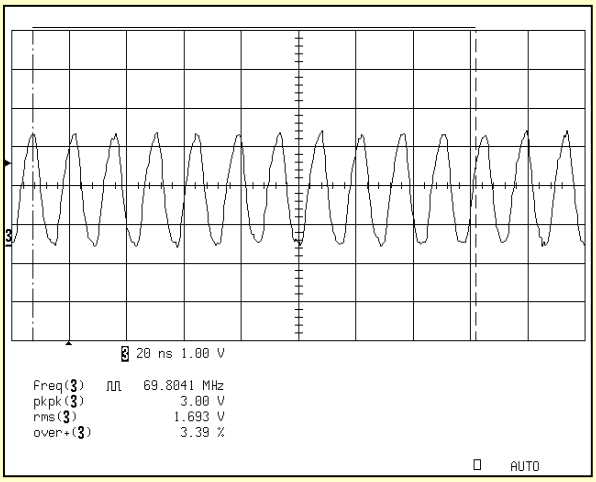
N010:U200_IRQ PIN:101



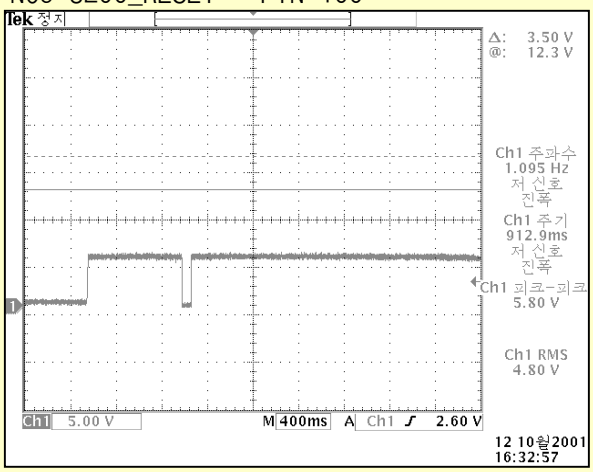
N08:U200_HDATA PIN:99



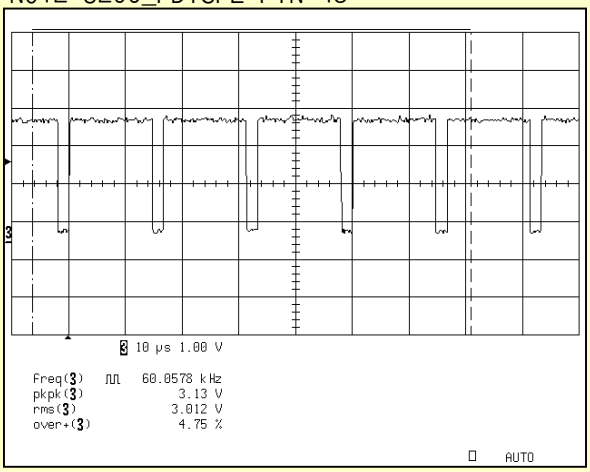
N011:U200_PCLLKA PIN:44



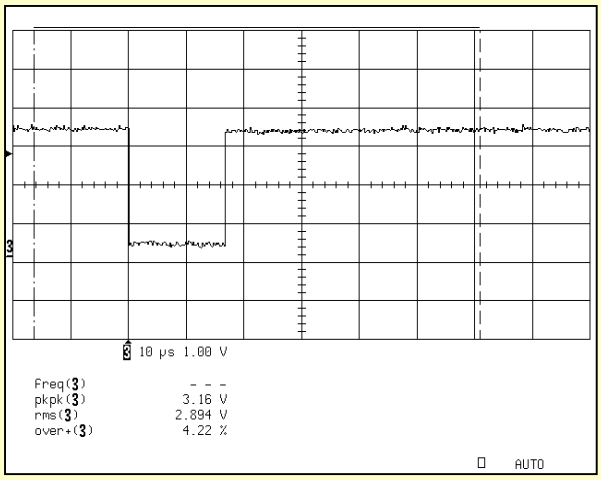
N09:U200_RESET PIN:100



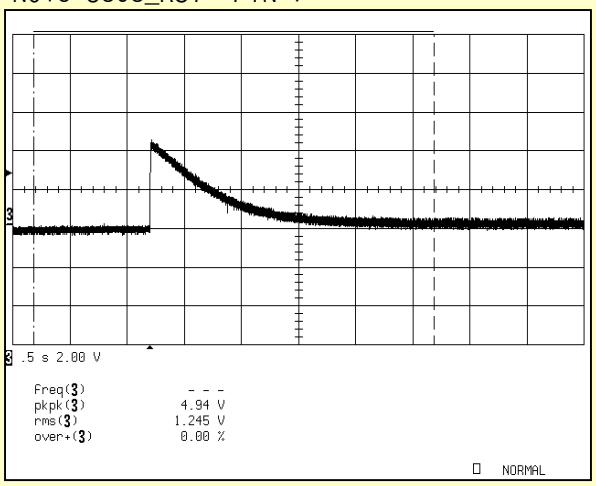
N012:U200_PDISPE PIN:43



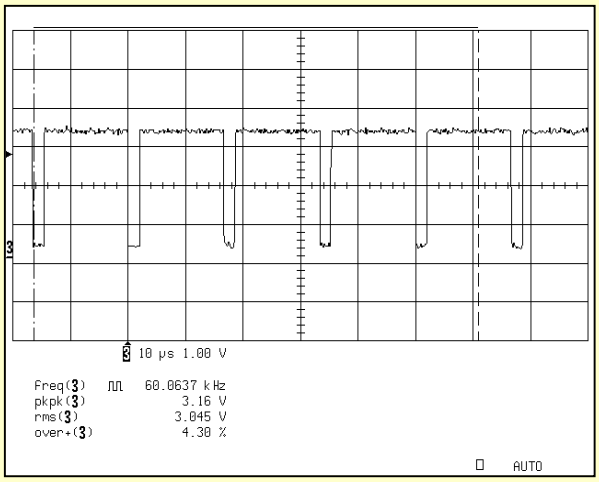
NO13:U200_VS PIN:73



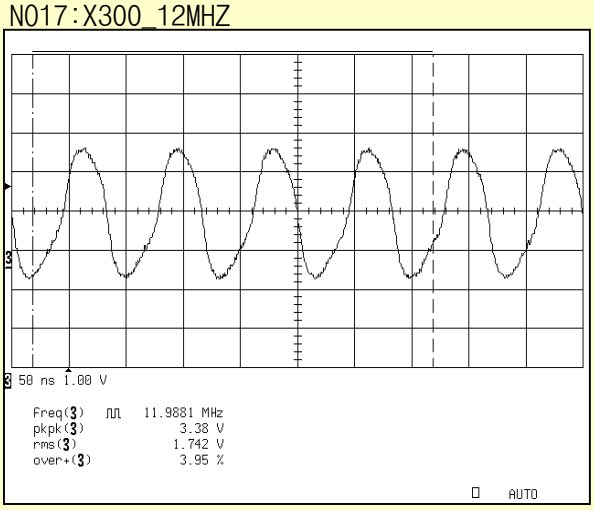
NO16:U303_RST PIN:7



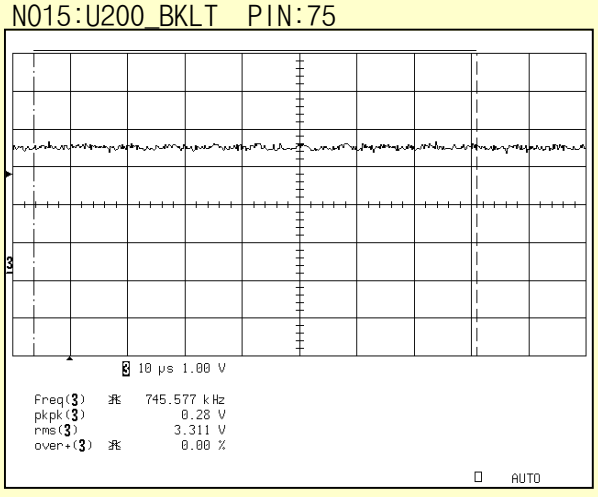
NO14:U200_HS PIN:74



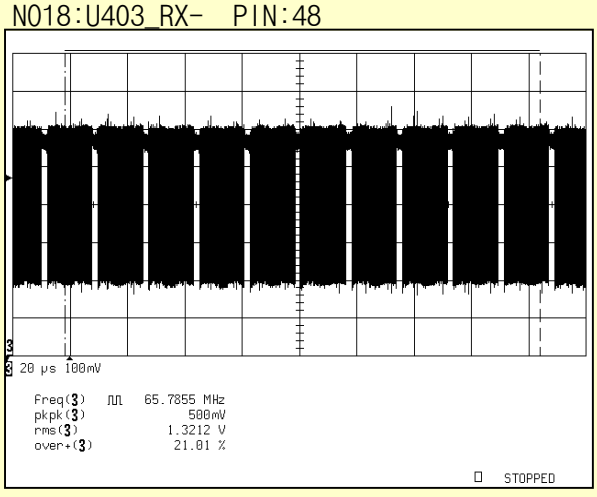
NO17:X300_12MHZ



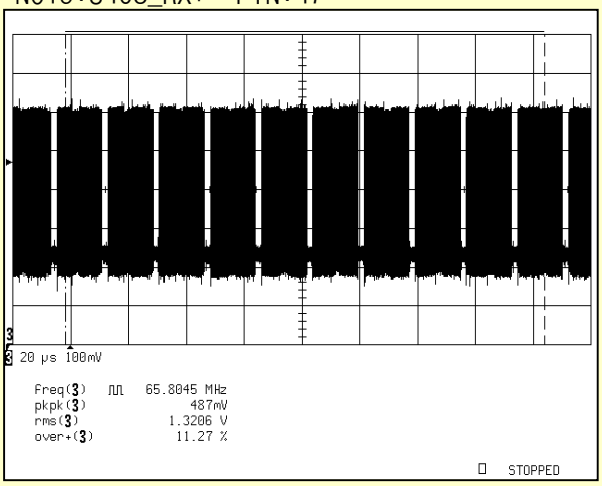
NO15:U200_BKLT PIN:75



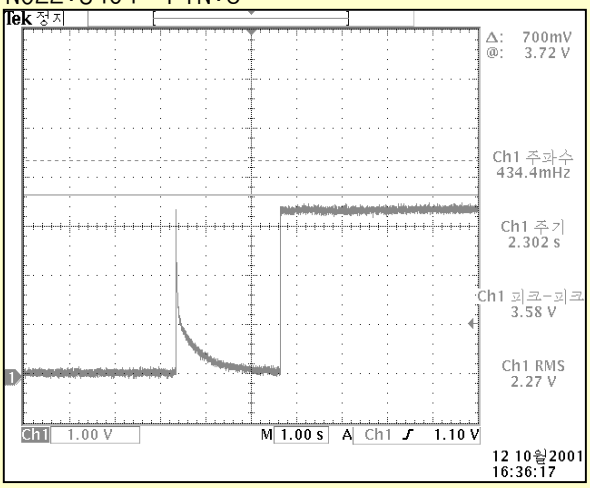
NO18:U403_RX- PIN:48



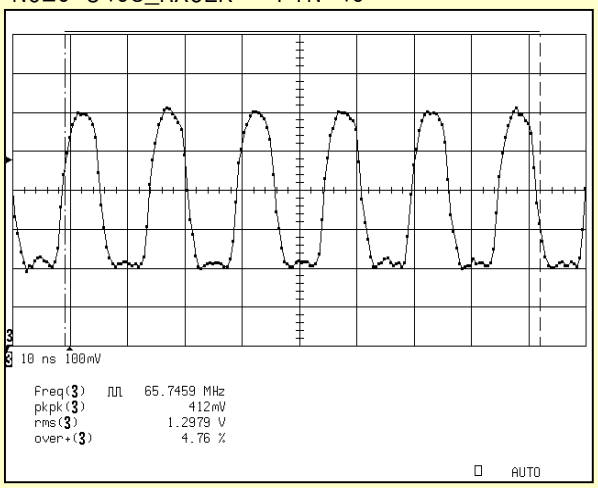
N019:U403_RX+ PIN:47



N022:U404 PIN:5



N020:U403_RXCLK- PIN:40



N021:U403_RXCLK+ PIN:39