General Information

Covers Models:
CF 9528 NFT
CF 9633 NFT
CRT: 28" & 33"

Service Adjustments

Alignment

38.9 MHz and AFC (TP2)

Connect a 38.9 MHz intermediate frequency generator to the tuner's IF output pin 17 and adjust the core L 4 so as to obtain 3.5V at pin 44 of TDA 8361/2.

Power Supply (TP3)

Measure the direct voltage at the terminals of diode DJ1 or D38 and potentiometer R162 so as to obtain a voltage of 142/152 V.

AGC (TP1)

Apply a 60 dBuV (+/- 1dB) RF signal, band III, channel 10 - to 12, and adjust potentiometer R111 so as to obtain a voltage of about 8V at tuner pin no. 5. (This voltage depends on the tuner used so check on the letter's characteristics.)

White Setting

1: Tune to a channel with colour test-pattern signal.
2: Position level potentiometers R18, R15, R14 and gain potentiometers R3 and R9 on the CRT socket, locating centrally.
3: Adjust the TV receiver to maximum brightness, minimum colour and contrast.
4: Switch the TV to AV using the corresponding button on the remote control.
5: Adjust potentiometer G2 (EHT transformer) to obtain a barely visible screen. The screen usually appears with a predominant colour hue.
6: Adjust the level potentiometers of the order two cathodes that are different from the predominating colour in order to obtain the white screen. If, for example, the predominant colour of the screen is red, the potentiometers of the blue cathode R14 and the green cathode R15 are adjusted.
7: Return to TV mode with the appropriate remote control button.
8: Check that the hue of the colours of the colour of test pattern picture are correct. If necessary adjust the potentiometers R3-R9.

Vertical Centring

1: Adjust R194 (VA) for proper vertical height.
2: Adjust R192 (VL) for proper vertical linearity.

Cut/solder the R215 and or R216 in order to obtain the right vertical geometric centring between CRT and signal (for example, use a test pattern signal).

Horizontal Centring and East-West Correction

1: Adjust R186 (HC) for proper horizontal centring.
2: Adjust R205 (HA) for proper horizontal width.
3: Adjust R200 (OW) for proper pin-cushion.
4: Adjust R203 (TZ) for proper trapezium.

Alignment for Auto Cut-Off

38.9 MHz and AFC (TP2)

Connect a 38.9 MHz intermediate frequency generator to the tuner's IF output pin 17 and adjust the core L 4 so as to obtain 4.5V at pin 9 of TDA 8361/2A.

Power Supply (TP3)

Measure the direct voltage at the terminals of diode DJ1 or D38 and potentiometer R162 so as to obtain a voltage of 142/152 V.

AGC (TP1)

Apply a 60dBuV (+/- 1dB) RF signal, band III, channel 10-to-12, and adjust potentiometer R111 so as to obtain a voltage of about 8V at tuner pin no. 5 (This voltage depends on the tuner used so check on the letter's characteristics.)

White Setting

Adjustment with Analogue Voltmeter
1: Power on TV Set.
2: Tune to a signal with white screen.
3: Contrast control set to minimum.
4: Adjust brightness to 2.5V DC on pin 17 TDA 8361/2A.
5: Analogue voltmeter 200V DC full scale.
6: Check for the highest PT cathode voltage than adjust it for 165 V DC via G2 potentiometer (on EHT transformer).

Vertical Centring

1: Adjust R194 (VA) for proper vertical height.
2: Adjust R192 (VL) for proper vertical linearity.

Cut/solder the R215 and/or R216 and/or R257 in order to obtain the right vertical geometric centring between CRT and signal. (For example, use a test-pattern).

Horizontal Centring and East/West Correction

1: Adjust R186 (HC) for proper horizontal centring.
2: Adjust R205 (HA) for proper horizontal width.
3: Adjust R200 (OW) for proper pin cushion.
4: Adjust R203 (TZ) for proper trapezium/

Functional Description of Monochip TDA 8361/2

IF Amplifier

The amplifier contains three differential stages with typical 60 dB dynamic control. The demodulator's polarity is suited for both positive and negative modulation in the TDA 8362 version (multi-standard PAL, SECAM, L, L') **and for only negative modulation in TDA 8361**.

The AFC circuit is driven by the same reference signal as the video demodulator. The AFC output voltage varies in the range 0—6V. The circuit for identifying the presence of the signal in the transmission channel works independently of the synchronisation circuit: 0V. No identification and mute sound; 8V. Identification and 4.43 MHz chroma frequency, 6V. Identification and chroma frequency 3.58 MHz.

The AGC system controls the IF amplifier gain is such a way that the amplitude of the output video signal remains contrast. The voltage of the AGC capacitors (pin 48) takes into account the IF amplification level. A second loop acts on the tuner to amplify the IF input. The amplification level is regulated by potentiometer R111.

Sound Circuit

The inter-carrier signal is amplified/limited and demodulated by a PLL (phase locked loop). The PLL circuit automatically locks onto the incoming signal. The volume controls the amplitude of the composite audio signal (pin 5). (700mV Max.)

Horizontal and Vertical Synchronisation Circuit

Upstream of the sync separator there is an amplifier that raises the synchronism pulse to a fixed level. The separated synchronism pulses are forwarded to the phase and coincidence detectors. The coincidence detector is used to synchronise the line oscillator and to identify the transmission channel. The integrated circuit contains a start-up circuit for the horizontal output (pin 36). The driving pulses for the vertical are generated by a divided circuit. The components for the generation of the vertical ramp are connected to pin 42. The feedback voltage from the vertical amplification stage is connected to pin 41.

Video Filters

The integrated circuit contains a chroma trap and band-pass circuit. The filters are implemented by means of circuit with gyrators. The chroma trap is active when the chroma input pin (pin 16) is connected to ground or directly to the power supply. If pin 16 is held at intermediate voltage, the trap does not operate and therefore S-VHS application is possible. The luminance delay line and the delay for peaking circuit are implemented by means of circuit with gyrators.

Colour Decoder

The colour decoder contains a quartz-controlled oscillator, a killer circuit and a colour difference demodulator. The 90° phase deviation is effected internally. The decoder adapts automatically to the PAL and NTSC system. For this purpose there are two pins 35 and 34. With TDA 8362 a PAL/SECAM/NTSC automatic multi-standard decoder may be built through the addition of the SECAM TDA 8395 decoder.

RGB Output Circuit

The colour difference signals enter the matrices with the luminance signal to obtain the RGB signals. The integrated circuit handles the internal signals and those coming from outside (SCART connector). Brightness and contrast act both on the internal signals and the external ones. Pin 21 of the fast blanking has a second, 4V threshold level. When this level is exceeded the RGB outputs are blocked and the OSD signals are sent directly to the output amplifier. The RGB signals have an amplitude of about 4V under nominal operating conditions.

Functional Description of Monochip TDA 8361/2A

IF Amplifier

The amplifier contains three differential stages with typical 60 dB dynamic control. The demodulator's polarity is suited for both positive and negative modulation in the TDA 8362A version (multi-standard PAL, SECAM, L, L'), **and only for negative modulation in TDA 8361A**.

The AFC circuit is driven by the same reference signal as the video demodulator. The AFC output voltage varies in the range 0—6V. The circuit for identifying the presence of the signal in the transmission channel works independently of the synchronisation circuit: 0v, no identification and mute sound; 8V, identification and 4.43 MHz chroma frequency; 6V, identification and chroma frequency 3.58 MHz.

The AGC system controls the IF amplifier gain in such a way that the amplitude of the output video signal remains constant. The voltage loop of the AGC capacitors (pin 48) takes into account the IF amplification level. A second loop acts on the tuner to amplify the IF input. The amplification level is regulated by potentiometer R111.

Sound Circuit

The inter-carrier signal is amplified/limited and demodulated by a PLL (phase locked loop). The PLL circuit automatically locks on to the incoming signal. The volume controls the amplitude of the composite audio signal (pin 5). (700mV Max.)

Horizontal and Vertical Synchronisation Circuit.

Upstream of the sync. separator there is an amplifier that raises the synchronism pulse to a fixed level. The separated synchronism pulses are forwarded to the phase and coincidence detectors. The coincidence detector is used to synchronise the line oscillator and to identify the transmission channel. The integrated circuit contains a start-up circuit for the horizontal output (pin 36). The driving pulses for the vertical ramp are generated by a divider circuit. The components for the generation of the vertical ramp are connected to pin 43. The feedback voltage from the vertical amplification stage is connected to pin 42.

Video Filters

The integrated circuit contains a chroma trap and band-pass circuit. The filters are implemented by means of circuit with gyrators. The chroma trap is active when the chroma input pin (pin 16) is connected to ground or directly to the power supply. If pin 16 is held at intermediate voltage, the trap does not operate and therefore S-VHS application is possible. The luminance delay line is implemented by means of circuit with gyrators.

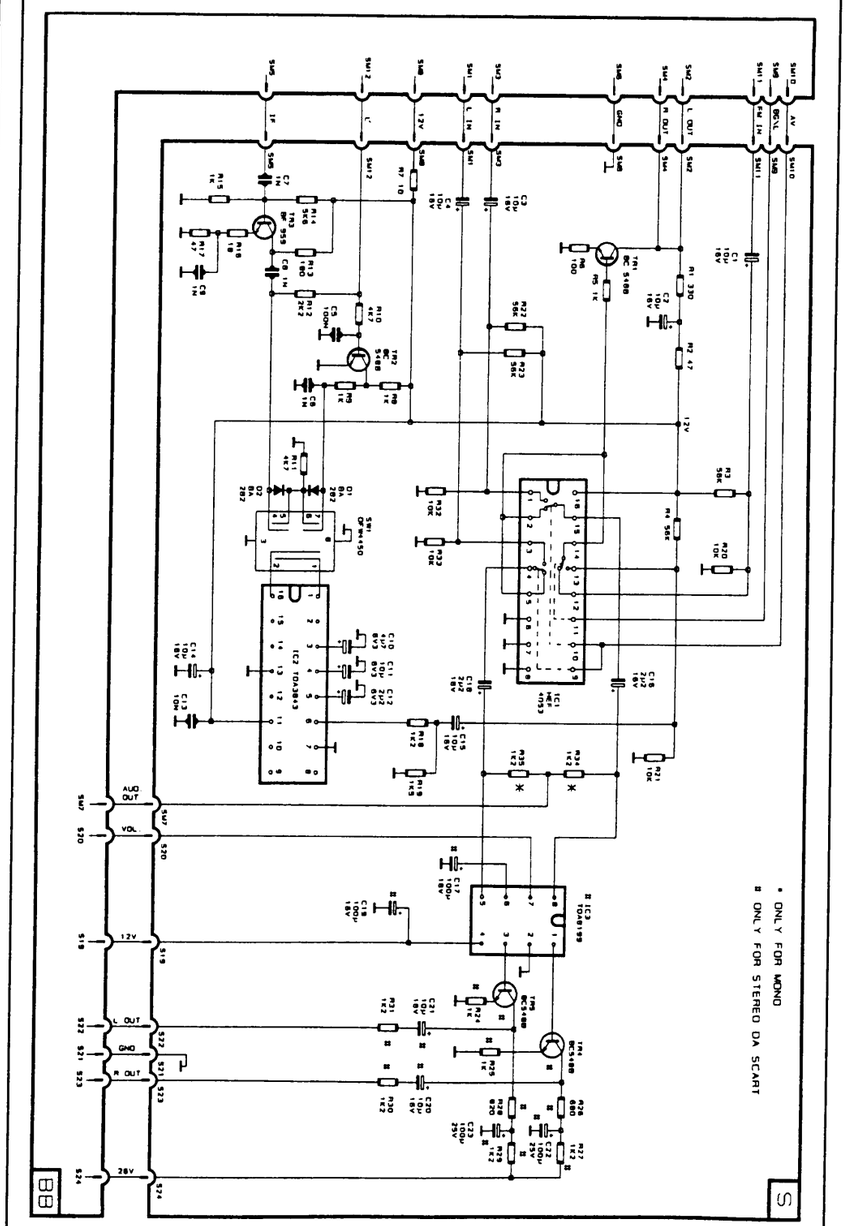
Colour Decoder

The colour decoder contains a quartz-controlled oscillator, a killer circuit and a colour difference demodulator. The 90° phase deviation is effected internally. The decoder adapts automatically to the PAL and NTSC system. For this purpose there are two pins 35 and 34. With TDA 8362A, a PAL/SECAM/NTSC automatic multi-standard decoder may be built through the addition of the SECAM TDA 8395 decoder.

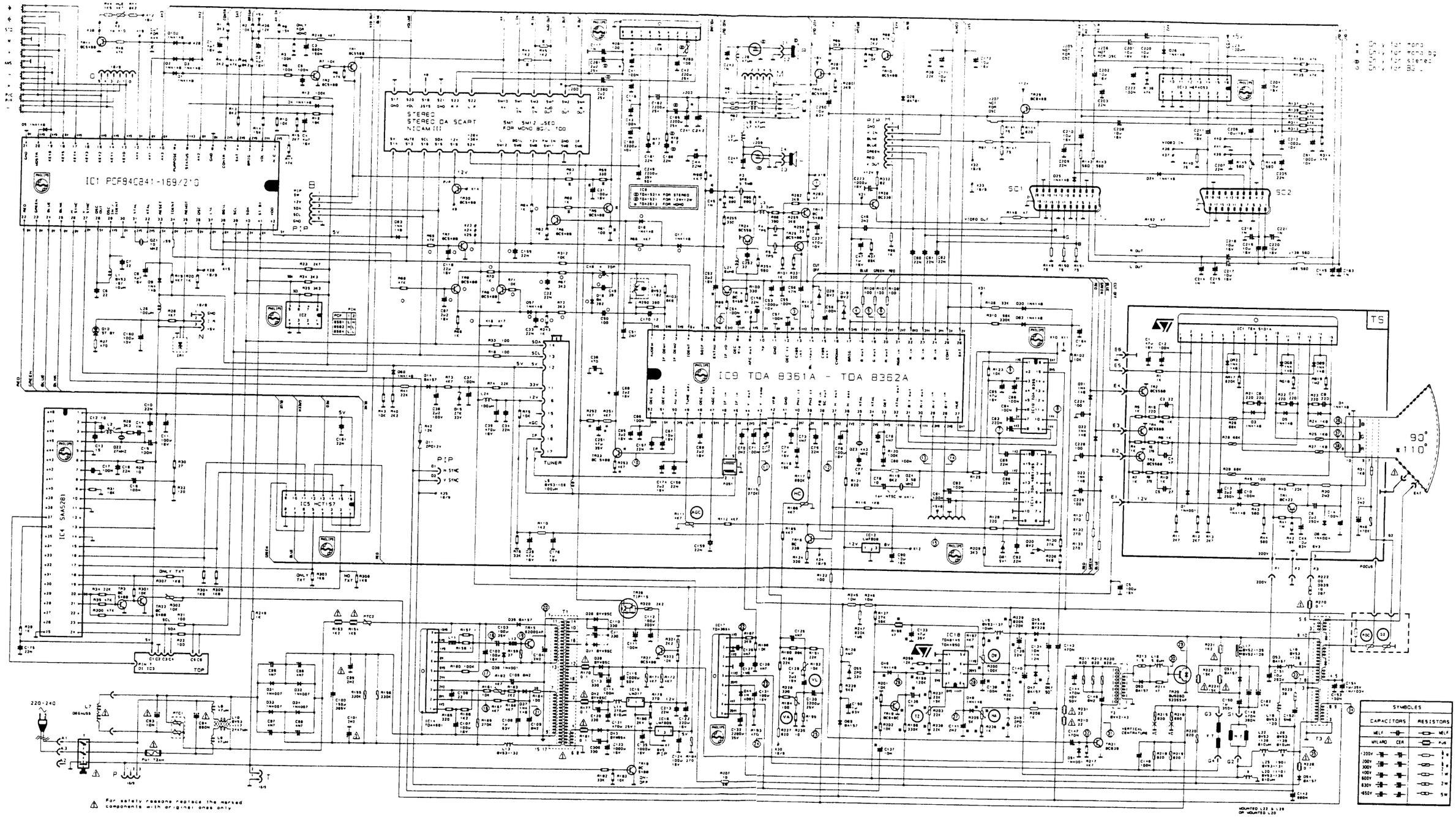
RGB Output Circuit

The colour difference signals enter the matrices with the luminance signal to obtain the RGB signals. The integrated circuit handles the internal signals and those coming from outside (SCART connector). Brightness and contrast act both on the internal signals and the external ones. Pin 21 of the fast blanking has a second, 4V, threshold level. When this level is exceeded the RGB outputs are blocked and the OSD signals are sent directly to the output amplifier. The RGB signals have an amplitude of about 4V under nominal operating conditions.

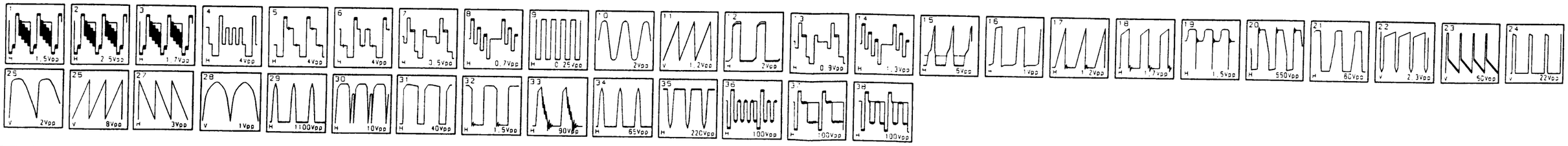
Audio L Diagram



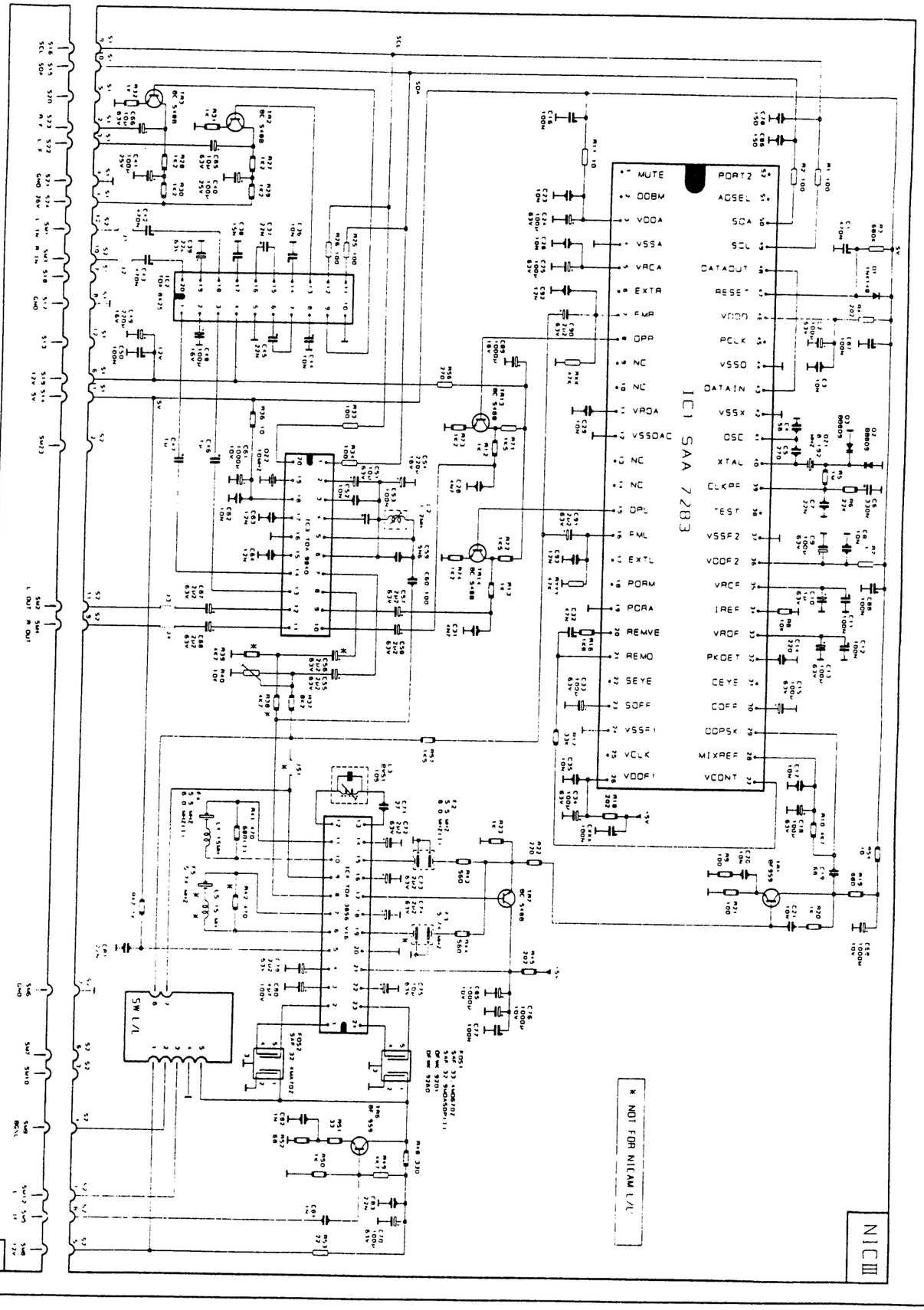
Main Diagram



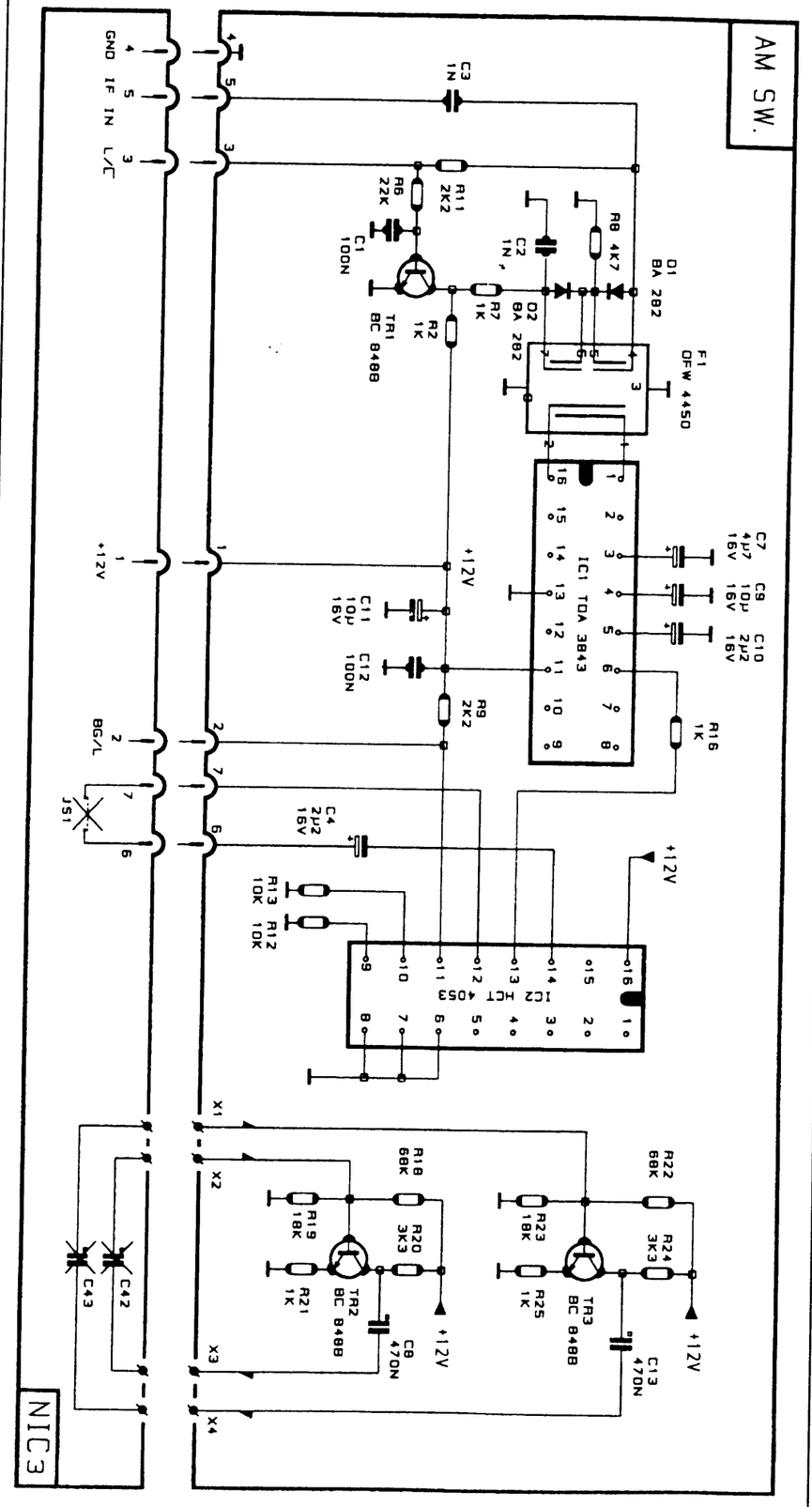
Waveforms



Nicam 3 Diagram



Nicam L Diagram



Stereo Decoder Diagram