8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

TC6208 - PUMA

8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

TAMARACK MICROELECTRONICS INC.

4FL No. 106 Hsin-Tai Wu Road,
Sec. 1, Hsichih,
Taipei Hsien, Taiwan R.O.C.
TEL: 886-2-2696-1669
FAX:886-2-2696-2220
www.tmi.com.tw

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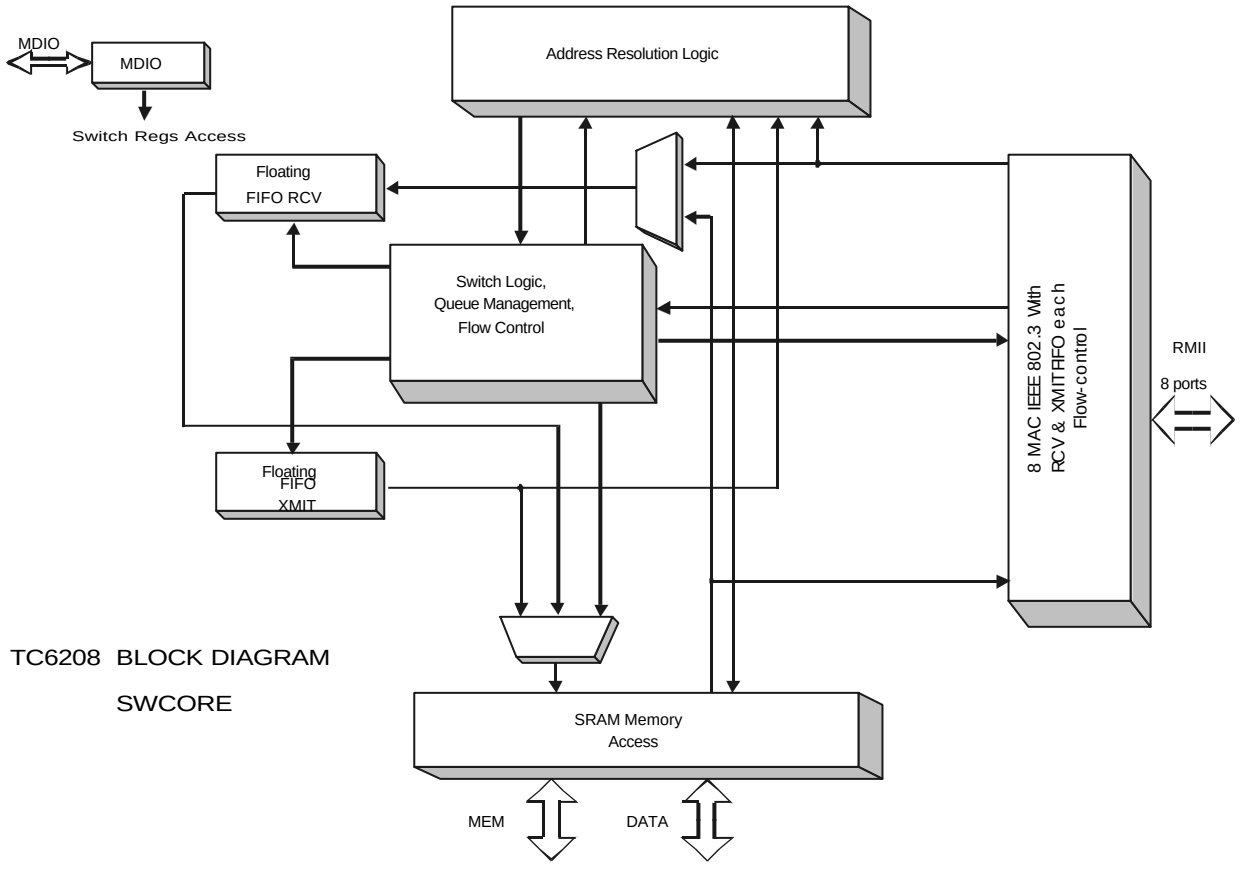
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

Features

- Stand Alone Switch On A Chip.
- 8 Ethernet 10/100 ports.
- MultipleTC6208 can produce larger switches by trunking.
- 10/100 selectable for each port.
- Full/Half Duplex for each port.
- Highly integrated switching logic, including the MAC functions on a single ASIC. All switching done in hardware.
- 16K MAC address table /chip.
- Flow-control for Full and Half Duplex.
- QoS, Port priority, 3 priority rates.
- Trunking.
- Maximum throughput.
- Broadcast throttling.
- RMII interface.
- Serial EEPROM Interface.
- MDIO master to read/write the PHY' s.
- 0.35 micron, 3.3 V technology.
- Packaged in 208 QFP.
- Using one pipelined burst SSRAM 64Kx64.



TC6208 BLOCK DIAGRAM

SWCORE

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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

General

- TC6208 is intended to produce low cost, high performance, with a rich set of features for desktop switches.
- MultipleTC6208 can produce larger switches by off PHY trunking.
- It is as a stand-alone unmanaged switch to produce cost effective switches.
- TC6208 is a highly integrated 8 Port 10/100 Ethernet Switch. It contains IEEE 802.3 MAC functions for 8 ports. Each port has its dedicated RCV and XMIT FIFO's with necessary logic to implement flow-control for full and half-duplex conditions. The MAC functions are tailored for high speed and flexible switching.
- Store and Forward. Bad packets are filtered before being forwarded.
- The rules to generate the destination port(s) are according with IEEE 802.1d.
- No packet lost using Flow-control for full-duplex and Back pressure for half-duplex.
- TC6208 support port priority per port basis and QoS (802.1p VLAN priority header, IP header). This will allow effective video switching in multimedia applications. TC6208 have 3 priority rates: Normal Rate (No Priority), High Rate, Very High Rate.
- With up to 16K MAC addresses on chip. All Address Resolution Functions are hardware implemented.
- Multiple TC6208 can be used to implement unmanaged switches with 8/12/20 ports.
- MAC's size and functions are optimized and friendly coupled with the Switch logic.
- Capable of Flow-control for full-duplex operation according with IEEE 802.3x, back-pressure for half-duplex operation.
- Broadcast throttling to avoid broadcast storms.
- Combinations of ports can be trunked to link multiple switches.
- MDIO master will read/write the PHY's for configuration, automatically on poll bases.

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Description

TheTC6208 is a low cost 8 port 10/100 scalable unmanaged Ethernet switch controller, intended to produce low cost switches without any companion chips or logic.

TC6208 supports a wide variety of switch features and configurations at the maximum performance levels with the lowest number of components per switch.

For unmanaged switches it provides at the lowest cost the highest number of features: wire speed switching, self-learning MAC addresses including aging, flow control (full/half-duplex), trunking, QoS, port priority.

A store-and-forward switching method is implemented using a non blocking architecture to improve the availability and bandwidth. Each TC6208 on a switch handles its own 16K address-lookup table with searching, self-learning, automatic aging, at a very high speed. Multiple queues including normal and high priority queues for each transmitting port.

For networks with QoS environment, TC6208 will forward the coming packets with precedence which have priority setup in their IP header or in their VLAN priority header (QoS).
For networks without QoS compatibility, it provides port priority to allow video servers to broadcast or unicast full color video traffic, that is, all the packets from this priority port(s). Will be forwarded to priority queue(s) of each transmitting port(s), a unique feature for TC6208.
TheTC6208 uses one low-cost, 7 ns, synchronous SSRAM from the PC market to provide speed at a low cost.

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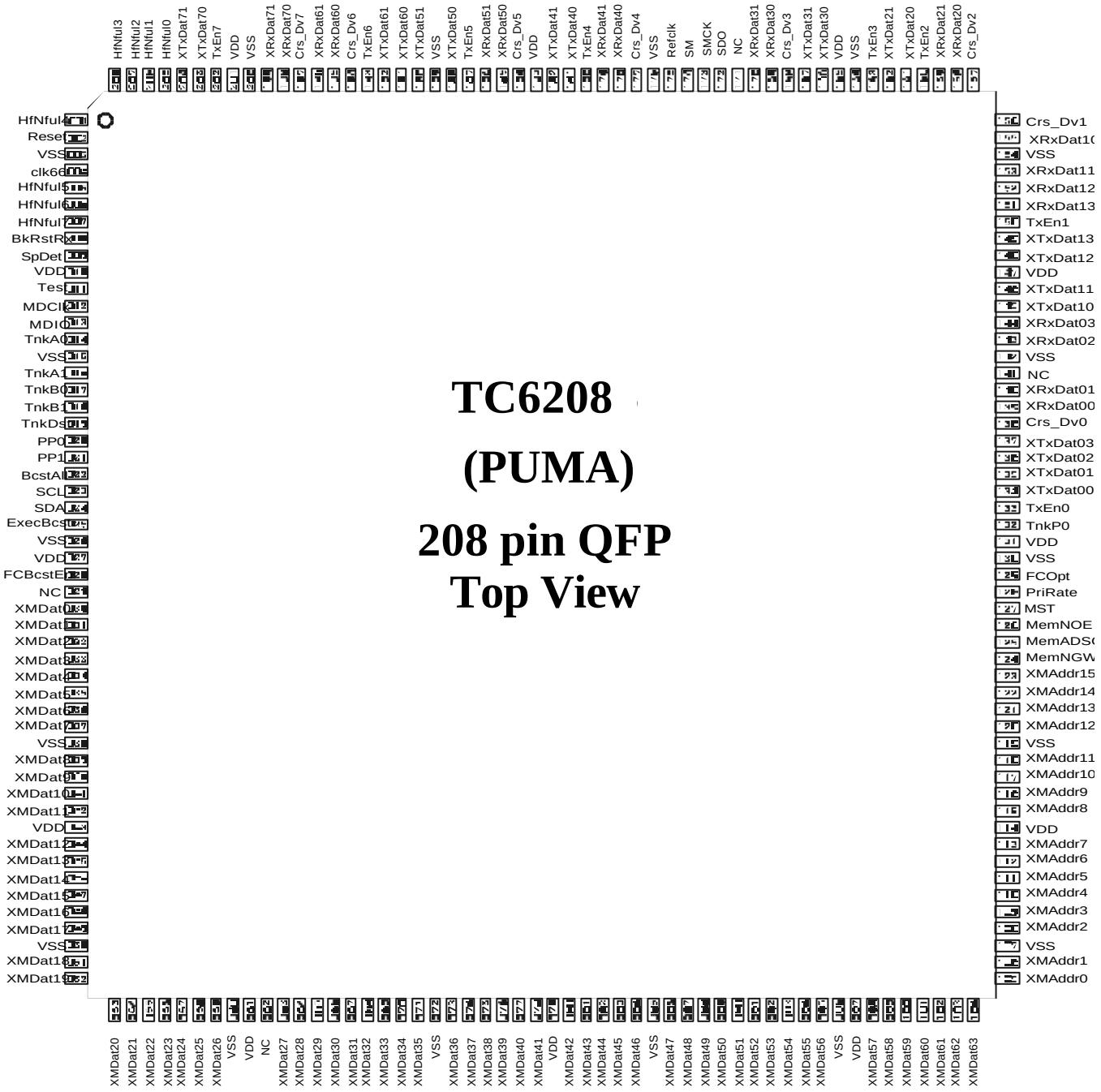
TC6208 Pin Diagram



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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

TC6208 Pin Listing

Pin#	Type	Pin Name	I/O	Type
1	**C&M**	HfNFul4	I	3.3V In
2	**RST**	Reset	I	3.3V In
3	**GND**	VSS	-	GND
4	**CLK**	Clk66	I	3.3V In
5	**C&M**	HfNFul5	I	3.3V In
6	**C&M**	HfNFul6	I	3.3V In
7	**C&M**	HfNFul7	I	3.3V In
8	**C&M**	BkRstRx	I	3.3V In
9	**C&M**	SpDet	I	3.3V In
10	**VDD**	VDD	-	3.3V
11	**C&M**	Test	I	3.3V In
12	**C&M**	MDClk	O	3.3V Out
13	**C&M**	MDIO	I/O	3.3V I/O
14	**C&M**	TnkA0	I	3.3V In
15	**GND**	VSS	-	DGND
16	**C&M**	TnkA1	I	3.3V In
17	**C&M**	TnkB0	I	3.3V In
18	**C&M**	TnkB1	I	3.3V In
19	**C&M**	TnkDst	I	3.3V In
20	**C&M**	PP0	I	3.3V In
21	**C&M**	PP1	I	3.3V In
22	**C&M**	BcstAll	I	3.3V In
23	**C&M**	SCL	O	3.3V Out
24	**C&M**	SDA	I/O	3.3V I/O
25	**C&M**	ExecBcst	I	3.3V In
26	**GND**	VSS	-	DGND
27	**VDD**	VDD	-	3.3V
28	**C&M**	FCBcstEn	I	3.3V In
29	**N.C.**	NC	-	-
30	**MEM**	XMDat0	I/O	3.3V I/O
31	**MEM**	XMDat1	I/O	3.3V I/O
32	**MEM**	XMDat2	I/O	3.3V I/O
33	**MEM**	XMDat3	I/O	3.3V I/O
34	**MEM**	XMDat4	I/O	3.3V I/O
35	**MEM**	XMDat5	I/O	3.3V I/O
36	**MEM**	XMDat6	I/O	3.3V I/O
37	**MEM**	XMDat7	I/O	3.3V I/O
38	**VSS**	VSS	-	DGND
39	**MEM**	XMDat8	I/O	3.3V I/O
40	**MEM**	XMDat9	I/O	3.3V I/O
41	**MEM**	XMDat10	I/O	3.3V I/O
42	**MEM**	XMDat11	I/O	3.3V I/O
43	**VDD**	VDD	-	3.3V
44	**MEM**	XMDat12	I/O	3.3V I/O

Pin#	Type	Pin Name	I/O	Type
45	**MEM**	XMDat13	I/O	3.3V I/O
46	**MEM**	XMDat14	I/O	3.3V I/O
47	**MEM**	XMDat15	I/O	3.3V I/O
48	**MEM**	XMDat16	I/O	3.3V I/O
49	**MEM**	XMDat17	I/O	3.3V I/O
50	**VSS**	VSS	-	DGND
51	**MEM**	XMDat18	I/O	3.3V I/O
52	**MEM**	XMDat19	I/O	3.3V I/O
53	**MEM**	XMDat20	I/O	3.3V I/O
54	**MEM**	XMDat21	I/O	3.3V I/O
55	**MEM**	XMDat22	I/O	3.3V I/O
56	**MEM**	XMDat23	I/O	3.3V I/O
57	**MEM**	XMDat24	I/O	3.3V I/O
58	**MEM**	XMDat25	I/O	3.3V I/O
59	**MEM**	XMDat26	I/O	3.3V I/O
60	**VSS**	VSS	-	DGND
61	**VDD**	VDD	-	3.3V
62	**N.C.**	NC	-	-
63	**MEM**	XMDat27	I/O	3.3V I/O
64	**MEM**	XMDat28	I/O	3.3V I/O
65	**MEM**	XMDat29	I/O	3.3V I/O
66	**MEM**	XMDat30	I/O	3.3V I/O
67	**MEM**	XMDat31	I/O	3.3V I/O
68	**MEM**	XMDat32	I/O	3.3V I/O
69	**MEM**	XMDat33	I/O	3.3V I/O
70	**MEM**	XMDat34	I/O	3.3V I/O
71	**MEM**	XMDat35	I/O	3.3V I/O
72	**VSS**	VSS	-	DGND
73	**MEM**	XMDat36	I/O	3.3V I/O
74	**MEM**	XMDat37	I/O	3.3V I/O
75	**MEM**	XMDat38	I/O	3.3V I/O
76	**MEM**	XMDat39	I/O	3.3V I/O
77	**MEM**	XMDat40	I/O	3.3V I/O
78	**MEM**	XMDat41	I/O	3.3V I/O
79	**VDD**	VDD	-	3.3V
80	**MEM**	XMDat42	I/O	3.3V I/O
81	**MEM**	XMDat43	I/O	3.3V I/O
82	**MEM**	XMDat44	I/O	3.3V I/O
83	**MEM**	XMDat45	I/O	3.3V I/O
84	**MEM**	XMDat46	I/O	3.3V I/O
85	**VSS**	VSS	-	DGND
86	**MEM**	XMDat47	I/O	3.3V I/O
87	**MEM**	XMDat48	I/O	3.3V I/O
88	**MEM**	XMDat49	I/O	3.3V I/O

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TC6208 Pin Listing (cont'd)

Pin#	Type	Pin Name	I/O	Type
89	**MEM**	XMDat50	I/O	3.3V I/O
90	**MEM**	XMDat51	I/O	3.3V I/O
91	**MEM**	XMDat52	I/O	3.3V I/O
92	**MEM**	XMDat53	I/O	3.3V I/O
93	**MEM**	XMDat54	I/O	3.3V I/O
94	**MEM**	XMDat55	I/O	3.3V I/O
95	**MEM**	XMDat56	I/O	3.3V I/O
96	**VSS**	VSS	-	DGND
97	**VDD**	VDD	-	3.3V
98	**MEM**	XMDat57	I/O	3.3V I/O
99	**MEM**	XMDat58	I/O	3.3V I/O
100	**MEM**	XMDat59	I/O	3.3V I/O
101	**MEM**	XMDat60	I/O	3.3V I/O
102	**MEM**	XMDat61	I/O	3.3V I/O
103	**MEM**	XMDat62	I/O	3.3V I/O
104	**MEM**	XMDat63	I/O	3.3V I/O
105	**MEM**	XMAdr0	O	3.3V Out
106	**MEM**	XMAdr1	O	3.3V Out
107	**VSS**	VSS	-	DGND
108	**MEM**	XMAdr2	O	3.3V Out
109	**MEM**	XMAdr3	O	3.3V Out
110	**MEM**	XMAdr4	O	3.3V Out
111	**MEM**	XMAdr5	O	3.3V Out
112	**MEM**	XMAdr6	O	3.3V Out
113	**MEM**	XMAdr7	O	3.3V Out
114	**VDD**	VDD	-	3.3V
115	**MEM**	XMAdr8	O	3.3V Out
116	**MEM**	XMAdr9	O	3.3V Out
117	**MEM**	XMAdr10	O	3.3V Out
118	**MEM**	XMAdr11	O	3.3V Out
119	**VSS**	VSS	-	DGND
120	**MEM**	XMAdr12	O	3.3V Out
121	**MEM**	XMAdr13	O	3.3V Out
122	**MEM**	XMAdr14	O	3.3V Out
123	**MEM**	XMAdr15	O	3.3V Out
124	**MEM**	MemNGW	O	3.3V Out
125	**MEM**	MemADSC	O	3.3V Out
126	**MEM**	MemNOE	O	3.3V Out
127	**Scan**	MST	I	3.3V In
128	**C&M**	PriRate	I	3.3V In
129	**C&M**	FCOpt	I	3.3V In
130	**VSS**	VSS	-	DGND
131	**VDD**	VDD	-	3.3V
132	**C&M**	TnkP0	I	3.3V In

Pin#	Type	Pin Name	I/O	Type
133	**RMII**	TXEn0	O	3.3V Out
134	**RMII**	XTxDat00	O	3.3 V Out
135	**RMII**	XTxDat01	O	3.3V Out
136	**MII**	XTxDat02	O	3.3 V Out
137	**MII**	XTxDat03	O	3.3V Out
138	**RMII**	Crs_Dv0	I	3.3/5 V In
139	**RMII**	XRxDat00	I	3.3/5 V In
140	**RMII**	XRxDat01	I	3.3/5 V In
141	**N.C.**	NC	-	-
142	**VSS**	VSS	-	DGND
143	**MII**	XRxDat02	I	3.3/5 V In
144	**MII**	XRxDat03	I	3.3/5 V In
145	**RMII**	XTxDat10	O	3.3V Out
146	**RMII**	XTxDat11	O	3.3V Out
147	**VDD**	VDD	-	3.3V
148	**MII**	XTxDat12	O	3.3V Out
149	**MII**	XTxDat13	O	3.3V Out
150	**RMII**	TxEn1	O	3.3V Out
151	**MII**	XRxDat13	I	3.3/5 V In
152	**MII**	XRxDat12	I	3.3/5 V In
153	**RMII**	XRxDat11	I	3.3/5 V In
154	**VSS**	VSS	-	DGND
155	**RMII**	XRxDat10	I	3.3/5 V In
156	**RMII**	Crs_Dv1	I	3.3/5 V In
157	**RMII**	Crs_Dv2	I	3.3/5 V In
158	**RMII**	XRxDat20	I	3.3/5 V In
159	**RMII**	XRxDat21	I	3.3/5 V In
160	**RMII**	TxEn2	O	3.3V Out
161	**RMII**	XTxDat20	O	3.3V Out
162	**RMII**	XTxDat21	O	3.3V Out
163	**RMII**	TxEn3	O	3.3V Out
164	**VSS**	VSS	-	DGND
165	**VDD**	VDD	-	3.3V
166	**RMII**	XTxDat30	O	3.3 V Out
167	**RMII**	XTxDat31	O	3.3 V Out
168	**RMII**	Crs_Dv3	I	3.3/5 V In
169	**RMII**	XRxDat30	I	3.3/5V In
170	**RMII**	XRxDat31	I	3.3/5V In
171	**N.C.**	NC	-	-
172	**Scan**	SDO	O	3.3 V Out
173	**Scan**	SMCK	I	3.3 V In
174	**Scan**	SM	I	3.3V In
175	**RMII**	RefClk	I	3.3/5 V In
176	**VSS**	VSS	-	DGND

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TC6208 Pin Listing (cont'd)

Pin#	Type	Pin Name	I/O	Type
177	**RMII**	Crs_Dv4	I	3.3/5 V In
178	**RMII**	XRxDat40	I	3.3/5 V In
179	**RMII**	XRxDat41	I	3.3/5 V In
180	**RMII**	TxEn4	O	3.3V Out
181	**RMII**	XTxDat40	O	3.3V Out
182	**RMII**	XTxDat41	O	3.3V Out
183	**VDD**	VDD	-	3.3V
184	**RMII**	Crs_Dv5	I	3.3/5 V In
185	**RMII**	XRxDat50	I	3.3/5 V In
186	**RMII**	XRxDat51	I	3.3/5 V In
187	**RMII**	TxEn5	O	3.3V Out
188	**RMII**	XTxDat50	O	3.3V Out
189	**VSS**	VSS	-	DGND
190	**RMII**	XTxDat51	O	3.3V Out
191	**RMII**	XTxDat60	O	3.3V Out
192	**RMII**	XTxDat61	O	3.3V Out
193	**RMII**	TxEn6	O	3.3V Out
194	**RMII**	Crs_Dv6	I	3.3/5 V In
195	**RMII**	XRxDat60	I	3.3/5 V In
196	**RMII**	XRxDat61	I	3.3/5 V In
197	**RMII**	Crs_Dv7	I	3.3/5 V In
198	**RMII**	XrxDat70	I	3.3/5 V In
199	**RMII**	XrxDat71	I	3.3/5 V In
200	**VSS**	VSS	-	DGND
201	**VDD**	VDD	-	3.3V
202	**RMII**	TxEn7	O	3.3V Out
203	**RMII**	XTxDat70	O	3.3V Out
204	**RMII**	XTxDat71	O	3.3V Out
205	**C&M**	HfNFul0	I	3.3 V In
206	**C&M**	HfNFul1	I	3.3 V In
207	**C&M**	HfNFul2	I	3.3 V In
208	**C&M**	HfNFul3	I	3.3 V In

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TC6208 Pin Description

Interface	Signal	I/O	Signal Description
Control/Clock	Reset	I	General reset. Should be valid more than 2*Tclk66. Active HIGH-
Interface	clk66	I	System clock 40 to 66MHz. The switch performance is related to the system clock.
Memory Interface	XMDat(0:63)	I/O	Memory Data Bus.
	XMAdr(0:15)	O	Memory Address Bus.
	MemNGW	O	This output pin is General Synchronous Write Enable signal for Memory.
	MemADSC	O	This output signal provides the Synchronous Address Status Controller for Memory.
	MemNOE	O	This output signal provides the Asynchronous Output Enable for Memory.
Trunking interface	TnkA(0:1) TnkB(0:1)	I	Trunking configuration. • First trunk channel **TnkA1 TnkA0** 0 0 No port is configured as trunk port 0 1 Ports 0 and 1 are configured as external trunk ports 1 0 Ports 0,1,2 and 3 are configured as external trunk ports 1 1 Ports 0 and 1 are configured as internal trunk ports (both for the same trunk) • Second trunk channel **TnkB1 TnkB0** 0 0 No port is configured as trunk port 0 1 Ports 6 and 7 are configured as external trunk ports 1 0 Ports 4,5,6 and 7 are configured as external trunk ports 1 1 Ports 0 and 1 are configured as internal trunk ports (for separate trunks)
	TnkDst	I	Trunk ports balancing for selecting method 1 or 2 '1' - Method 1 based on SA and source port '0' - Method 2 based on SA and DA
	TnkP0	I	When is set Port 0 is configured as internal link port (for the case when we have only one internal trunk line)
Half/Full	HfNFul(0:7)	I	Half/Full signaling. *HnNFul = '1' – **Half*** *HnNFul = '0' – **Full***
FC Bcst Enable	FcBcstEn		Enable Flow Control when Broadcast. '1' - Enable '0' - Disable
Broadcast All	BcstAll	I	Broadcast All '1' - send broadcast packets to all the ports '0' - send broadcast packets just to previously learned ports
Broadcast Excess	ExecBcst	I	Enable/Disable - Broadcast Throttling '1' - Enable '0' - Disable
Back Off Reset	BkRstRx	I	Fair Back Off Algorithm - adjusting of the backoff , using 2 different methods for back pressure algorithm.

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TC6208 Pin Description (cont'd)

Optional Flow Ctrl	FCOpt	I	Flow Control resolution : '1' - the A-NEG result is considered '0' - doesn't matter the A-NEG result
MDIO Interface	MDIO	I/O	MDIO BUS.
	MDClk	I	MDIO clock.
Test	Test	I	Test pin. *Test='1' – **test mode*** *Test='0' – **normal operation***
Speed Detect	SpDet	I	Indicate if speed is auto detected. '1' - Speed Detect '0' - Auto Negotiation
EEPROM Interface	SDA	I/O	Serial Data
	SCL	O	. Serial Clock.
Priority Ports	PP(0:1)	I	Indicates which ports, if any, are prioritized; when selected the ports will have normal ,high or very high priority rate depending of the state of PriRate pin. **PP0** **PP1** **Port priority scheme** 0 0 No port is configured as a prioritized port 0 1 Port 7 is configured as a prioritized port 1 0 Ports 6 and 7 are configured as prioritized ports 1 1 Ports 5, 6 and 7 are configured as prioritized ports
Priority Rate	PriRate	I	Priority Rate, '0' - the selected priority ports will have a high priority; '1' - the selected priority ports will have a very high priority rate.
Scan Pins These pins are used just by the chip vendor for circuit testing. In a normal operation they must have the specified values.	MST	I	Scan Mode - for normal operation must be tied **Low**.
	SMCK	I	Scan Clock - for normal operation must be tied **High**.
	SM	I	Internal RAM Scan Mode - for normal operation must be tied **High**
	SDO	O	Internal Scan Data Out - it is not used in normal operation . Must be left **open**.

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TC6208 Pin Description (cont'd)

RMII Interface Port0	XTxDat0(0:1)	O	RMII Tx Data. / MII Tx Data (0:1)*
	XTxDat0(2:3)	O	MII Tx Data (2:3).
	TxEn0	O	RMII Tx Enable.
	Crs_Dv0	I	RMII Carrier Sense / Receive Data Valid.
	XRxDat0(0:1)	I	RMII Rx Data. / MII Rx Data (0:1)**
	XRxDat0(2:3)	I	MII Rx Data (2:3).
RMII Interface Port1	XTxDat1(0:1)	O	RMII Tx Data / MII Tx Data (0:1)*
	XTxDat1(2:3)	O	MII Tx Data (2:3) .
	TxEn1	O	RMII Tx Enable
	Crs_Dv1	I	RMII Carrier Sense / Receive Data Valid
	XRxDat1(0:1)	I	RMII Rx Data / MII Rx Data (0:1)**
	XRxDat1(2:3)	I	MII Rx Data (2:3).
RMII Interface Port2	XTxDat2(0:1)	O	RMII Tx Data
	TxEn2	O	RMII Tx Enable
	Crs_Dv2	I	RMII Carrier Sense / Receive Data Valid
	XRxDat2(0:1)	I	RMII Rx Data
RMII Interface Port3	XTxDat3(0:1)	O	RMII Tx Data
	TxEn3	O	RMII Tx Enable
	Crs_Dv3	I	RMII Carrier Sense / Receive Data Valid
	XRxDat3(0:1)	I	RMII Rx Data
RMII Interface Port4	XTxDat4(0:1)	O	RMII Tx Data
	TxEn4	O	RMII Tx Enable
	Crs_Dv4	I	RMII Carrier Sense / Receive Data Valid
	XRxDat4(0:1)	I	RMII Rx Data
RMII Interface Port5	XTxDat5(0:1)	O	RMII Tx Data
	TxEn5	O	RMII Tx Enable
	Crs_Dv5	I	RMII Carrier Sense / Receive Data Valid
	XRxDat5(0:1)	I	RMII Rx Data
RMII Interface Port6	XTxDat6(0:1)	O	RMII Tx Data
	TxEn6	O	RMII Tx Enable
	Crs_Dv6	I	RMII Carrier Sense / Receive Data Valid
	XRxDat6(0:1)	I	RMII Rx Data
RMII Interface Port7	XTxDat7(0:1)	O	RMII Tx Data
	TxEn7	O	RMII Tx Enable
	Crs_Dv7	I	RMII Carrier Sense / Receive Data Valid
	XRxDat7(0:1)	I	RMII Rx Data
RMII Reference Clock	Refck	I	RMII Reference Clock for Port 0-7

* Used for **MII Tx Data (0:1)** when ports 0 and 1 are configured as internal trunk ports.
** Used for **MII Rx Data (0:1)** when ports 0 and 1 are configured as internal trunk ports.

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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

Ethernet Media Access Controller

Transmit MAC

There are 8 independent transmit MAC's for each port with 8 independent transmit FIFO's.

The transmit Media Access Controller (MAC) section generates an Ethernet MAC frame **(IEEE 802.3)** from transmit FIFO data, generates preamble and start frame delimiter, and maintain a standard inter-frame gap time during transmit.

TC6208 automatically determine if the port is in half duplex.

The MAC works in 10/100, half/full-duplex, with or without flow-control depending of the state of the transmission. In half duplex mode the transmit MAC meets CSMA/CD **IEEE 802.3** requirements: it will retransmit if collisions occur during the first 64 bytes (early collisions) or it will discard the packet if collisions occur after 64 bytes (late collisions). It also follows the truncated binary exponential backoff algorithm, collision and jamming procedures.

The transmit MAC appends the standard preamble and start frame delimiter to the every packet from FIFO.

The MAC also follows as default the standard InterFrame Gap. The default IFG is 96 bit time.

The transmit FIFO acts as a temporary buffer between the transmit MAC section and core switch interface. The FIFO logic manages the retransmission for early collision conditions or discards the frames for late collision or underflow. The transmit FIFO underflow condition occurs when FIFO is empty and transmit MAC is in the middle of a packet transmission.

TheTC6208 in the full-duplex mode uses the flow-control algorithm specified in **IEEE 802.3x** .

MAC Pause frames are used primarily for flow control packets, which pass signaling information between stations. MAC Pause frame have a unique type **8808H,** Pause op code **0001H**. The MAC Pause frame contains in the data field a Pause Value. The flow-control manager will auto-adapt the procedure based on traffic volume and speed to avoid losing packets and unnecessary pause periods.

TheTC6208 in the half-duplex mode will start back-pressure algorithm. The back-pressure algorithm based on a false carrier sense (forced collision) and an aggressive backoff algorithm. The forced collisions generated in these conditions are limited to a maximum of 7 consecutive collisions.

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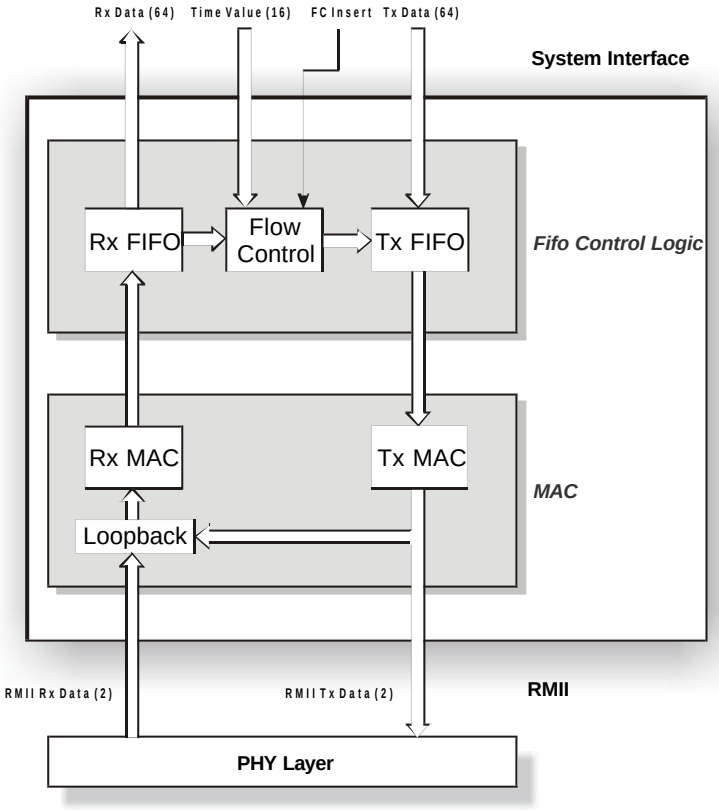
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING



MAC Block Diagram

Receive MAC

When **a frame** is received from the Ethernet media through **the RMII**, the data is **stored** in a receive FIFO. The **receive FIFO** work as a temporary buffer between the receive MAC section and switch interface.

The **receive MAC** sublayer decomposes Ethernet packets acquired from the PHY layer via RMII, by stripping off the preamble sequence and SFD, checking the CRC, checking for MAC Control frames and checking frame validity against the drop conditions . The receive MAC then sends the valid packets to the receive FIFO.

The receive MAC determines the validity of each received packet by checking for valid Type, CRC and oversize or undersize packet conditions. The bad packets will be dropped either by the MAC or by the switch.

Oversized packets are truncated at 1536 bytes and marked to be erroneous.

Undersized packets are packets whose length is less than the minimum packet size. This size is defined to be 64 bytes, exclusive of preamble sequence and SFD. If the received packet is an undersize packet, then the frame is determined to be invalid and it is removed from Rx FIFO. The space in the receive FIFO will be recovered.

The CRC and length/type field of frame is checked to detect whether the packet is a valid **MAC Control** frame.

When theTC6208 receives a MAC control frame and determines that the op code is a pause command (**Flow Control** frame) and the CRC of the frame is OK, the chip will load its internal pause counter with the Number_of_Slots variable from the MAC control packet just received. Anytime the

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XReceive_Pause_Counter is zero the Transmit MAC will XON. If the XReceive_Pause_Counter is not zero the Receive MAC will XOFF the Transmit MAC. The transmit MAC when detect an XOFF condition will continue transmitting the current packet but will stop transmission until receiving XON condition from the receive MAC.

If a frame transmission is in progress when the Flow Control packet is received, the transmission is allowed to complete. The pause time will begin at the end of current transmission or immediately (if no transmission). If a pause command is received while the transmitter is already in pause, the new pause time indicated by the new Flow Control packet will be loaded into the pause register.

When the receive FIFO is full and additional data are still incoming from the MAC, then the **Overrun** conditions occurs and the frame is dropped. This situation continues until the system read from FIFO.

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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

Broadcast

TC6208 has some unique features in supporting the broadcast.

When TC6208 is configured in BroacastAll mode(default) all the packets will be sent to all ports.

When TC6208 is not configured in BroacastAll mode the broadcast packets will be sent only to ports which have activity. The activity is being learned for each port and also activity indication will be purged if no activity is detected for typical 10 minutes. This feature will eliminate the broadcast on ports unconnected or dead.

In case of broadcast storm the broadcast traffic will be throttled. This option refers just to multicast packets and can be Enabled or Disabled using the pin ExecBcst or using the EEPROM General Configuration Register, bit EnBcstDrop. If TC6208 receives more than 16 consecutive broadcast packets some packets will be discarded. Setting the BcstDropReg (3 bits) TC6208 can adjust the number of discarded packets between 8 to 15 at 16 Broadcast packets. This means that the percent of discarded packets can vary between 50% and 93%. The default value is 50%.

On the same timeTC6208 is capable of taking continuos broadcast packets from one port and deliver them to all ports at maximum speed without losing or fragmenting packets. This is a feature needed for video application to broadcast video to customers from one video server.

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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

Priority

TC6208 support port priority and QoS (802.1p, VLAN priority header, IP header).

Continuous priority traffic to a destination port will take precedence against normal continuos traffic to the same destination port. The normal continuous traffic is guaranteed to arrive to a given destination even if continuous priority traffic is designated to the same port when the senders are flow-control capable.

Priority rules apply for ports in any speed mode and duplex mode.

The priority traffic in TC6208 is individually flow-controlled.

For continuos traffic which come from senders which are not flow-control capable some of the packets may be lost if the destination port has priority traffic to transmit from other ports.

The 802.1p, VLAN Priority Header is always checked in TC6208 and IP header will be checked when "Layer 3 En" (General Configuration Register) bit set.

The port priority is suitable for video application for networks which does not support VLAN or priority traffic. It' s a unique feature of TC6208.

Packets from priority ports will arrive at the destination port earlier than packets arrived from normal ports.

The port no. 5,6,7 of TC6208 can be configured as priority port (high or very high priority depending of the state of PriRate pin) when is using pin configuration or any port when is using EEPROM configuration. Any traffic from this port will be switched to destination with precedence against any traffic arrived from the other ports.

In Multimedia application, the audio & voice message is time critical to users. Normally it might have discontinue phenomenon through the Ethernet network, especially if the network segment utilization more than 30%, the message can not reach users in time. TC6208 provides the "QoS" compatibility, it means, TC6208 will forward the coming packets with precedence which have priority setup in their IP header or in their VLAN priority header (802.1p). More on this, TC6208 also provides a unique and convenient feature for users to speed up their specific application (Video Conference, for example) in their high traffic environment. This feature we call it "Port Priority" .You can set a port(s) to be "Priority Port" by jumper or by EEPROM, and TC6208 will forward all the coming packets with precedence to their destination port, no matter with these packets from this priority port have the priority setup or not.

TC6208 has 2 queues for each port: One for regular traffic, another for priority traffic. The packets coming from the port(s) with priority setup (QoS), OR packets which does have priority (higher than ZERO) setup in their IP header , OR packets which does have priority setup in their VLAN priority header (QoS) will go to the priority queue of the destination port. The packets from priority queue will be extracted with precedence than the one from regular queue. There are two precedence levels (high or very high) and can be setup by jumper or by EEPROM. TC6208 serve these two queues (regular & priority) in a fairly manner.

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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

Trunk Configuration

TheTC6208 has the ability to configure some of its ports as trunking ports.

Using the pin configuration *TnkA0 , TnkA1 , TnkB0 ,TnkB1* or using EEPROM configuration ports on the switch may be configured for trunking, allowing the user to interconnect a switch implemented with theTC6208 with any switch that supports trunking, or to economically expand the number of ports for a switch.

The ports can be trunked internally on MII interface bypassing the PHY' s or externally with 100BaseT cables (to link 2 or more switches). The TC6208 support 2 or 4 ports trunking based on the state of input *TnkA0 , TnkA1 , TnkB0 ,TnkB1* or using EEPROM configuration

The traffic on the ports of the same trunk will be automatically balanced.

TC6208 does use 2 methods for balancing scheme, (Pin or EEPROM selectable):

Method 1. based on SA and source port (default).
Method 2. based on SA and DA.

Station connected on the same port may not send traffic on the same trunk line. The packet order is guaranteed for method 1 for unicast and broadcast packets. The packet order is guaranteed for method 2 only for unicast packets. Switches interconnected through trunk ports can be cascaded. For ex. Switch A connected by a trunk with Switch B and Switch B connected by another trunk by switch C. All stations connected on switch A, B, C can communicate with each other as local to the switch.

The default mode for all trunking ports is 100 M full-duplex. It is recommended that all trunking ports to be configured with the same speed. The half-duplex ports do not trunk. If the user select a trunk configuration it must make sure that all ports are connected within the trunk, the port order is not mandatory. If one wire from a defined trunk is not connected the trunk may not work properly.

Another way to expand the number of ports for a switch is using *internal link* mode .*The port(s)* can be configured as internal link port(s) using pin configuration TnkB0 ,TnkB1 or TnkP0 or EEPROM configuration .This Tnkp0 mode is similarly with internal trunk but is using a single port .

Multiple switches can be cascaded by trunking or internal link.

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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

Flow Control

TC6208 has the ability to generate Flow Control Packets.

When FCOpt = '1' (the pin or bit from MACConfigReg) TC6208 set the Flow Control ability according to auto-negotiation (bit 10 from the PHY's Link Partner register) result. If FCOpt = '0', the Flow Control settings doesn't care about the auto-negotiation result.

Without using an EEPROM , when configuration pin FCOpt is '1' the Flow Control is set according to auto-negotiation (bit 10 from the PHY's Link Partner register). When FCOpt is '0' the Flow Control is Enabled regardless the auto-negotiation result.

Using an EEPROM, when FCOpt is '1' the Flow Control ability setting is based on FCPort (bit 5 - DsFulDplxFC- from Port 0..7 Configuration Register) and also on auto-negotiation (bit 10 from the PHY's Link Partner register). If FCOpt is '0' TC6208 doesn't care about auto-negotiation and send Flow Control packets according to FCPort bit.

Without EEPROM

FCOpt (Pin)	A-NEG(Nway) (bit 10 from the PHY's Link Partner Register)	FC - Ability (per port base)
0	Don't care	Enabled
1	Disabled	Disabled
	Enabled	Enabled

With EEPROM

FCOpt	FCPort X (EEPROM)	A-NEG(Nway) (bit 10 from the PHY's Link Partner Register)	FC - Ability (per port base)
0	1	Don't care	Disabled
	0		Enabled
1	1	Don't care	Disabled
	0	Disabled	Disabled
		Enabled	Enabled

Flow Control default enable EEPROM overwrite Nway results.

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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

Auto Negotiation

TC6208 has 2 modes for speed and mode settings : Speed Detect and Auto-Negotiation.

In Speed Detect Mode TC6208 can adjust a port speed after at least one packet is received on that port. The Port mode (Half or Full Duplex) is forced using the external configuration pins (HfNFul0-7) or an external EEPROM.

In Auto-Negotiation Mode TC6208 is polling the PHY's Advertisement Registers, using the MDIO line, and force the ports according to this settings. In this way TC6208 can follow any line changes of speed or mode.

Using an EEPROM , ports settings can be forced in 10/100 MHz or Half/Full Duplex. In this case TC6208 writes the Advertisement Register of the PHY's and starts an auto-negotiation.

Also the TC6208 writes bit 10 from PHY's Advertisement Register, according to Flow Control ability settings and starts PHY's auto-negotiation to inform the link partner about flow control ability.

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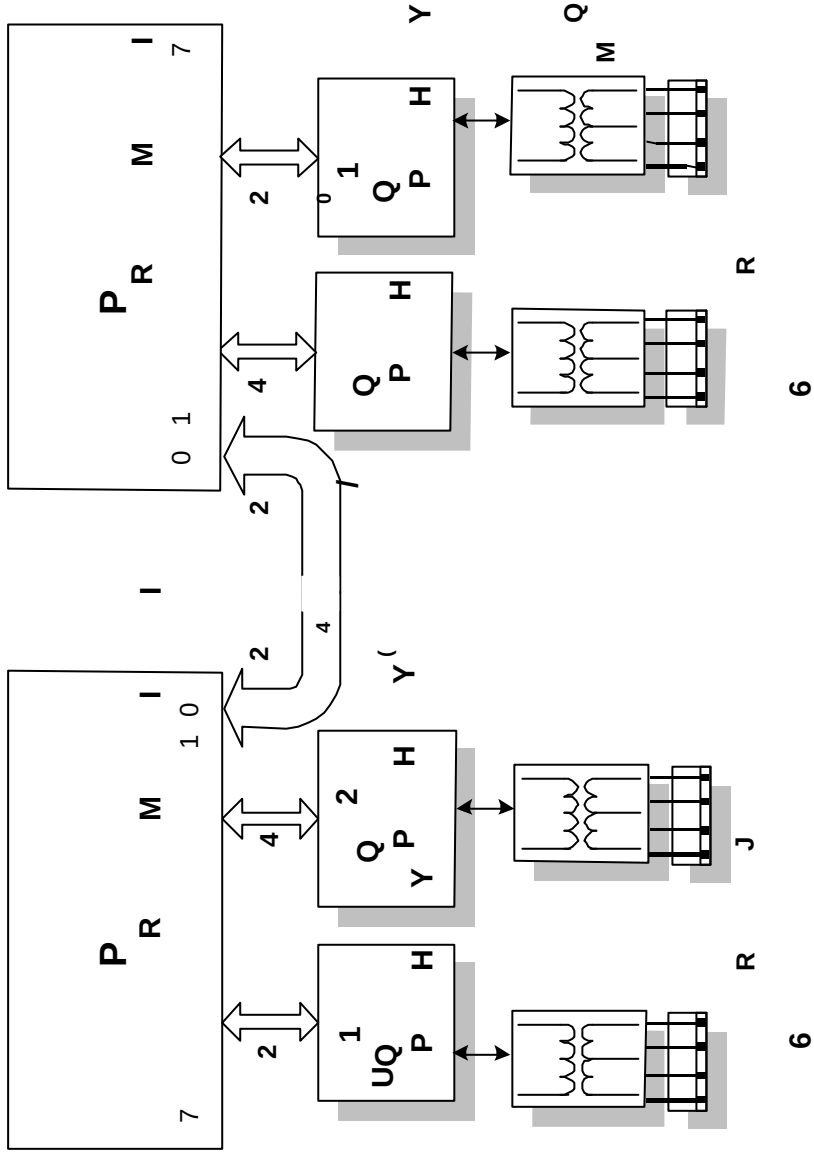
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING



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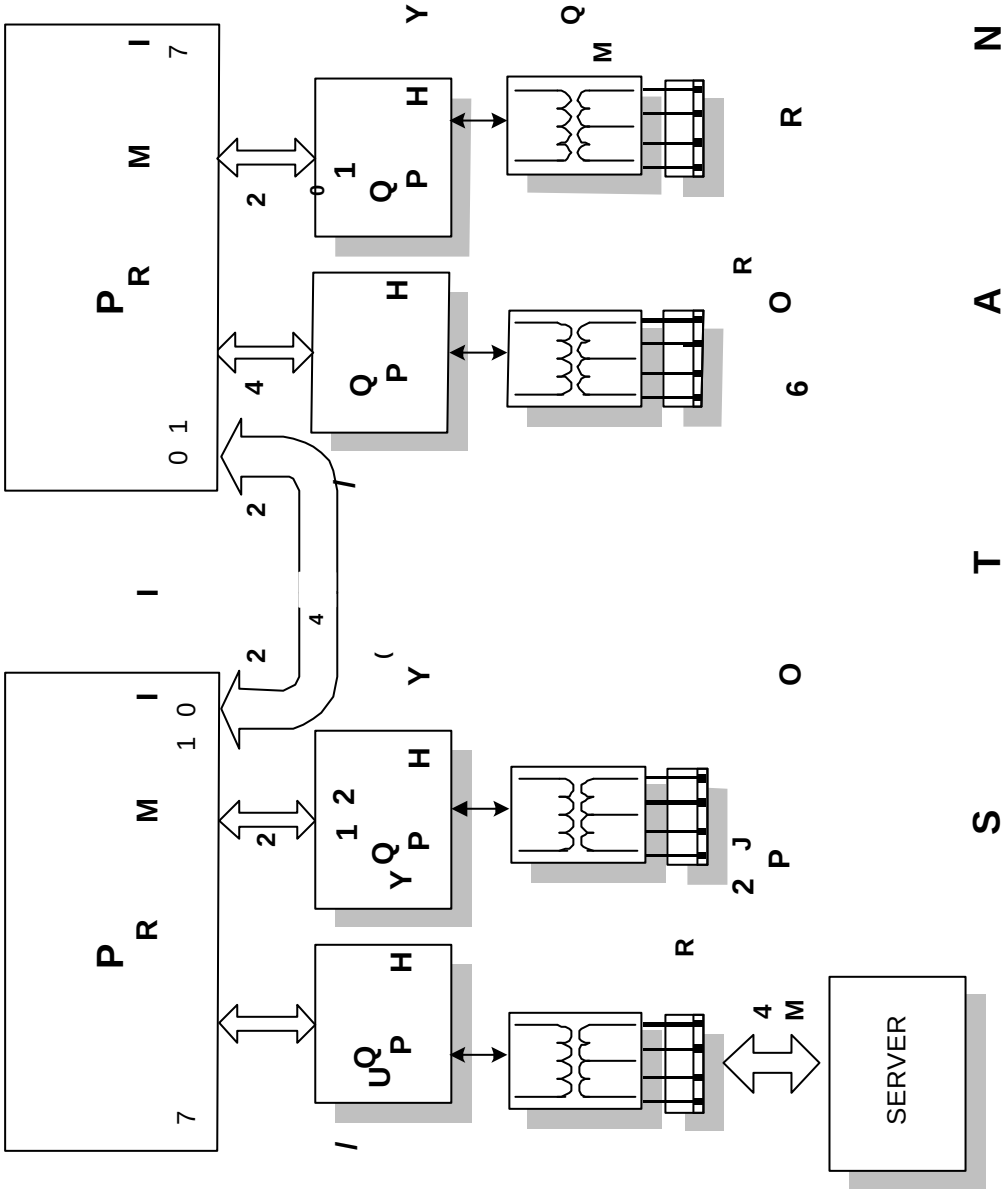

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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

EEPROM Interface

The TC6208 uses 24C02 serial EEPROM device (2048 bits organized as 256 bytes x 8)

The EEPROM interface is provided so the manufacturer can provide a pre-configured system to their customers. Customers can change or reconfigure their system and retain their preferences.

The EEPROM contains configuration information, which is accessed at power up and reset.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence ,the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8 bit words . The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C02A features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then create a start condition as SDA is high.

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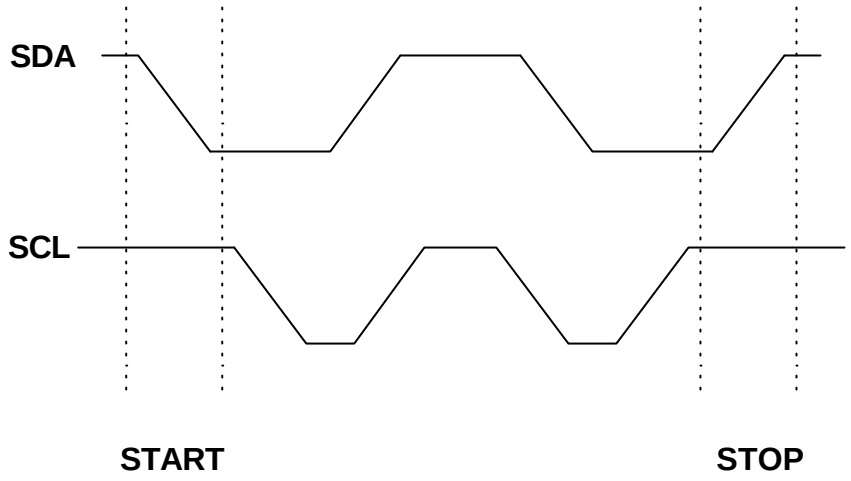
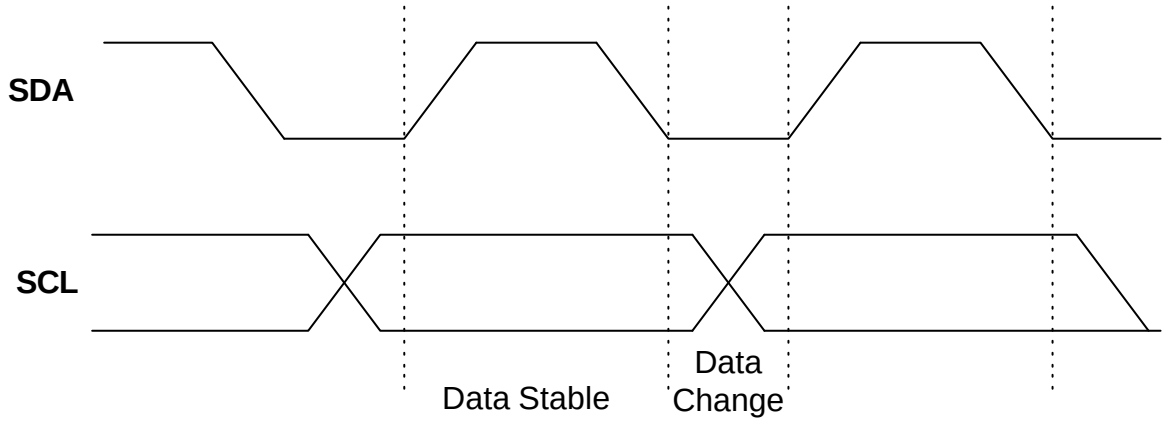
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

- *Start and Stop Timing Diagram*



- *Data Validity Timing Diagram*



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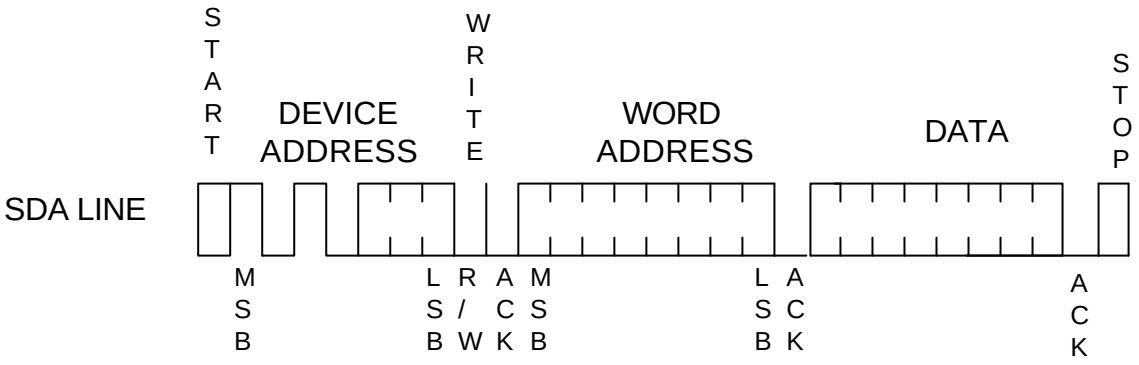
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

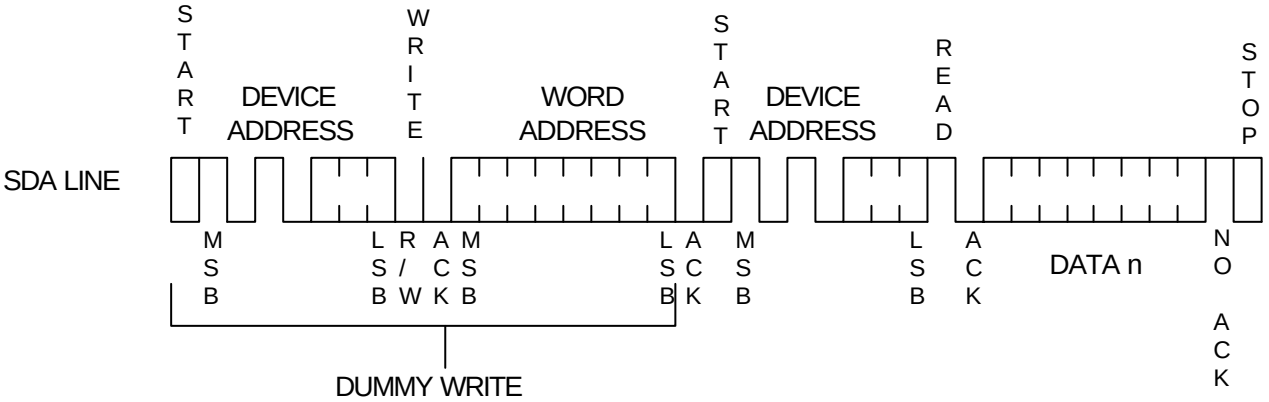
TYPICAL WRITE OPERATION (BYTE WRITE)

A write operation requires an 8 bit data word address following the device address word and acknowledgement. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8 bit data word. Following receipt of the 8 bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete.



TYPICAL READ OPERATION (RANDOM READ)

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition .



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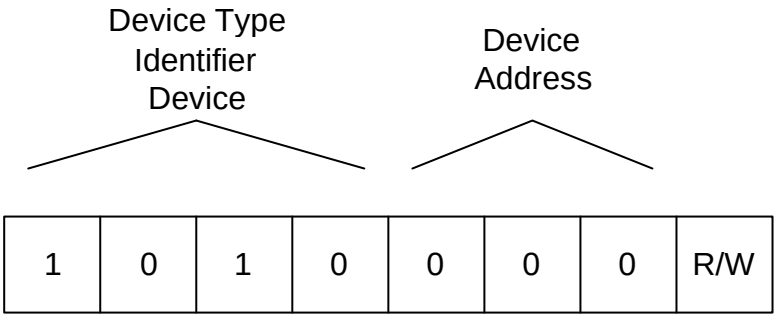
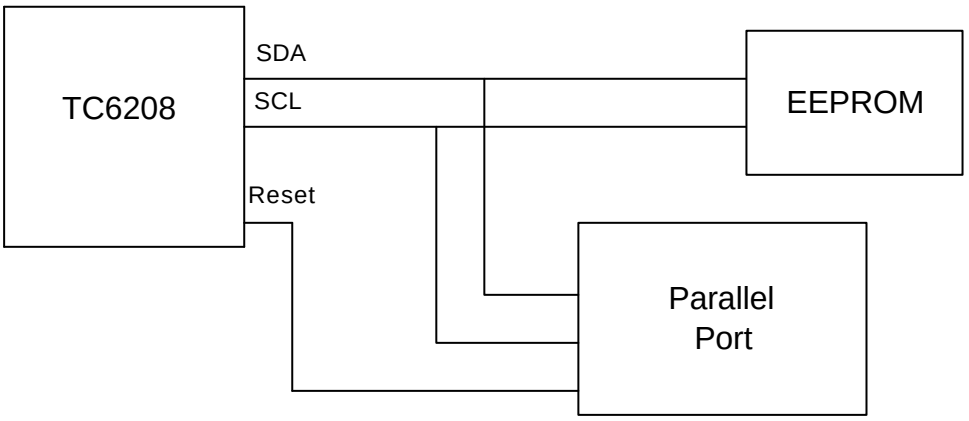
DEVICE ADDRESS



Reprogramming the EEPROM for reconfiguration

If the RESET pin is held high the TC6208 ' s EEPROM interface will go into high impedance state .This feature is very useful for reprogramming the EEPROM during installation or reconfiguration.

The EEPROM can be reprogrammed by an external parallel port . For reprogramming using a parallel port a signal is used to hold the RESET pin high; the EEPROM interface will then be in the high impedance state. Once the pins are in high impedance state the EEPROM can now be programmed by the parallel port trough the SDA and SCL pins.



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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

EEPROM Address Map

EEPROM

Physical Address	Bits	TC6208 Register [Bits]	Validate by	DESCRIPTION
00	[7:0]	ValidReg [15 downto 7]	-	Validate Registers
01	[7:0]	ValidReg [7 downto 0]	-	Validate Registers
02	[7:0]	FCPauseVal [15 downto 8]	ValidReg [0]	Flow Control Pause Value
03	[7:0]	FCPauseVal [7 downto 0]	ValidReg [0]	Flow Control Pause Value
04	[7:0]	ConfigRegP0 [7 downto 0]	ValidReg [1]	Port 0 Configuration Register
05	[7:0]	ConfigRegP1 [7 downto 0]	ValidReg [2]	Port 1 Configuration Register
06	[7:0]	ConfigRegP2 [7 downto 0]	ValidReg [3]	Port 2 Configuration Register
07	[7:0]	ConfigRegP3 [7 downto 0]	ValidReg [4]	Port 3 Configuration Register
08	[7:0]	ConfigRegP4 [7 downto 0]	ValidReg [5]	Port 4 Configuration Register
09	[7:0]	ConfigRegP5 [7 downto 0]	ValidReg [6]	Port 5 Configuration Register
0A	[7:0]	ConfigRegP6 [7 downto 0]	ValidReg [7]	Port 6 Configuration Register
0B	[7:0]	ConfigRegP7 [7 downto 0]	ValidReg [8]	Port 7 Configuration Register
0C	[7:0]	MACCfgReg [15 downto 8]	ValidReg [9]	MAC Configuration Register
0D	[7:0]	MACCfgReg [7 downto 0]	ValidReg [9]	MAC Configuration Register
0E	[7:0]	TrunkCfgReg [7 downto 0]	ValidReg [10]	Trunk Configuration Register
0F	[7:0]	GenCfgReg [7 downto 0]	ValidReg [11]	General Configuration Register

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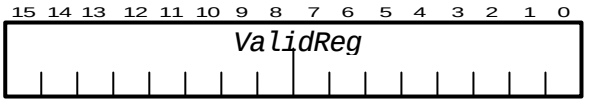
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

Register Description

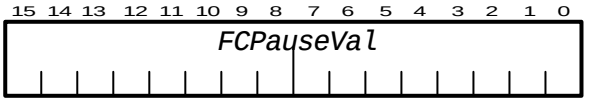
Validate Register



Bit(s)	Field	Description
15 –12	Not Used	
11 – 0	ValidReg	Validate Register

- **ValidReg [0]** – when is set validate **FCPauseVal** register
- **ValidReg [1]** – when is set validate **ConfigRegP0** register (jumper less mode)
- **ValidReg [2]** – when is set validate **ConfigRegP1** register (jumper less mode)
- **ValidReg [3]** – when is set validate **ConfigRegP2** register (jumper less mode)
- **ValidReg [4]** – when is set validate **ConfigRegP3** register (jumper less mode)
- **ValidReg [5]** – when is set validate **ConfigRegP4** register (jumper less mode)
- **ValidReg [6]** – when is set validate **ConfigRegP5** register (jumper less mode)
- **ValidReg [7]** – when is set validate **ConfigRegP6** register (jumper less mode)
- **ValidReg [8]** – when is set validate **ConfigRegP7** register (jumper less mode)
- **ValidReg [9]** – when is set validate **MACCfgReg** (jumper less mode)
- **ValidReg [10]** – when is set validate **TrunkCfgReg** (jumper less mode)
- **ValidReg [11]** – when is set validate **GenCfgReg** (jumper less mode)

Flow Control Pause Value



Bit(s)	Field	Description
15 – 0	FCPauseVal	Time value to insert into a Flow Control packet

- **FCPauseVal** – 16-bits data used by every port to compute the delay of a FC packet in Full Duplex mode.
  - default ‘ 0000011000000000’ = 1536

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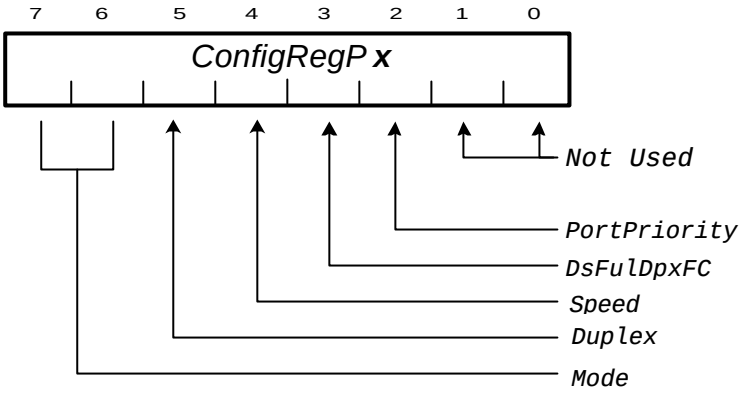
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

Port *x* Configuration Register



Bit(s)	Field	Description
7 – 6	*Mode*	Select source
5	*Duplex*	Full / NOT Half Duplex Configuration
4	*Speed*	100 Mb / 10Mb Configuration
3	*DsFulDpxFC*	Disable Full Duplex Flow Control
2	*PortPriority*	Port Priority
1 – 0	Not Used	

Mode		Duplex	Speed
0	0	Pin Configuration	Auto Detect
0	1	Auto - Negotiation	Auto - Negotiation
1	0	EEPROM configuration	EEPROM configuration
1	1	Auto - Negotiation	Auto Detect

- **Duplex** – When is asserted high set port ***X*** in Full Duplex mode (if **mode = "**10**")**.
  – When is asserted low set port ***X*** in Half Duplex mode (if **mode = "**10**")**.
- **Speed** – When is asserted high set port ***X*** in 100Mb mode (if **mode = "**10**")**.
  – When is asserted low set port ***X*** in 10Mb mode (if **mode = "**10**")**.

- **DsFulDpxFC** – Setting this bit to 1 disable transmit Full Duplex Flow Control Packet on port ***X***.
- **PortPri** – When is set force port ***X*** in Priority Mode.

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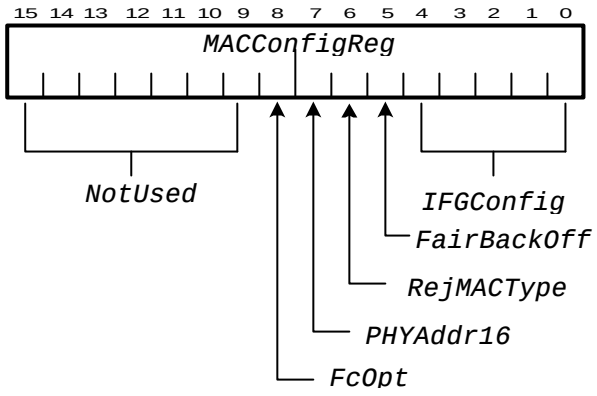
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

MAC Configuration Register



Bit(s)	Field	Description
14 – 9	*Not Used*	
8	*FcOpt*	Optional Flow Control
7	*PHYAddr16*	MDIO PHY Address 16 to 23
6	*RejMACType*	Reject MAC Type
5	*FairBackOff*	Fair Backoff Algorithm
4 – 0	*IFGConfig*	Interframe Gap Configuration

- **FCOpt** – Flow Control resolution. If is set the result of A-NEG is considered otherwise doesn't care.
- **PHYAddr16** – Setting this bit to ‘1’ will program the MDIO PHY address to addresses 16 to 23. - default ‘0’
- **RejMACType** – When is set RXMAC eliminate all MAC Type packets. - delault '0'
- **FaireBkOfff** – Indicate Back Off Mode.
- **IFGConfig** – These bits control the inter gap length. - default ‘ 10101’ = 21

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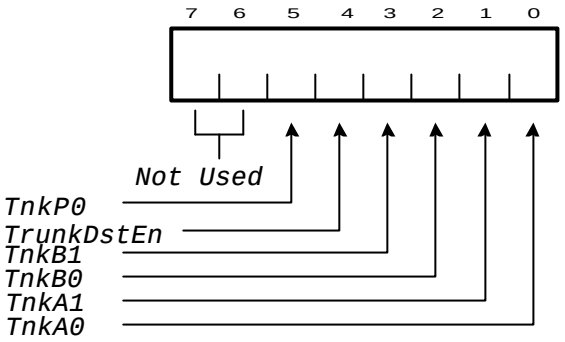
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

TrunkCfgReg



TnkA1	TnkA0	Ports	Type
0	0	No Trunk	-
0	1	Trunk on ports 0 ,1	External
1	0	Trunk on ports 0,1,2,3	External
1	1	Trunk on ports 0 ,1	Internal
TnkB1	**TnkB0**	**Ports**	**Type**
0	0	No Trunk	-
0	1	Trunk on ports 6 ,7	External
1	0	Trunk on ports 4,5,6,7	External
1	1	Trunk on ports 0 ,1	Internal*

* for separate trunks

- **TrunkDstEn** – When is set TC6208 use SA and source port method for balancing scheme.
  – When is not asserted TC6208 use DA method for balancing scheme.
- **TnkP0** – When is asserted Port 0 is configured as *internal link*.

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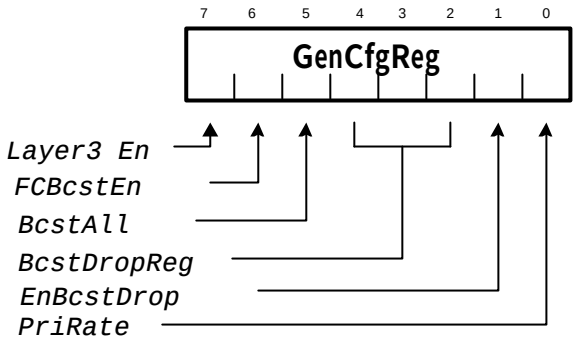
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

General Configuration Register



Bit(s)	Field	Description
7	*Layer3En*	Enable IP header priority, bits checked.
6	*FCBcstEn*	Flow Control Broadcast Enable
5	*BcstAll*	Broadcast All
4-2	*BcstDropReg*	Broadcast Drop Register
1	*EnBcstDrop*	Enable Broadcast Drop
0	*PriRate*	Priority Rate

- **Layer3En** – When is set Enable check IP priority.
- **FCBcstEn** – When is set Enable Flow Control when broadcast packets.
- **BcstAll** – When is set all the packets will be sent to all ports.
- **EnBcstDrop** – When is set the broadcast traffic will be throttled.
- **PriRate** – When is set the selected priority ports will have a very high priority rate.
  – When is not asserted the selected priority ports will have a high priority rate.
- **BcstDropReg** – When is set **EnBcstDrop** will be dropped (8+**BcstDropReg**) packets.
  – Default "000"

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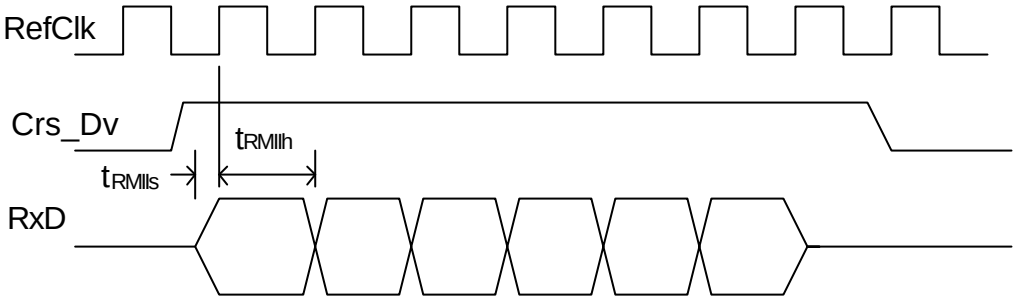
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

TIMING REQUIREMENT

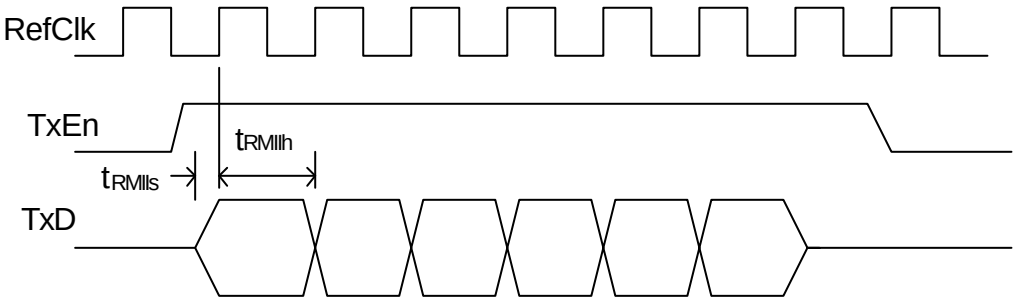
- RMII Receive Timing

Name	Signal	Min.	Typ.	MAX	Unit
T_{RMIIs}	Crs_Dv,RxD	4	-	-	ns
T_{RMIIh}	Crs_Dv,RxD	2	-	-	ns



- RMII Transmit Timing

Name	Signal	Min.	Typ.	MAX	Unit
T_{RMIIs}	TxEn,TxD	4	-	-	ns
T_{RMIIh}	TxEn,TxD	2	-	-	ns



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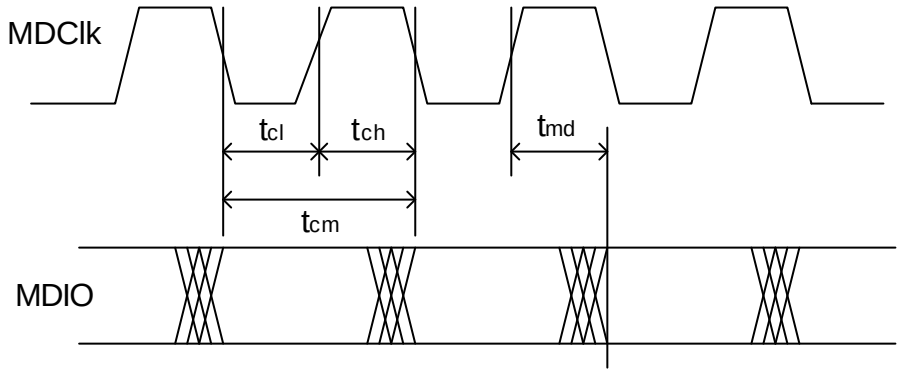
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

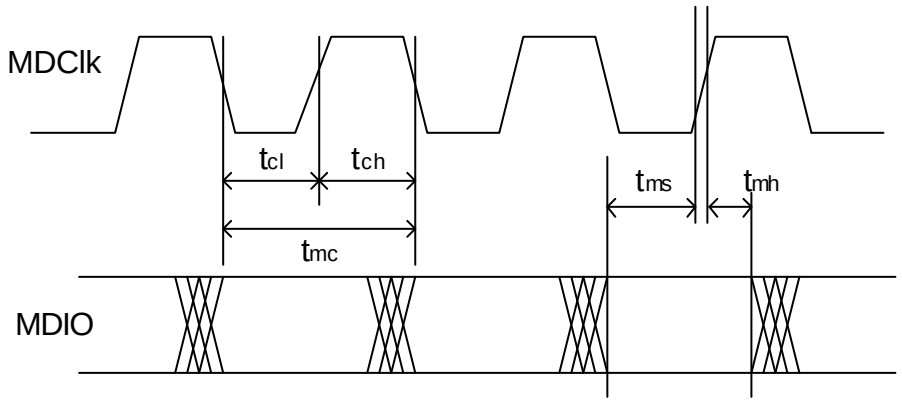
- PHY Management (MDIO) Read Timing

Name	Signal	Min.	Typ.	MAX	Unit
t_{ch}	MDCK High Time	180	200	220	ns
t_{cl}	MDCK Low Time	180	200	220	ns
t_{cm}	MDCK period	-	400	-	ns
t_{md}	MDIO output delay		10	300	ns



- PHY management Write Timing

Name	Signal	Min.	Typ.	MAX	Unit
t_{ch}	MDCK High Time	180	200	220	ns
t_{cl}	MDCK Low Time	180	200	220	ns
t_{mc}	MDCK period	-	400	-	ns
t_{ms}	MDIO setup time	10			ns
t_{mh}	MDIO hold time	10			ns



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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

ELECTRICAL SPECIFICATIONS

1. ABSOLUTE MAXIMUM RATINGS

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in Recommended Operating Conditions. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage (External) (Internal)	V_{DDE} V_{DDI}	V_{SS}*1 – 0.5 V_{SS}*1 – 0.5	6.0 6.0	V
Input Voltage	V_I	V_{SS}*1 – 0.5	V_{DD}+0.5	V
Output Voltage	V_O	V_{SS}*1 – 0.5	V_{DD}+0.5	V
Storage Temperature	T_{ST}	Plastic -55 Ceramic -65	+125 +150	°C
Junction Temperature	T_j	Plastic -40	+125	°C
Supply Pin Current	I_D	For one V_{DD} pin For one V_{SS} pin	60 60	mA
Output Current	I_O	Power type I_{OL}=8mA	±14	mA
Overshoot Undershoot		V_{DD} + 1.0 *2 V_{SS} – 1.0 *2		

Note: *1 Vss = 0V
*2 For 50 ns. Max.
Note: The maximum ratings are the limit value that must never be exceeded even for an instant.

2. OPERATING CONDITIONS

The recommended operating conditions are the recommended values for assuring normal logic operation. As long as the device is used within the recommended operating conditions, the electrical characteristics (DC and AC characteristics) described below are assured.

PARAMETER			SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage			V_{DD}	3.0	3.3	3.6	V
High-level input voltage	3V interface CMOS	Standard Schmidt	V_{IH}	V_{DD}x0.65 V_{DD}x0.80		V_{DD}+0.3	V
	5V tolerant	Standard Schmidt		V_{DD}x0.65 V_{DD}x0.80		5.25	
Low-level input voltage	3V/5V CMOS	Standard Schmidt	V_{IL}	V_{SS}* V_{SS}*		V_{DD}x0.25 V_{DD}x0.20	V
Junction Temperature			T_j	-40		125	°C

Note: * V_{SS}=0V.

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8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

3. DC CHARACTERISTICS (VDD=3.3V ± 0.3V : Standard Specifications)

(Measuring Condition V_{DD}=3.3 V ± 0.3 V, V_{SS}=0V, T_j=-40 to 125 °C)

PARAMETER	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Supply Current	I_{DSS}	Standby mode*1	P1 to PC			2.0	mA
			PD to PF			4.0	
High-level output voltage	V_{OH}	I_{OH}=-8 mA		V_{DD}-0.5		V_{DD}	V
Low-level output voltage	V_{OL}	I_{OL}= 8 mA		V_{SS}		0.4	V
Input Leakage Current *2 (Tri state Pin: Input)	I_{LI}	V_I=0V-V_{DD}		-5		5	µA
	I_{LZ}			-5		5	
Output short circuit current *3	I_{OS}	3.3 V output pin V_O=0V or V_{DDE}		I_{OL}=8mA	-120	+120	mA

Note: *1 V_{IH}=V_{DD} and V_{IL}=V_{SS} , the memory is in the standby mode.
*2 If an input buffer with pull-up/pull-down resistance is used, the input leakage current may exceed the above value.
*3 Maximum supply current at the short circuit of output and V_{DD} or V_{SS}, for 1 second per LSI pin.

4. CAPACITANCE

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Pin Capacitance	C_{IN}	-	-	16	pF
Output Pin Capacitance	C_{OUT}*	-	-	16	
I/O Pin Capacitance	C_{IO}*	-	-	16	

Measuring conditions : T_j=25 °C
V_{DD}=V_I=0V, f=1MHz.

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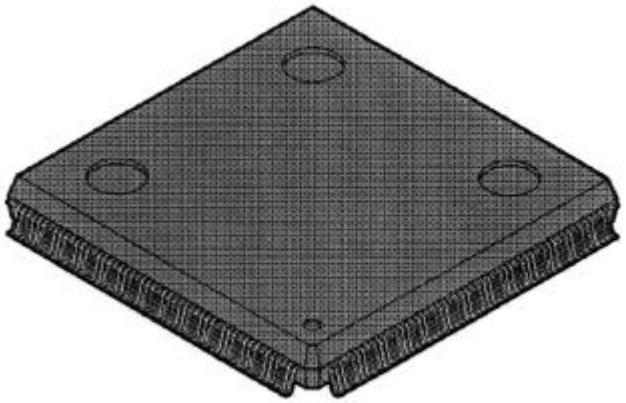
8 PORT 10/100 UNMANAGED ETHERNET SWITCH WITH FLOW-CONTROL, PRIORITY, TRUNKING

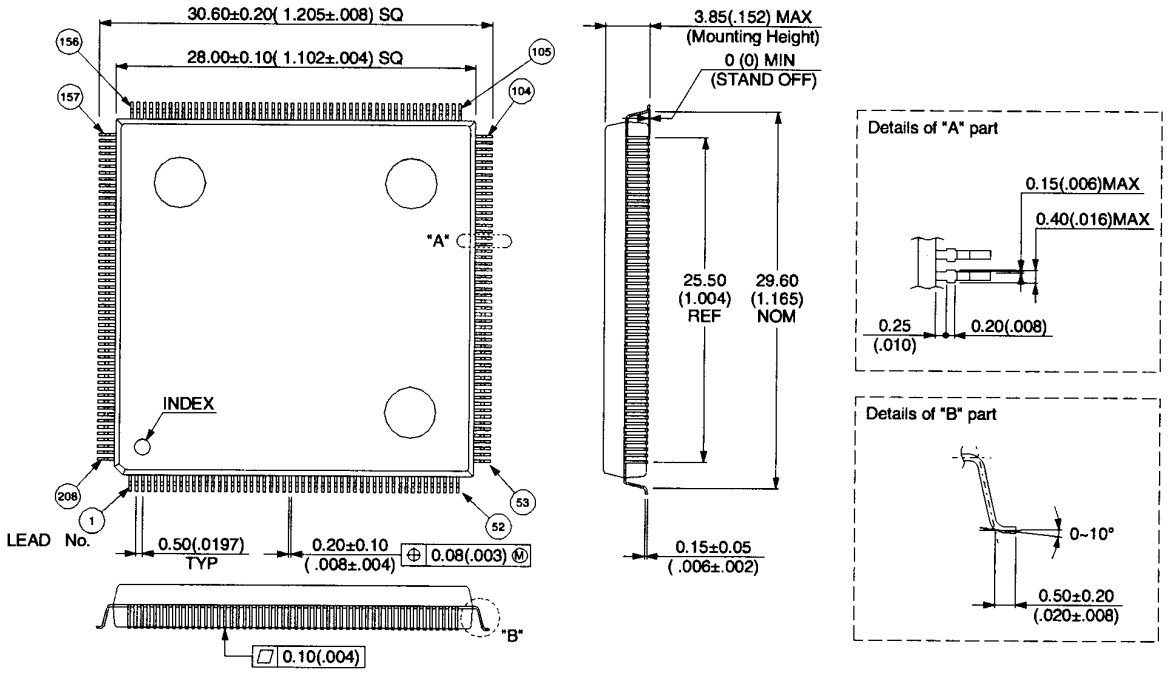
MECHANICAL DIMENSIONS - 208 LEAD QFP PACKAGE

208-pin plastic QFP



Lead pitch	0.50 mm
Package width x Package length	28 x 28 mm
Lead shape	Gullwing
Sealing method	Plastic mold

208-pin plastic QFP
(FPT-208P-M01)



Dimensions in mm (inches).

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