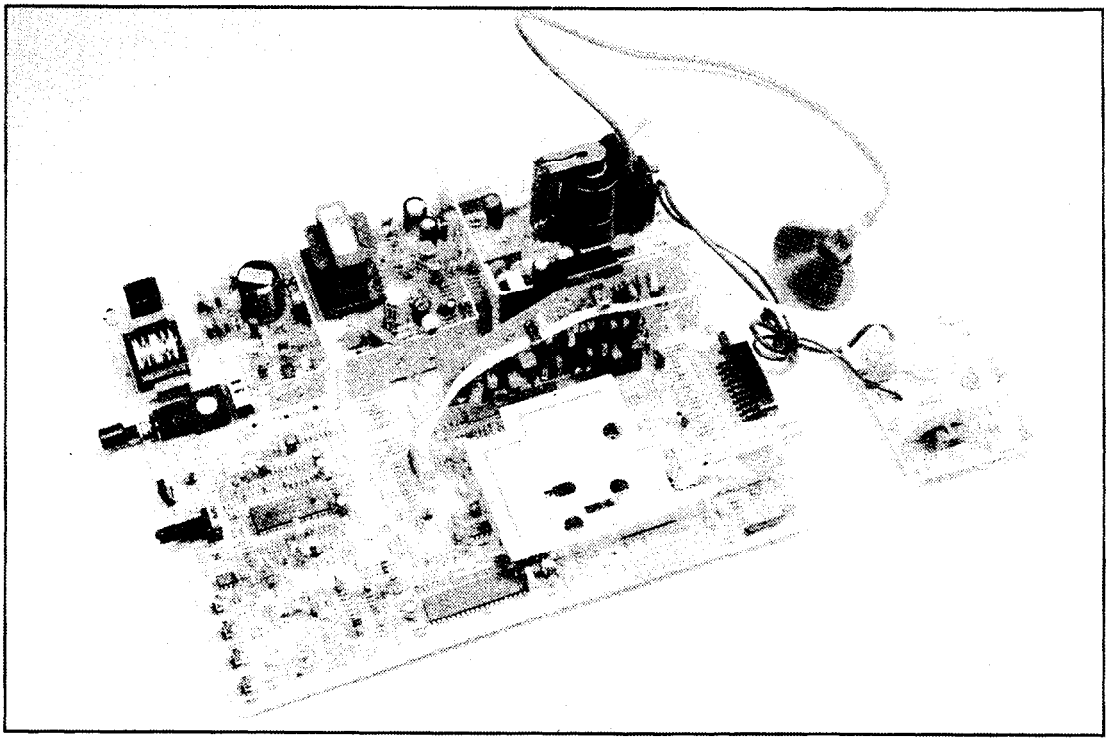
SERVICE MANUAL

PT-11 CHASSIS

AKAI



TV-1411TGB

TV-2111TGB

PT-11 CHASSIS ADJUSTMENT PROCEDURE

1- System Voltage (+B) Adjustment :

- Before switching on TV, all potentiometers should be adjusted at medium level. Then TV is switched on;
- Adjust all of the analog parameters to minimum with RC
- Adjust P1 trimpot until find +115 V on the cathode of D2 diode

2- AFT Adjustment:

- Place a balloon coil (300 Ohm dc resistance) parallel to L104
- Apply 80 dB uV 38.9 MHz (39.5 MHz for I) signal via balloon coil
- Connect a voltmeter to aft pin (pin 9) of IC301
- Adjust T101 coil until the voltage of this pin being 2.5 V dc

3- Adjustment of G2:

- Apply Philips Test pattern
- Adjust all of the analog parameters to minimum with RC
- Adjust G2 trimpot until seeing two bars on gray scale

4- Horizontal and Vertical Adjustment:

- Apply Philips Test pattern signal
- Center the picture horizontally while picture shifting to right and left with P101,
- Make vertical amplitude adjustment with P602 until seeing top and lower lines of picture will be seen
- Center the picture with P601

5- AGC Adjustment:

- Apply Philips Test Pattern whose amplitude is 60 dB uV to the rf input
- Adjust P102 until find a picture without snowy

6- Focus Adjustment:

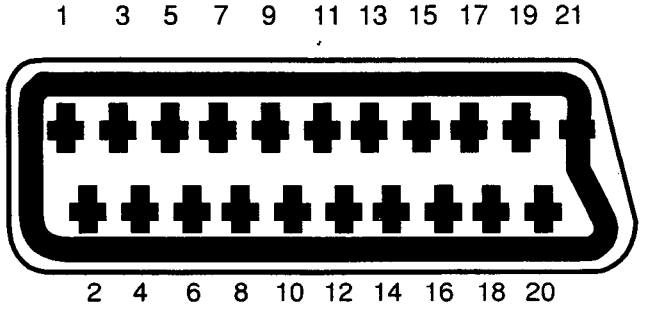
- Apply Cross-Hatch Pattern signal
- Find the optimum concentration point between H and V intersection in the middle of screen.

7- White Balance Adjustment :

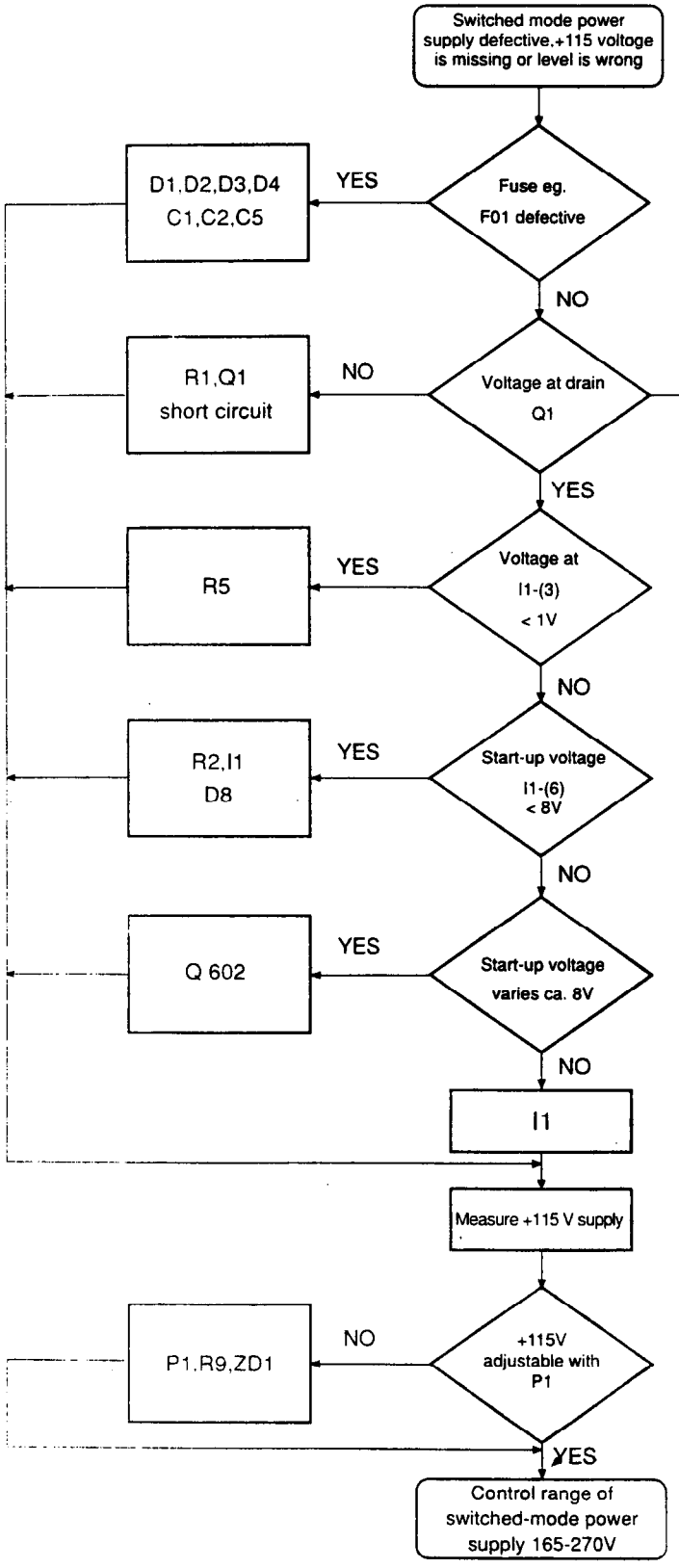
- Apply Philips Test Pattern signal
- Adjust all of the trimpots on CRT board to medium level
- Adjust color, contrast, brightness to minimum by RC
- Adjust G2
- Apply white pattern, settle in the probe of color analyzer to screen
- Increase brightness until geting Y=10 nits
- Adjust x=270 - 276 nits y=270 - 276 nits via "VR201, VR203, VR205"
- Increase brightness and contrast until Y=90 - 100 nits
- Adjust x, y to same values via "VR202 and VR204"
- Check white balance at high and low contrast level. Again make adjustment if it's necessary.

SPECIFICATIONS OF THE CONNECTOR (EURO SCART)

I- Audio output 1. right channel 0.5 VRMS/<I k 0
2- Audio input 1. right channel 0.5 VRMS (connected to No.6)
3- Audio output 2. left channel 0.5 VRMS (connected toNo.1)
4- GND (audio)
5- GND
6- Audio input 2. left channel 0.5 VRMS/>10k 0
7- RGB input, blue (B)
8- Switch signal video (status)
9- GND
10- Reserved for clock signals (not connected)
11- RGB input, green (G)
12- Reserved for remote control (not connected)
13- GND
14- GND switch signal RGB
15- RGB input, red (R)
16- Switch signal RGB
17- GND (video)
18- GND19- Video output 1 Vpp/75 ohm
20- Video input 1 Vpp/75 ohm
21- Shield



FAULT TRACING DIAGRAM-POWER SUPPLY

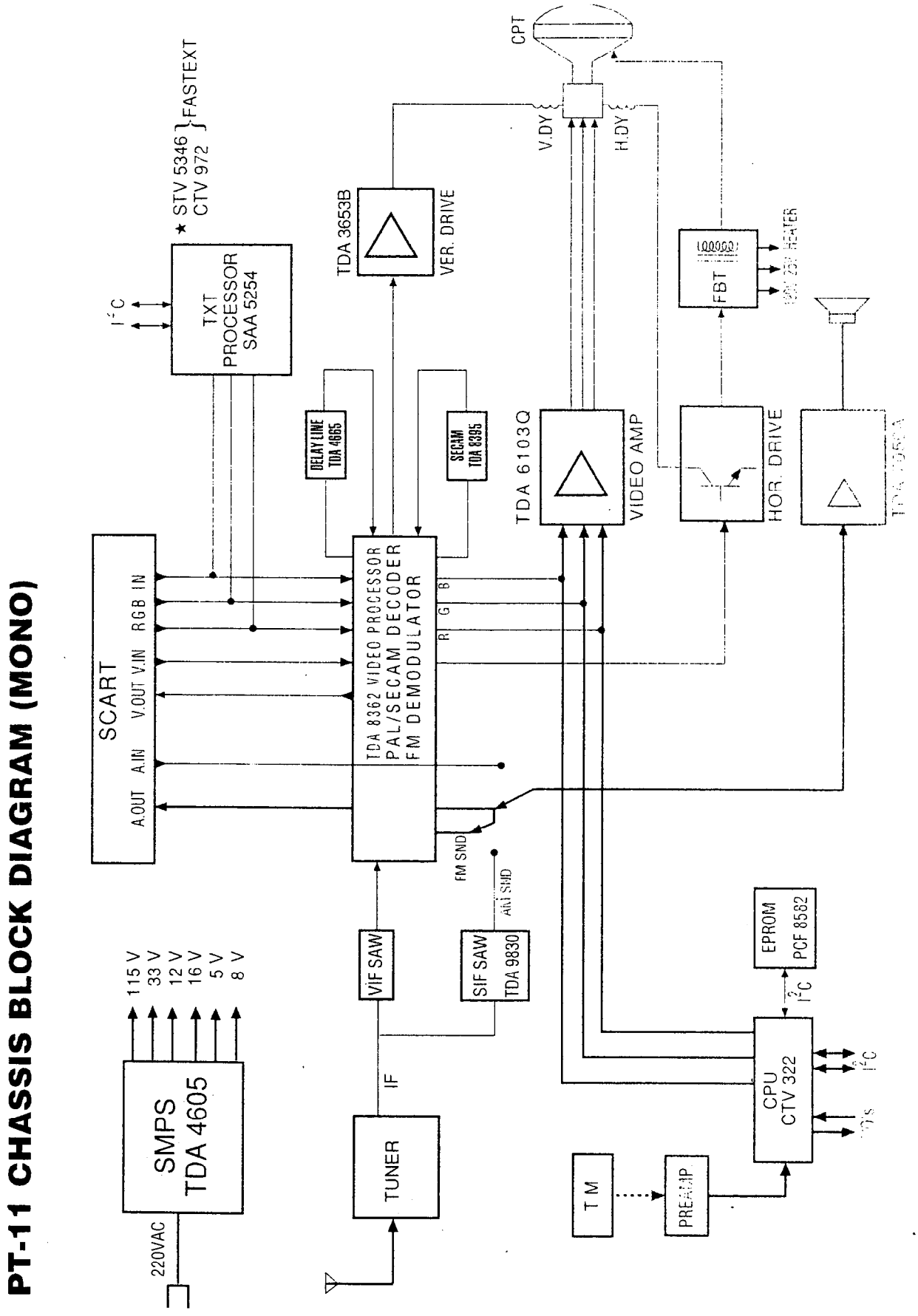


Important Service Note :
Before changing a component in the Primary Mains Stage it is imperative, that C5 is discharged by a resistor of approx. 100 Ohm.

TROUBLESHOOTING GUIDE FOR MAIN PCB

TROUBLE	CHECK POINTS
No color	I101, T102, C127, I102, check pin 38-SSC
No vertical deflection	Check +K, I601, pin 42 I401, pin 43 I401
Vertical linearity	C 625, R 623
Vertical size	C 625, R 624
Vertical shift	R 626, P 601
Horizontal linearity	L 601, C 608
Horizontal size	+B, C 607, L 602
Flue picture	I101 pin 25, ABL, FOCUS, HEATER, EHT
Dark picture	I101 pin 17, SCREEN, EHT, +M
Noise picture	TU01, AGC, IF, FI101
Vert./horizontal synchrony	I401
Interference	TU01, IF, FI101
No sound	Check I101 pin 5 and pin 50, I401 pin 3, pin 5, +G
Low sound	I101 pin 5, pin 50, I401 pin 5, +G, R 403
Sound distortion	I401, +G, R 403
Contrast	I301 pin 5, I101 pin 25, ABL
Brightness	I301 pin 3, I101 pin 17
Color saturation	I301 pin 4, I101 pin 26
Tuning	I301 pin 1, Q 301, +D, TU01
Memory	I 302, I 301, SDA, SCL
Band select	I 301 pin 7/8, I 303, +K, TU01
No video-out on the SCART	Check TV-VID signals, Q 651
No video-in on the SCART	Check I301 pin 12, I101 pin 16 on AV mode, check the video signals on AV mode SCART pin 20 and I101 pin 15
No sound out on the SCART	I101 pin 1, Q 653 , Q654
No sound in on the SCART	Check the audio signals on SCART pin 2/6 and I101 pin 6
No remote control reception	Check signals on pin 3 IR01and I301 pin 35

PT-11 CHASSIS BLOCK DIAGRAM (MONO)



DESCRIPTONS OF THE PARTS

1- SWITCH MODE POWER SUPPLY STAGE

In order to supply the DC voltage required at various parts of the chassis, a SMPS transformer controlled by the IC TDA 4605 and switching transistor 3N90 is used. Cl, EM1, C2 filter circuit prevents the network noises and the effects of high frequency which produced in TV set. After rectifying DC voltage is filtered by using C5. The stat up voltage of TDA4605 is obtained from R2 at the same time a square wave ii produced from pin 5 of IC TDA4605. This square wave reaches Ql passing through R8. After that Q1 form and induction on TR1. which produces a voltage on pin 6. This voltage rectified by D6 is used as a supply voltage of IC 1. IC 1 does not operates SMPS by stopping pulses at pin 5, when the network is higher or lower than fixed limits. Pin 2 is control pin of overload. This stage produces 115V for FBT, 12V for audio part, 33 V for tuning circuit 5V, 12V (tuner and some ICs) and 8V (for TDA8362) are produce by the means of the regulators LM7805, LM317 and LM7808. This circuit operates between 165 VAC and 250VAC (5OHz).

2- MICROCONTROLLER STAGE

Below items are controlled or generated by means of these controllers.

- CTV 322S V2.0 (for mono models) and CTV 352S V1.4 (for stereo models) are used as controller on PT chassis.
- Voltage synthesis tuning
- On screen display
- Control of two transmission standard
- Controls of the simple text or fastext decoder
- Full peri-TV (scart) switching and double scart switching on stereo models,
- Controls of stereo decoder TDA 9840 as German Stereo Decoder
- SAA 7283 as Nicam decoder
- Sound processing (Bass, treble, balance)
- Controls of the analog values of the picture (Brightness, Color, Contrast)

3- ANALOG OPERATION PART WITH TDA 8362

TDA8362 is a single-chip TV processor which contains nearly all small signal functions that are required for color television receiver. Fora complete receiver the following circuits need to be added a base-band delay line (TDA4665) a tuner and output stages for audio, video and horizontal and vertical deflection. TDA8362 can handle signals with positive modulation and it supplies the signals which are required for secam decoder TDA8395.

VIDEO IF AMPLIFIER

The IF amplifier contains 3 AC-coupled control stages with a total gain control range of greater than 60 dB.The reference carrier for the video demodulator is obtained by means of passive regeneration of the picture carrier. The external reference tuned circuit is the only remaining adjustment of the IC.

In the TDA8362 the polarity of the demodulator can be switched so that the circuit is suitable for both positive and negative modulated signals. The AFC circuit is driven with the same reference signal as the video demodulator. To ensure that the video content does not disturb the AFC operation a sample and hold circuit incorporated: the capacitor for this function is internal. the AFC output voltages 6V. The AGC detector operates on levels, top sync for negative modulated and top white for positive modulated signals . The AGC detector time constant capacitor is connected externally.

SOUND IF CIRCUIT

On mono models;

The sound bandpass and trap filters have to be connected externally. The filtered intercarrier signal is fed to a limiter circuit and is demodulated by means of PLL demodulator. The PLL circuit tunes itself automatically to the incoming signal, consequently, no adjustment is required.

The volume is DC controlled. The composite audio output signal has an amplitude of 700 mV RMS at a volume control setting of -6 dB. The de-emphasis capacitor has to be connected externally. The non-controlled audio signal can be obtained from pin 1 via a buffer stage. The amplitude of this signal is 350 mV RMS.

The TDA8362 external audio input signal must have an amplitude of 350 mV RMS. The audio/video switch is controlled via the chrominance input pin.

On stereo models;

On stereo models, the adjustable sound output pin (pin50) is used for mono sound. An external sound IF circuit TDA3845 is used for NICAM B/G, I stereo systems. For NICAM L stereo system, TDA4470B Sound IF IC is used so that obtain AM sound and NICAM I sound carrier. On German Stereo system, TBA120U is used as FM demodulator for second sound carrier.

SYNCHRONIZATION CIRCUIT

The sync separator is preceded by a voltage controlled amplifier which adjusts the sync pulse amplitude to a fix level. The sync pulses are then fed to the slicing stage (separator) which operates at 50 % of the amplitude.

The separated sync pulses are fed to the first phase detector and to the coincidence detector. The coincidence detector is used for transmitter identification and to detect whether the line oscillator is synchronized. When the circuit is not synchronized, the voltage on the peaking control pin (pin 14) is LOW so that this condition can be detected externally

The IC TDA8362 contains a start up circuit for the horizontal oscillator. When this feature is required a current of 6.5 mA has to be supplied to pin 36.

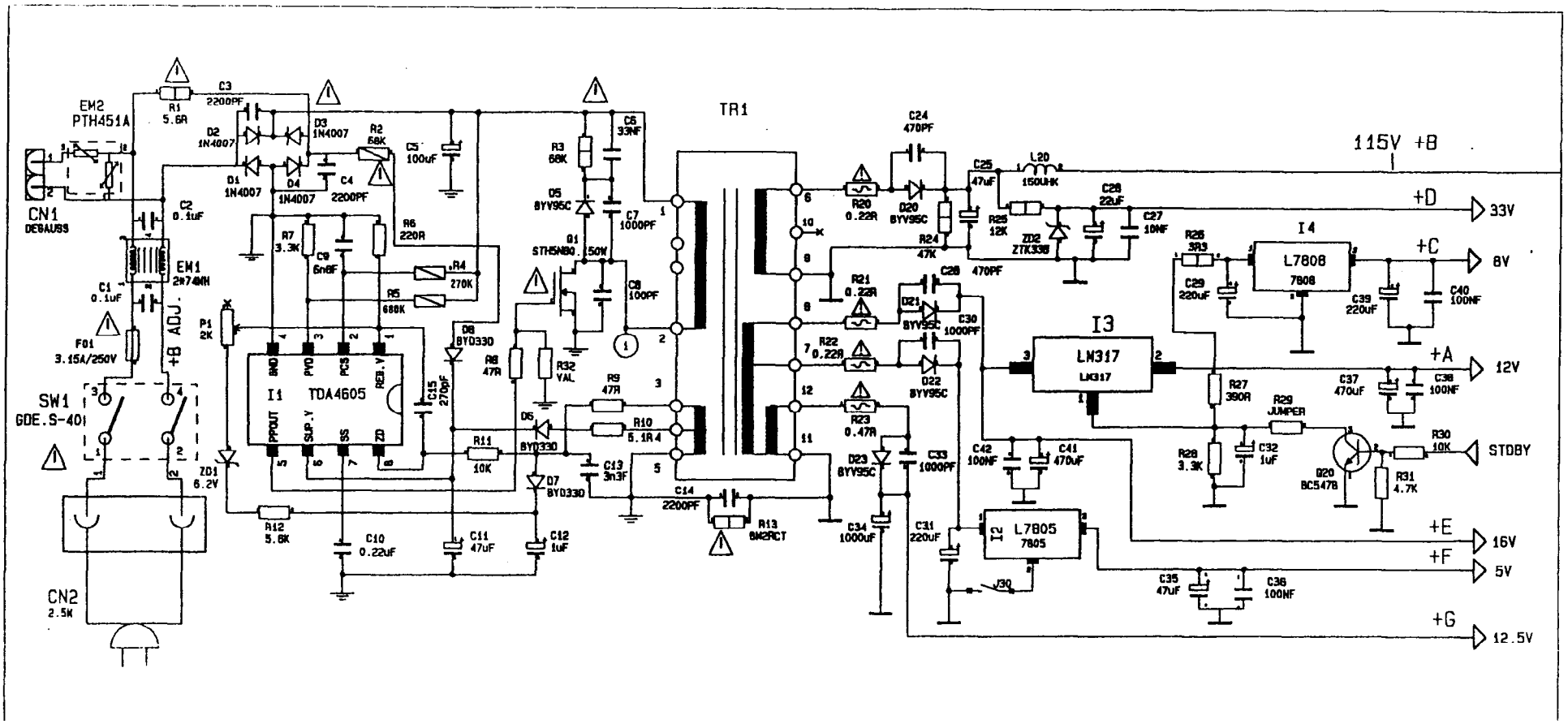
COLOR DECODING

TDA8362 contains PAL and NTSC decoder (TDA8361 contains only PAL decoder) but it can cooperate with the secam add-on secam decoder TDA8395. The communication between two IC's is achieved via pin 32. The TDA8362 supplies the reference signal (4.43 MHz) for the calibration system of the TDA8395, identification of the color standard is via the same connection. When a SECAM signal is detected by the TDA8395 the IC will draw a current of 150 uA. When TDA8362 has not identified a color signal in this condition it will go into the SECAM mode, that means it will switch of the

R-Y and B-Y outputs and increase voltage level on pin 32.

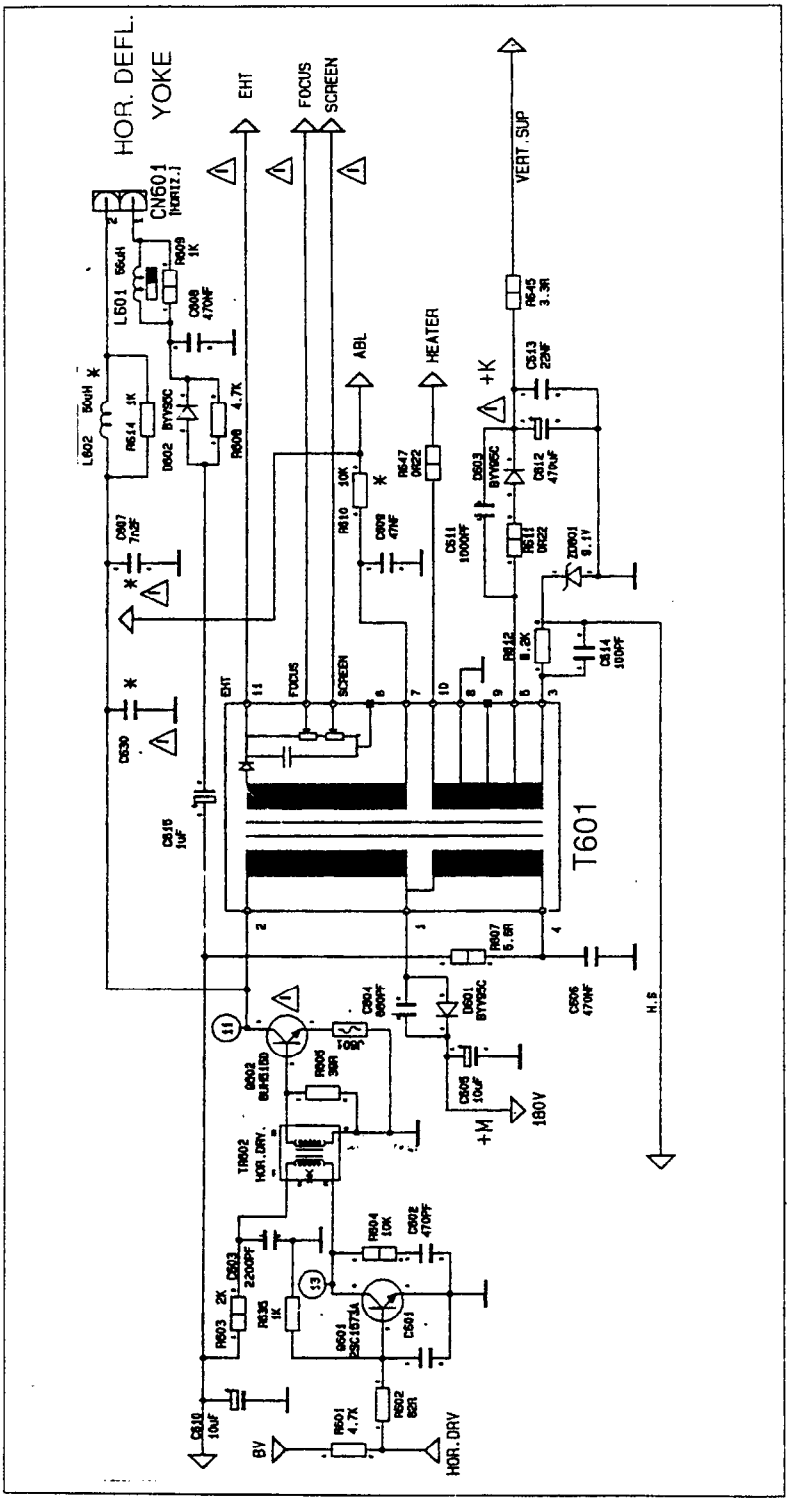
4- VERTICAL DEFLECTION CIRCUIT WITH TDA3653B

The TDA3653B is vertical deflection circuit for drive of various deflection systems with currents up to 1.5 A peak to peak. Pin 5 is the output pin. the supply for the output stage is fed to pin 6 and the output stage ground is connected to pin 4. Pin 1 is the input for the driver of the output stage . The signal at pin 1 is also applied via external resistors to pin 3 which is the input of the switching circuit. When the flyback starts, this switching circuit rapidly turns off the lower output stage and so limits the turn-off dissipation. It should be noted that the lowest voltage at pin 8 is > 2.5 V, during normal operation.


EM2
PTH451A
CN1
DEBAUSS
EM1
2m74MH
F01
3.15A/250V
SW1
GDE.S-401
+B ADJ.
P1
2K
CN2
2.5K
I1
TDA4605
BMD
PVD
PCS
REG.V
PPOUT
SUP.V
SS
ZD
TR1
Q1
STH5NB0.150W
D5
BYV95C
D6
BYD330
D7
BYD330
D8
BYD330
ZD1
6.2V
R1
5.6R
R2
68K
R3
68K
R4
270K
R5
680K
R6
220R
R7
3.3K
R8
47R
R9
47R
R10
5.1R4
R11
10K
R12
5.6K
R13
6M2RCT
R20
0.22R
R21
0.22R
R22
0.22R
R23
0.47R
R24
47K
R25
12K
R26
3R3
R27
390R
R28
3.3K
R29
JUMPER
R30
10K
R31
4.7K
R32
VAL
C1
0.1uF
C2
0.1uF
C3
2200PF
C4
2200PF
C5
100uF
C6
33NF
C7
1000PF
C8
100PF
C9
6n8F
C10
0.22uF
C11
47uF
C12
1uF
C13
3n3F
C14
2200PF
C15
270pF
C24
470PF
C25
47uF
C26
470PF
C27
10NF
C28
22uF
C29
220uF
C30
1000PF
C31
220uF
C32
1uF
C33
1000PF
C34
1000uF
C35
47uF
C36
100NF
C37
470uF
C38
100NF
C39
220uF
C40
100NF
C41
470uF
C42
100NF
L20
150UHK
D20
BYV95C
D21
BYV95C
D22
BYV95C
D23
BYV95C
ZD2
Z7K338
I2
L7805
7805
I3
LM317
LM317
I4
L7808
7808
Q20
BC547B
J30
115V +B
+D
33V
+C
8V
+A
12V
STDBY
+E
16V
+F
5V
+G
12.5V

5- HORIZONTAL DRIVE CIRCUIT

The horizontal drive pulses obtained from pin 37 of the TDA8362 are connected to base of Q601(2SC1573) via R602 . Q601 drives Q602 (BUH515D) via the drive transformer TR602. TR601 is the EHT transformer. + B (115 V) is switched by Q602 and TR601 generates both "EHT, FOCUS, G2 voltages required for CRT" and "170 V. Heater voltage and 26 V vertical supply voltage". The anode beam current information from pin 7 of TR601 is used for reducing contrast at too high beam currents, in order to stabilize the voltages derived from power supply.



HORIZONTAL DRIVE PART CIRCUIT DIAGRAM

6- SOUND OUTPUT STAGE

On mono models, TDA7056A is used as sound output amplifier with DC volume control. Pin 50 of the TDA8362 is AC coupled to the input pin 3 of the TDA7056A via a RC filter. It is supplied by + 12V coming from a separate winding in the SMPS transformer.

On stereo models, TDA7057AQ is used as sound amplifier. The sound level is controlled by sound processor TDA8425 via I^2C bus on stereo boards. The outputs of TDA8425 (pin 9 and pin 13) is connected to TDA7057AQ via a divider circuit and two capacitors.

7- TELETEXT STAGE

The teletext stage consists of I SAA5254. On this stage, it should be paid attention that there is video signal on pin 8 of I SAA5254 after a RCL filter, on condition that existence of the other requirements such as +5V, periferical components.

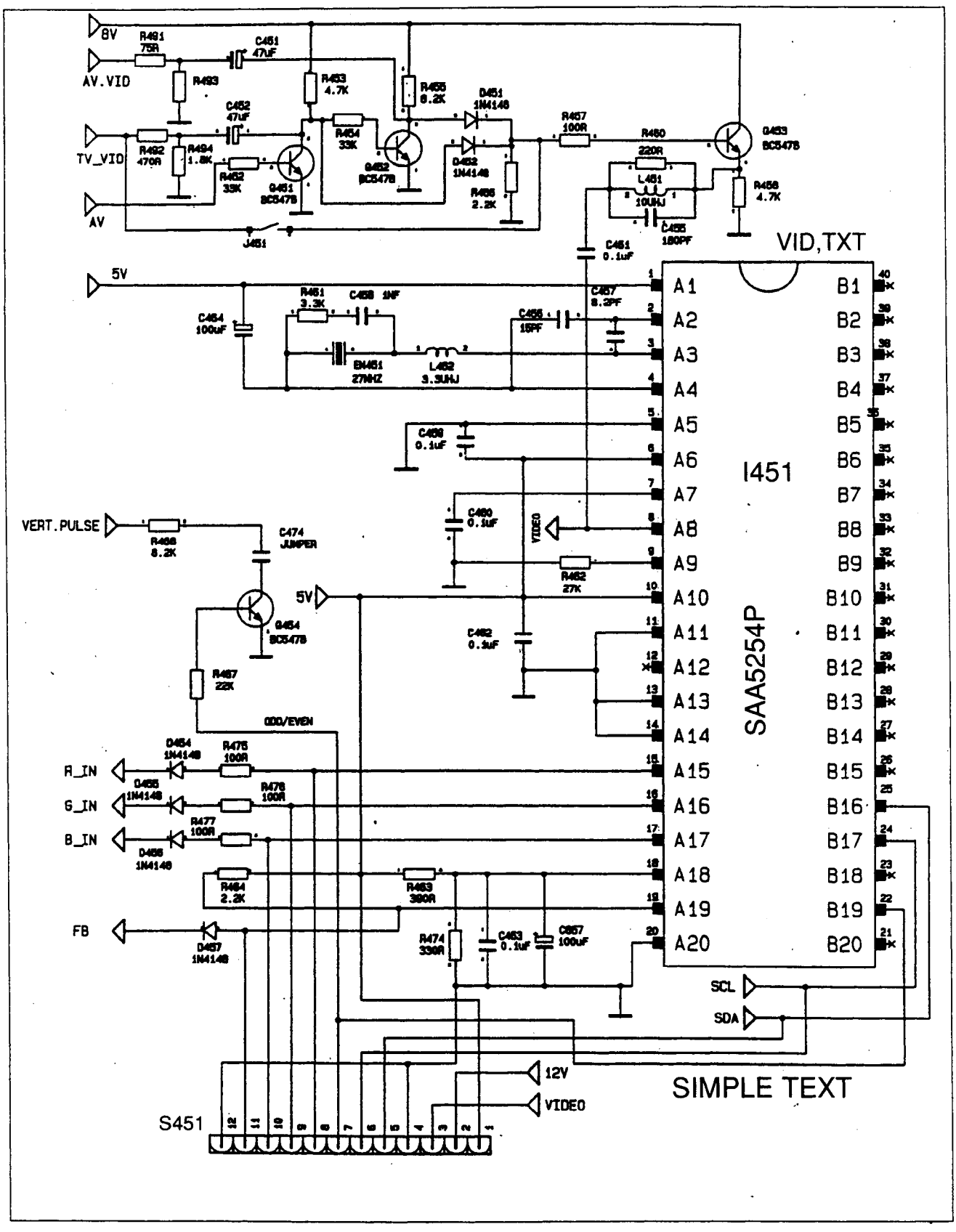
Basically, fastext stage consists two I's, STV5346 Teletext decoder and CTV 974 fastext controller with I^2C bus interface. For List Mode a 2K EEPROM (PCF8582) can be added.

8- CRT STAGE

The TDA6103Q is used on CRT stage as video output amplifier. The TDA6103Q consists of three monolithic video output amplifiers. Each amplifier can be seen as an operational amplifier with negative feedback. The advantage of negative feedback is that the amplifier characteristics do not play an important role up to certain frequencies.

The device needs only one power supply voltage (+M). In contrast to previous types of DMOS video amplifiers, the TDA 6103Q does not need a second supply voltage (12V.), so it saves one wire from motherboard to CRT stage.

As the TDA 8362 has no white point adjustment and no black current set-up, two adjustments are required for gain and three adjustments for black setting.



SIMPLE TEXT PART CIRCUIT DIAGRAM

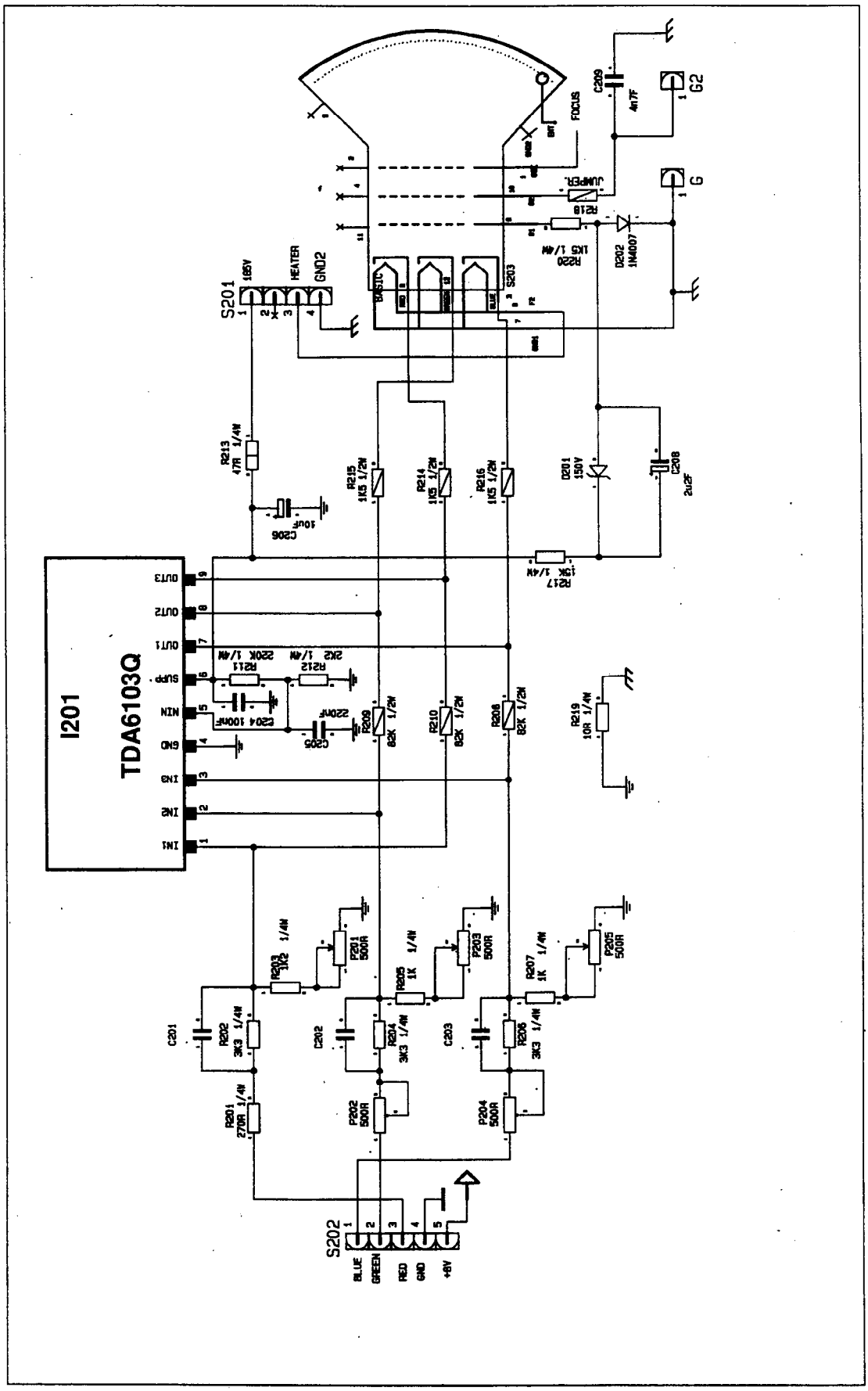
THE DETAILS OF THE BOARDS

Mother Board Contains

- TDA 8362 multistandard TV processor
- CTV 322 / CTV 352 S micro controller with OSD
- TDA 4605 Switch Mode Power Supply Controller
- TDA 4665 Baseband Delay Line
- TDA 8395 Secam Decoder
- TDA 7056A Audio Output Amplifier (for mono)
  TDA 7057AQ Audio Output Amplifier (for stereo)
- PCF 8582 2K EEPROM
- TDA 3653B Vertical Driver
- SAA 5254 Simple Text Processor
- TDA 9830 AM Demodulator
- LM 317 Voltage Regulator
  LM 7805 Voltage Regulator
  LM 7808 Voltage Regulator
- Tuner
- Infrared Receiver
- Horizontal Deflection Part
- Degaussing Circuit
- 4 push buttons (p+, p-, v+, v-)
- Stand By Led
- Main Switch
- Scart Jack
- Extension Connectors

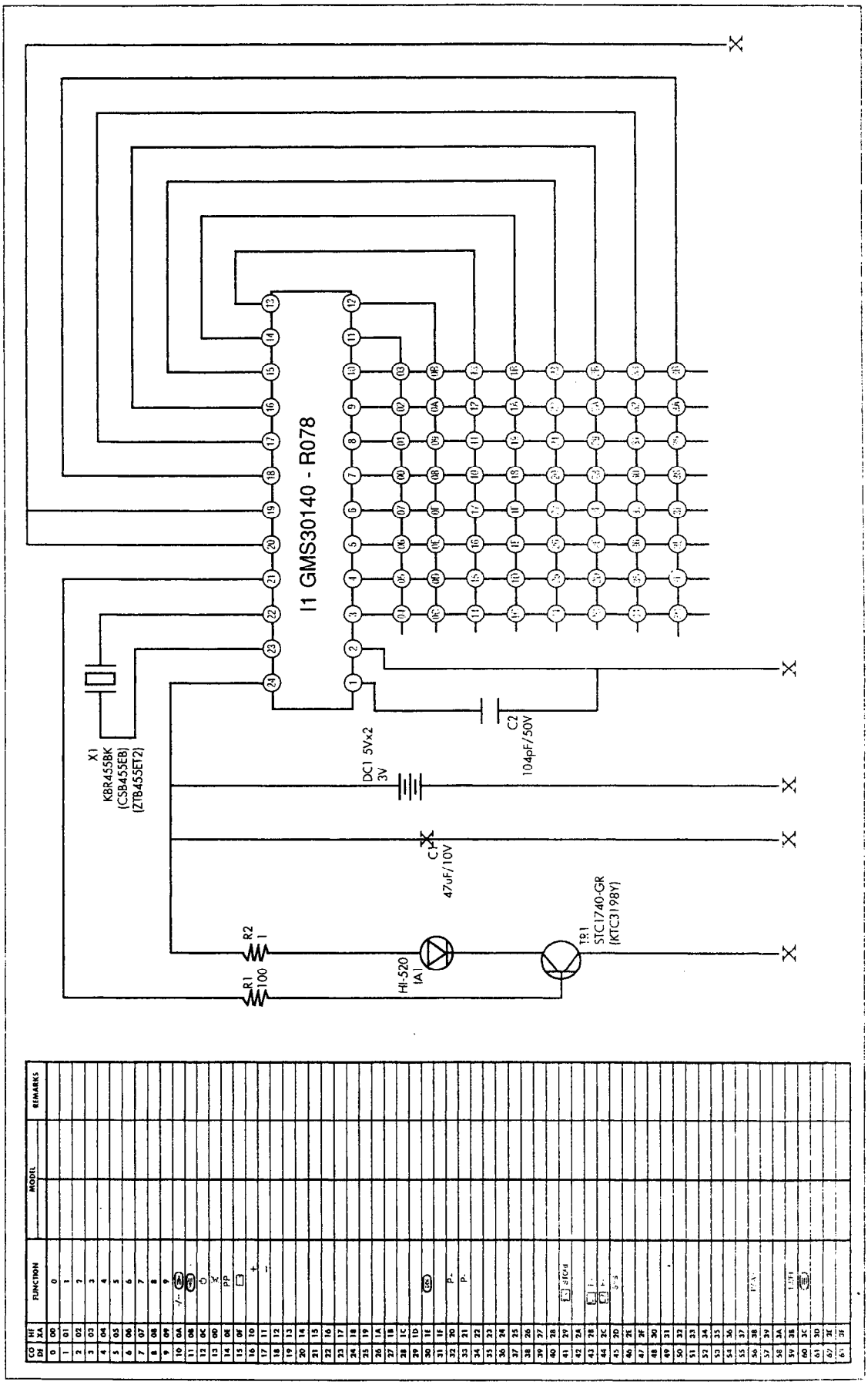
CRT Board

- TDA 6103Q Video Output Amplifier



CRT BOARD CIRCUIT DIAGRAM

REMOTE CONTROLLER TRANSMITTER PCB CIRCUIT DIAGRAM



THE DESCRIPTION OF THE INTEGRATED CIRCUITS

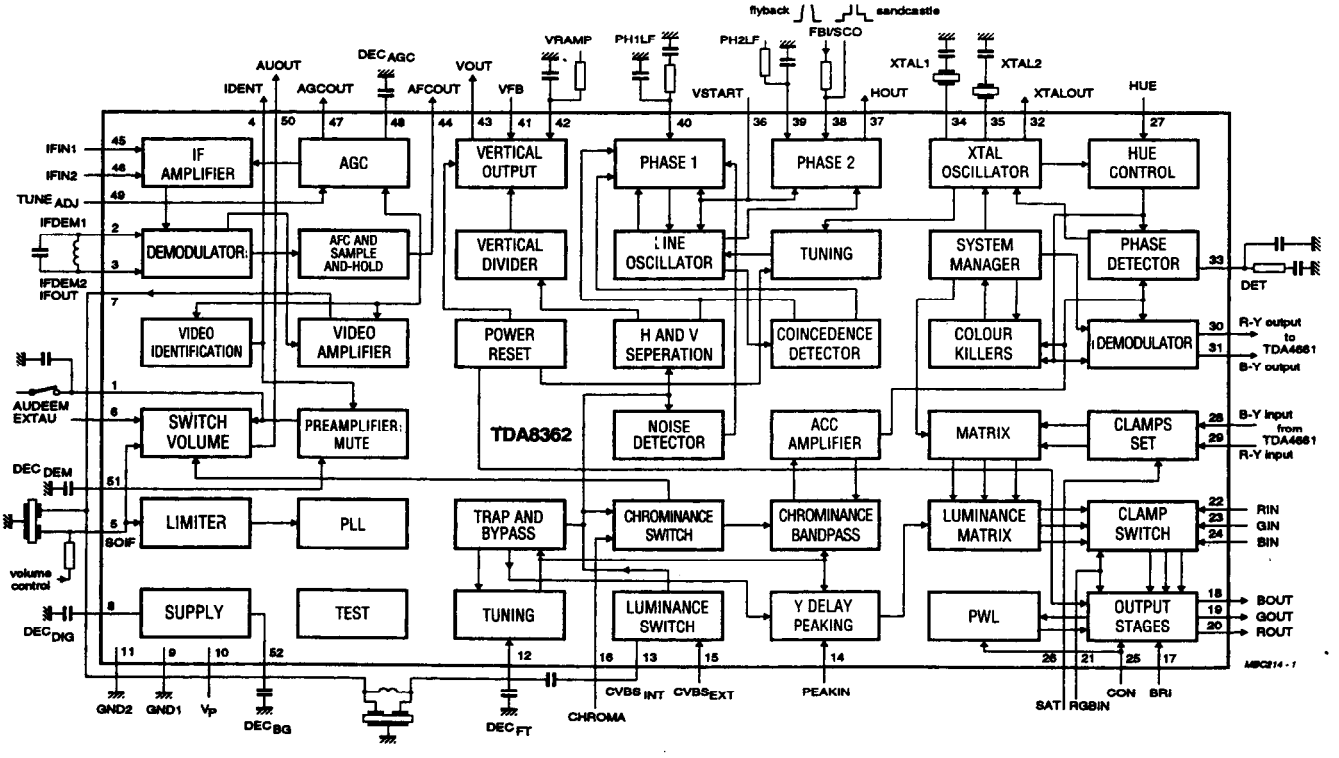
Video Processing Unit With TDA8362

Video and time base is based on the TDA 8362 Multistandard TV Processor(Pal Decoder),TDA 4665 Base-band Delay Line and TDA8395 Secam Decoder.

The Features of this Concept:

- Multistandard vision IF circuit (positive and negative modulation)
- Multistandard FM sound demodulator (4.5 MHz to 6.5 MHz)
- External Video and Audio Switches
- Integrated chrominance traps and baseband filters
- Integrated luminance delay line
- RGB control circuit with linear RGB inputs
- Horizontal synchronization with two loops and alignment-free horizontal oscillator without external components.
- Vertical count-down circuit (50-60 Hz) and vertical preamplifier
- Low dissipation
- Only one adjustment (vision IF demodulator)

Block Diagram

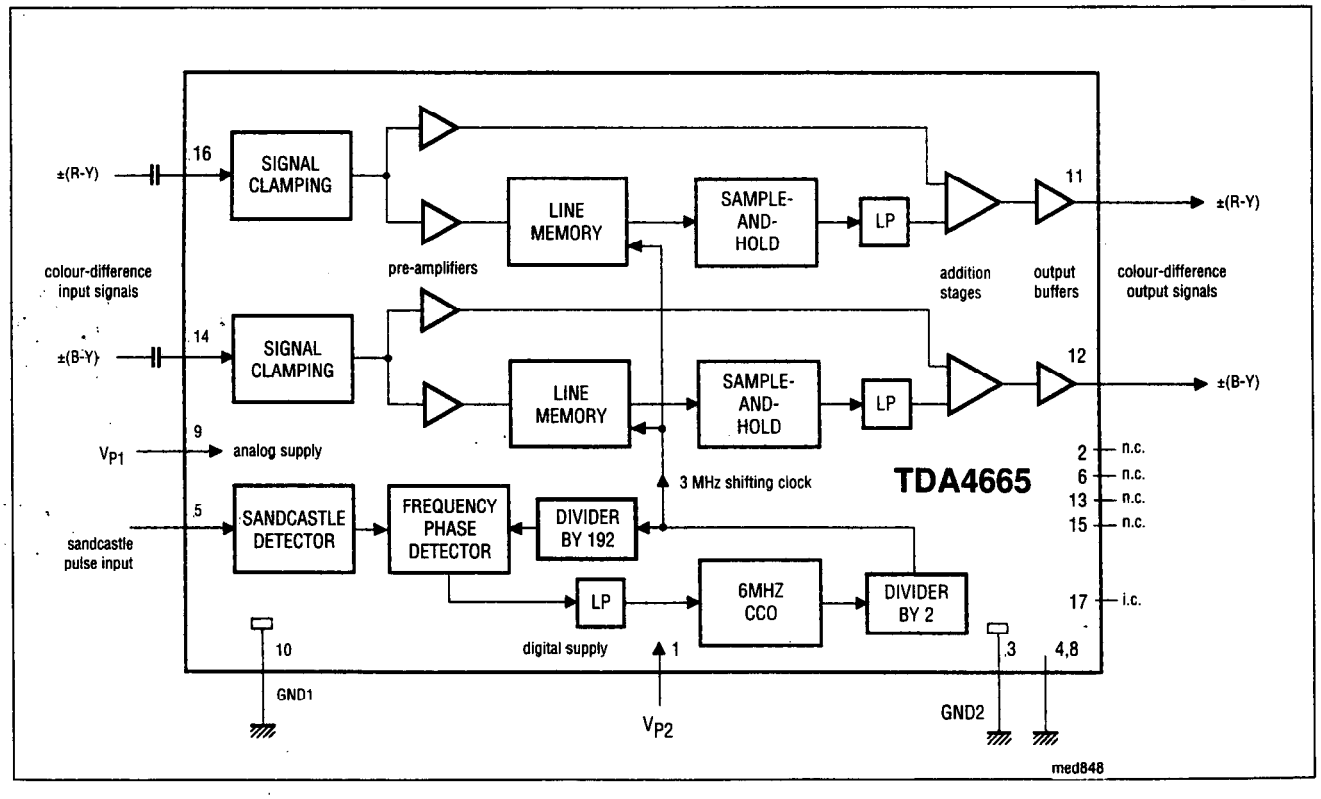


TDA 4665

The TDA4665 is an integrated baseband delay line circuit. It provides a delay of 64 us for the color difference signals. (R-Y) and (B-Y), in multi-standard TVs.

PINNING		PIN VOLTAGE
1	Digital supply voltage	: 5V
2	Not connected	: -
3	Digital ground	: 0V
4	Test input	: 0V
5	Sandcastle input	: -
6	Not connected	: -
7	Test input	: -
8	Test input	: -
9	Analog supply voltage	: 5V
10	Analog ground	: -
11	-(R-Y) output	:3.25V
12	-(B-Y) output	:3.25V
13	Reference current	: -
14	-(B-Y) input	:1.35V
15	Not connected	: -
16	-(R-Y) input	:1.35V

Block diagram

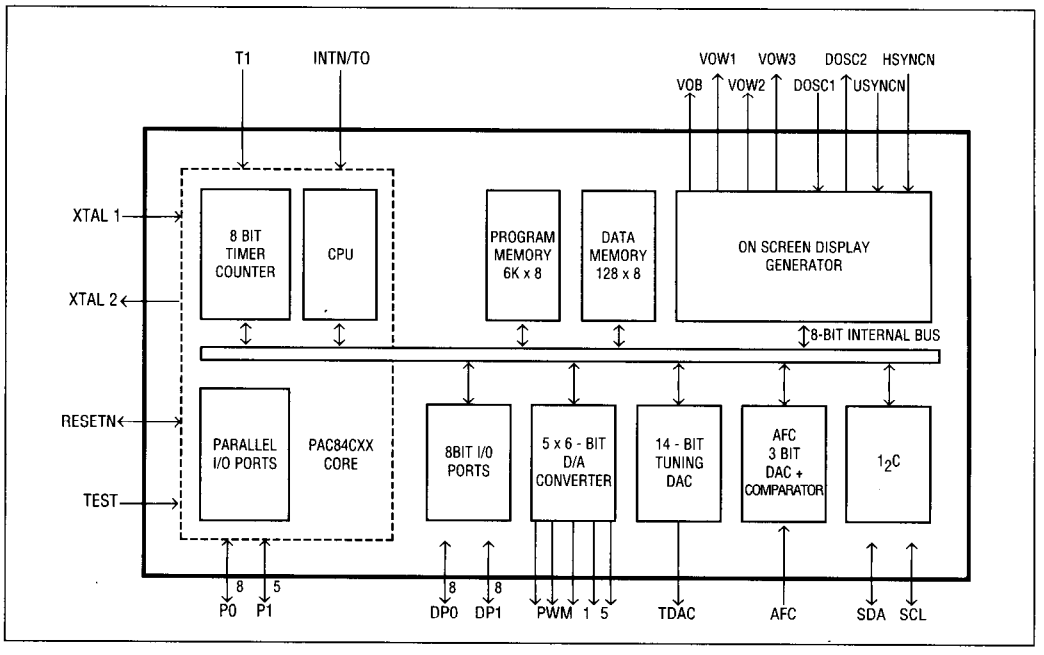


Microcontroller Unit

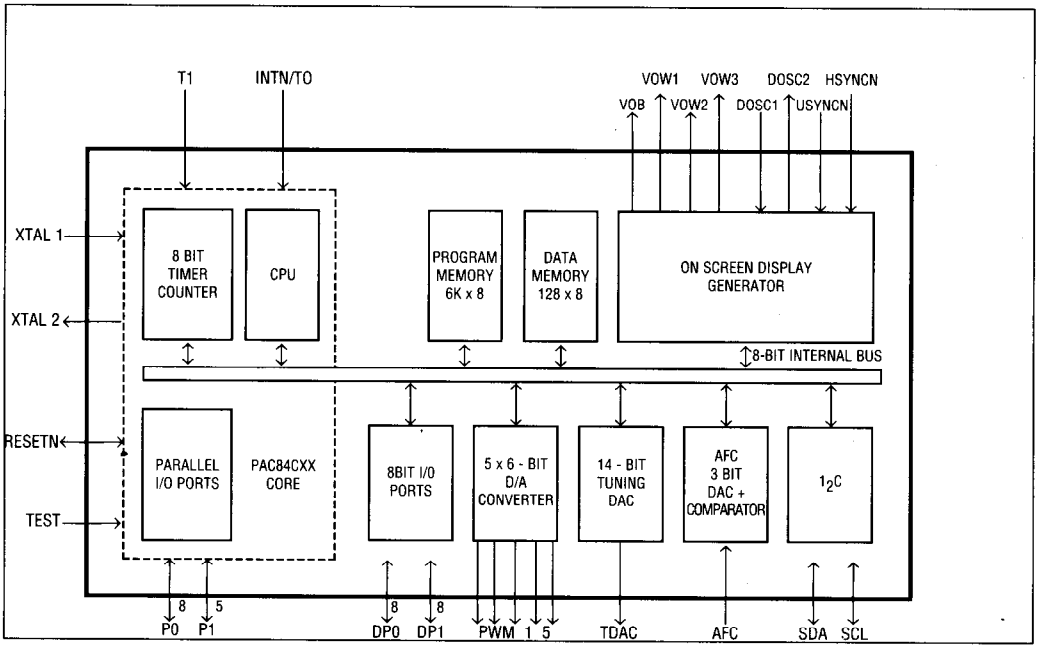
CTV 352 S(for stereo) and CTV 322(for mono) are a voltage synthesis tuning system with on screen display OSD of all relevant control function. Analog picture settings are controlled by 4 on-chip digital to analog converters. Sound volume can be controlled by the fifth on-chip digital to analog converter in mono only system. Full sound (volume, bass, treble, balance) in German Stereo and Nicam configuration and Teletext can be controlled via the I2C bus using a sound processor and teletext decoder. This controllers can control up to two scart plugs.

PINNING		PIN VOLTAGE
1	Tuning voltage control output	: 5V - 0V
2	Volume control output	: 0 - 5V
3	Brightness control output	: 0 - 5V
4	Color control output	: 0 - 5V
5	Contrast or hue control output	: 0 - 5V
6	Tone, balance or hue control output	: -
7	Band-switch 0-output	: -
8	Band-switch 1-output	: -
9	Analogue AFC sense input	: 2-4V
10	Dual/Non Dual language sound input	: -
11	VTR time constant control output	: -
12	Ext./int. audio/video source control output	: 5V (TV) - 0V (AV)
13	Keyboard scan line input/output	: -
14	Keyboard scan line input/output	: -
15	Keyboard scan line input/output	: -
16	Keyboard scan line input/output	: -
17	Keyboard scan line input/output	: -
18	Keyboard scan line input/output	: -
19	Keyboard scan line input/output	: -
20	System mode strobe output	: 5V
21	Ground supply input	: -
22	OSD red output	: 4.5Vpp
23	OSD green output	: 4.5Vpp
24	OSD blue output	: 4.5Vpp
25	OSD fast blanking output	: 4.5Vpp
26	Horizontal synchronization input	: 5Vpp HF
27	Vertical synchronization input	: 5Vpp HF
28	LC oscillator input for OSD	: 5V
29	LC oscillator output for OSD	: 5V
30	Test input; connected to ground	: -
31	Oscillator input; 10MHz crystal	: -
32	Oscillator output	: 2V
33	Power-on reset input/output	: 5V
34	Horizontal coincidence input	: 4.5V
35	RC-5 remote control input	: 4V
36	Mono/Stereo or language 1/2 output	

PINNING		PIN VOLTAGE
37	Sound effect control output	: -
38	System select output	: -
39	I^2C-bus clock signal output	: 5V and 5Vpp
40	I^2C-bus data signal output	: 5V and 5Vpp
41	Standby/On control input/output	: 0V (ST-BY) 5V (Open)
42	+5V supply voltage input	: 5V



Block diagram of PCA84C641



Block diagram of PCA84C841

Power Supply With TDA4605

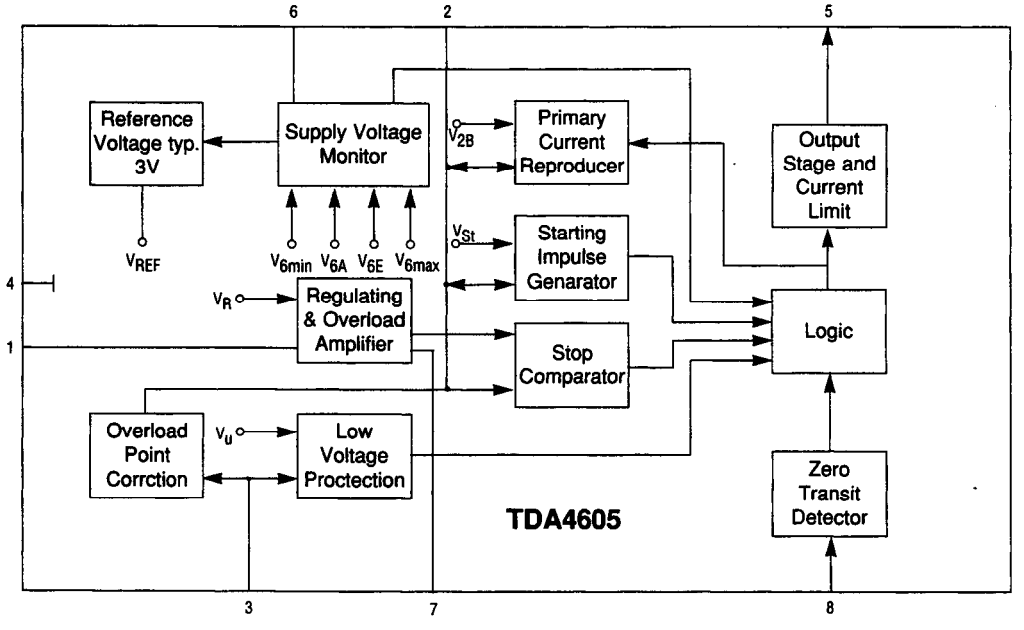
The IC TDA 4605 controls the MOS power transistor and performs all necessary regulation and monitoring functions in free running flyback converters.

Features

- Overload protection
- Burst operation under short circuit conditions
- Loop error protection
- Switch-off if line voltage is too low
- Line voltage compensation of overload point
- Soft start for quite start up
- Chip over temperature protection
- On-chip parasitic transformer oscillation suppression circuit

TDA 4605-3

PINNING		PIN VOLTAGE	
		ST-BY	NORM.
1	Information Input Concerning Secondary Voltage	0.4V	0.4V
2	Information Input Regarding the Primary Current	1V	1.2V
3	Input for Primary Voltage Monitor	2.1V	2V
4	Ground	0V	0V
5	Output	0.8V	8V (10Vpp)
6	Supply voltage Input	12V	12.8V
7	Input for Soft-Start and Integrator Circuit	1.1V	1.9V
8	Input for the Feedback of the Oscillator	0.3V	0.4V



Pin Definitions and Functions

Pin No.	Function
1	**Information Input Concerning Secondary Voltage** By comparing the regulating voltage - obtained trom the regulating winding of the transformer - with the internal reference voltage, the output impulse width on pin 5 is adjusted to the load of the secondary side (normal, overload, short-circuit, no load).
2	**Information Input Regarding the Primary Current** The primary current rise in the primary winding is simulated at pin 2 as a voltage rise by means of external RC-element. When a voltage level is reached thats derived from the regulating voltage at pin 1, the output impulse at pin 5 is terminated. The RC-element serves to set the maximum power at the overload point set.
3	**Input for Primary Voltage Monitoring** In the normal operation V3 is moving between the thresholds V3H and V3L (V3H > V3 > V3L)- V3 < V3L: SMPS is switched OFF (line voltage too low). V3 > V3H : Compensation of the overload point regulation (controlled by pin 2) starts at V3H : V3L = 1.7.
4	**Ground**
5	**Output** Push-pull output provides ±1 A for rapid charge and discharge of the gate capacitance of the power MOS-transistor.
6	**Supply Voltage Input** A stable internal reference voltage VREF is derived from the supply voltage also the switching thresholds V6A, V6E, V6 max and V6 min for the supply voltage detector. If V6 > V6E then VREF is switched on and swiched off when V6 < V6A - In addition the logic is only enable for V6 min < V6 < V6 max-
7	**Input for Soft-Start** Start-up will begin with short pulses by connecting a capacitor from pin 7 to ground.
8	**Input for the Oscillation Feedback** After starting oscillation, every zero transition of the feedback voltage (falling edge) through zero (failing edge) triggers an output pulse at pin 5. The trigger threshold is at + 50 mV typical.

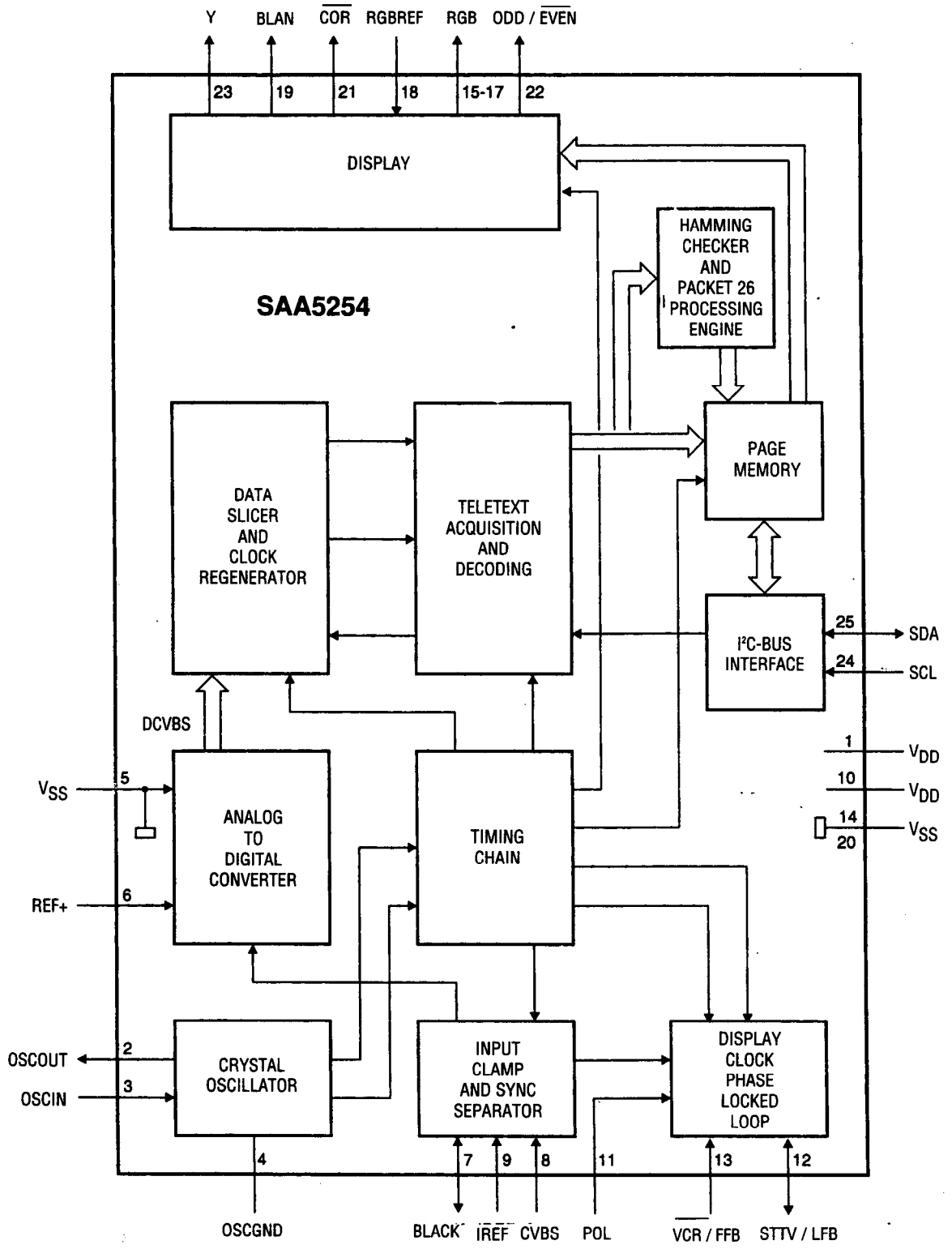
TELETEXT PART

Simple text stage consists of SAA 5254 Teletext decoder. This I is controlled via I²C bus.

Basically fastext stage consists two I's, STV 5346 Teletext decoder and CTV 974 Fastext controller with I²C bus interface. For List Mode a 2K EEPROM (PCF8582) can be added.

SAA 5254

PINNING		PIN VOLTAGE
1	+ 5V supply	: -
2	27 MHz crystal oscillator output	: -
3	27 MHz crystal oscillator input	: -
4	0V crystal oscillator ground	: 0V
5	0V ground	: 0V
6	Positive reference voltage for the ADC.	: 5V
7	Video black level storage pin, connected to ground via a 100 nF capacitor	: -
8	Composite video input pin	: 1Vpp
9	Reference current input pin, connected to ground via a 27kohm resistor	: -
10	+5V supply	: 5V
11	STTV/FB/FFB polarity selection pin	: -
12	Sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)	: -
13	PLL time constant switch/field flyback input pin. Function controlled by an internal register bit (scan sync mode)	: -
14	0V ground	: 0V
15	Dot rate character output of the RED color information	
16	Dot rate character output of the GREEN color information	
17	Dot rate character output of the BLUE color information	
18	DC input voltage to define the output high level on the RGB pins	
19	Dot rate fast blanking output	
20	Ground	: 0V
21	Programmable output to provide contrast reduction of the TV picture formixed text and picture displays or when viewing newflash/subtitle pages;open drain output	: -
22	25Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents	: -
23	Dot rate character output of teletext foreground color information; open drain output	: -
24	Serial clock input for the I²C-bus. It can still be driven during power-down of the device	: 5Vpp
25	Serial data port for the I²C-bus; open drain output. It can still be driven during power-down of the device	: 5Vpp
26	to 40 Internally connected.Must be left open-circuit in application	: -



Block diagram for SIT129 (DIL40) package

Vertical Deflection Circuit With TDA3653B

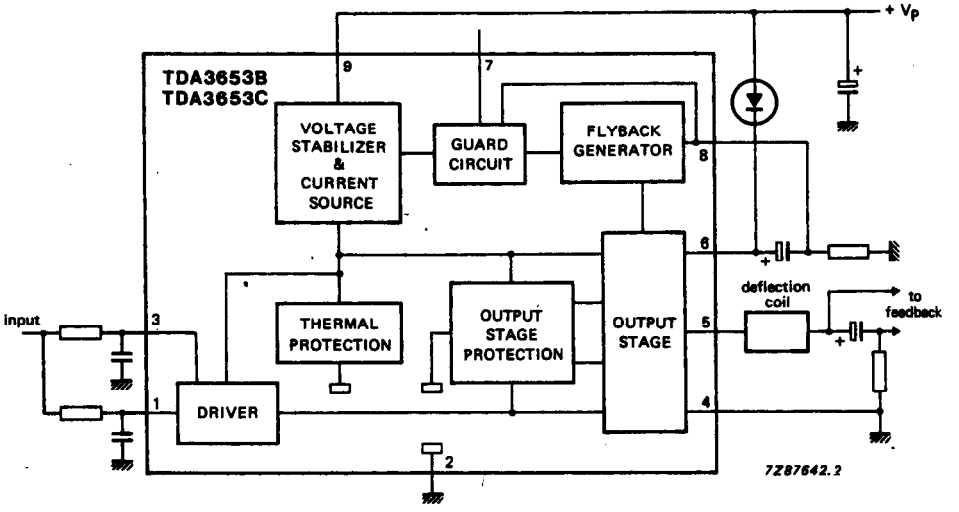
The TDA3653B is a vertical deflection output circuit for drive of various deflection systems with current up to 1.5 A peak to peak.

Features

- Driver
- Output Stage
- Thermal Protection
- Flyback Generator
- Voltage Stabilizer
- Guard Circuit

TDA 3653B

PINNING		PIN VOLTAGE
1	Output Stage Driver Input	1.2V and 2Vpp
2	Ground	-
3	Switching Circuit Input	1.2V and 2Vpp
4	Output Stage Ground	-
5	Output Voltage	13V and 45Vpp
6	Supply Voltage for the Output Stage	26V
7	DC Voltage produced by the Guard Circuit	-
8	Flyback Generator Output	8V
9	Supply Voltage	26V



Block diagram

Video Output Amplifier

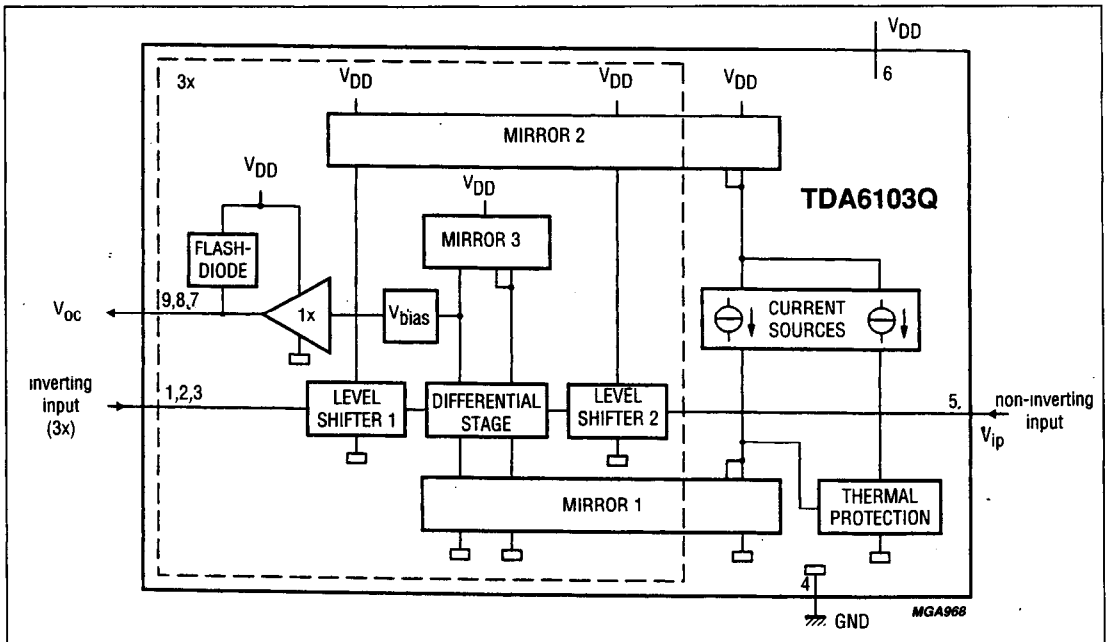
On CRT Board, TDA 6103Q is used as video output amplifier. The TDA 6103Q includes three video output amplifier intended to drive the three cathodes of color CRT.

Features

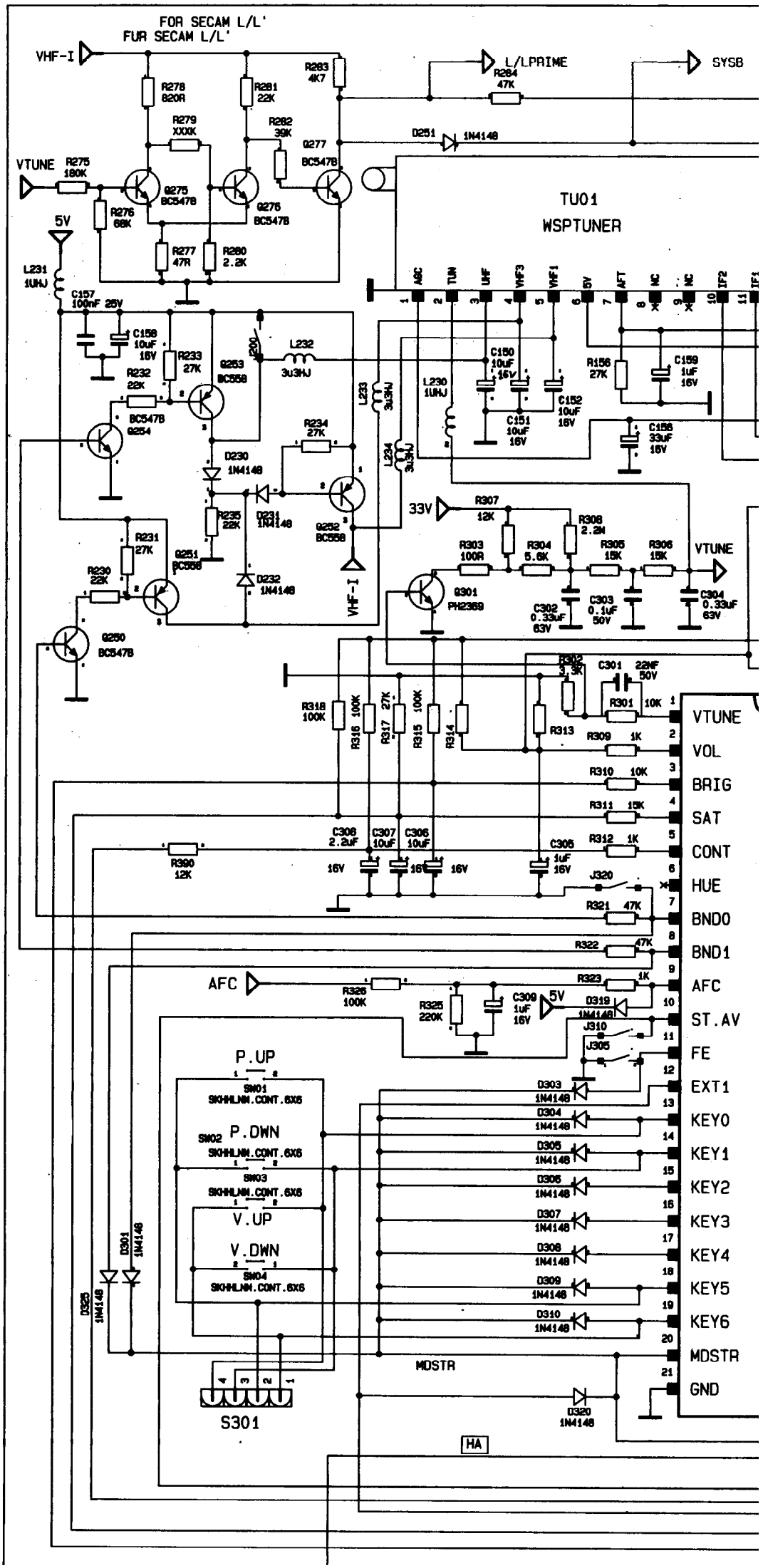
- High Bandwith : 7.5 Mhz typical
- High slew rate : 1600 V/us
- Simple application with a variety of color decoders
- Only one supply voltage needed
- Internal protection against positive appearing CRT flashover discharges
- One non-inverting input with a low minimum input voltage of 1V
- Thermal protection
- Controllable switch-off behavior

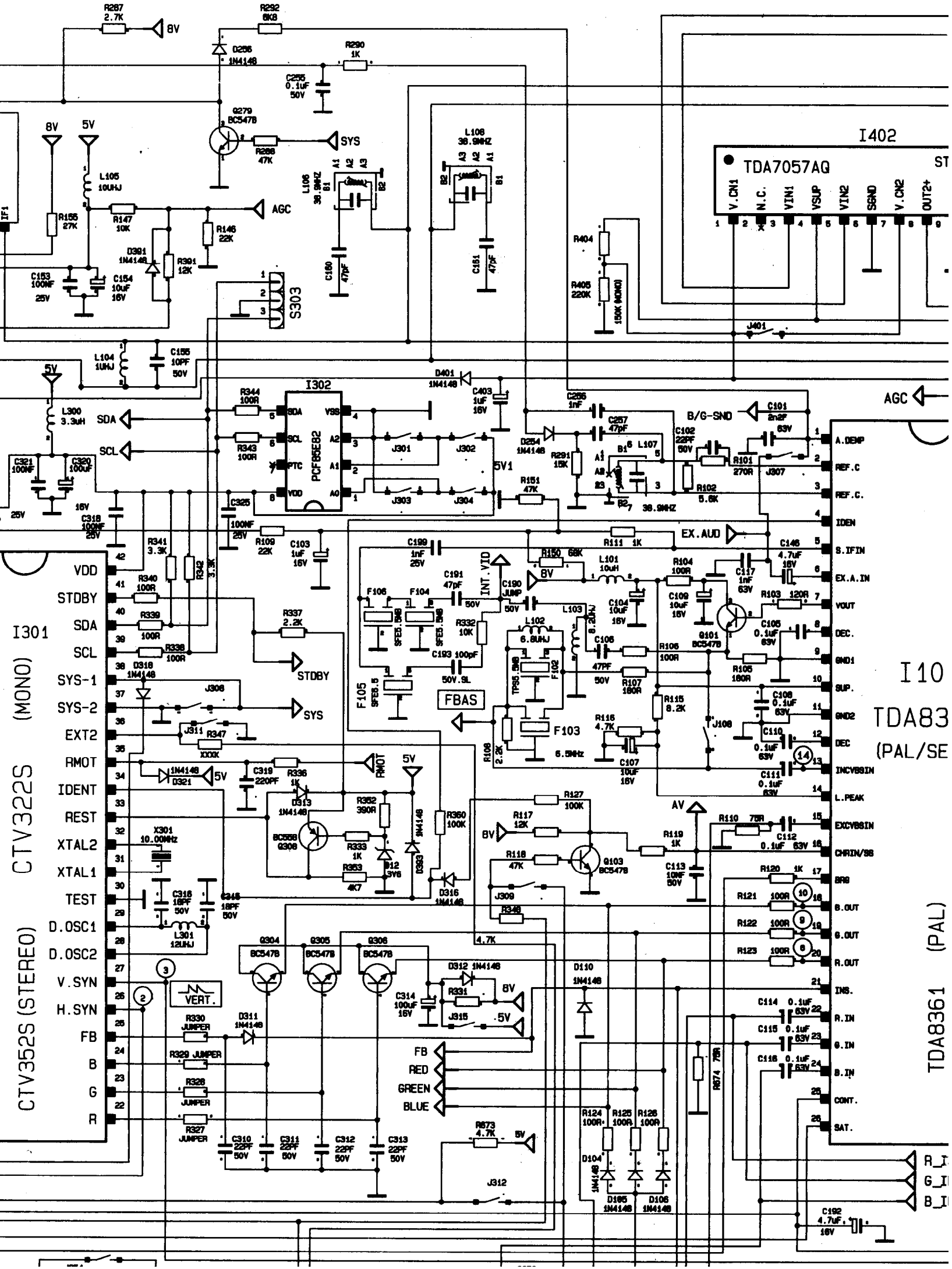
TDA 6103Q

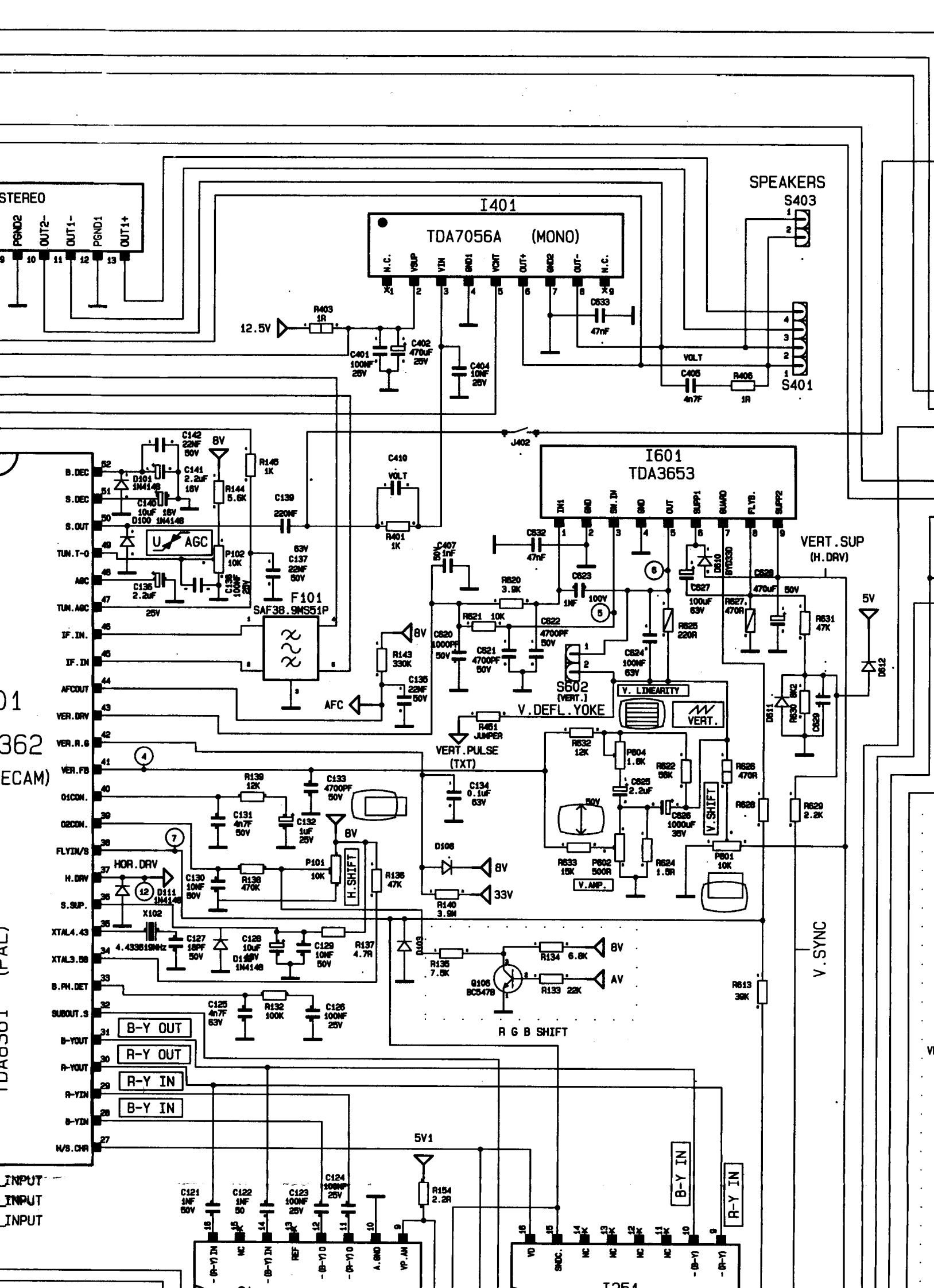
PINNING		PIN VOLTAGE
1	Inverting input 1	:1.0Vpp
2	Inverting input 2	:1.0Vpp
3	Inverting input 3	:1.0Vpp
4	Ground, fin	: -
5	Non-inverting input	:1.8V
6	Supply voltage	:180V
7	Cathode output 3	: 90Vpp
8	Cathode output 2	: 90Vpp
9	Cathode output 1	: 90Vpp

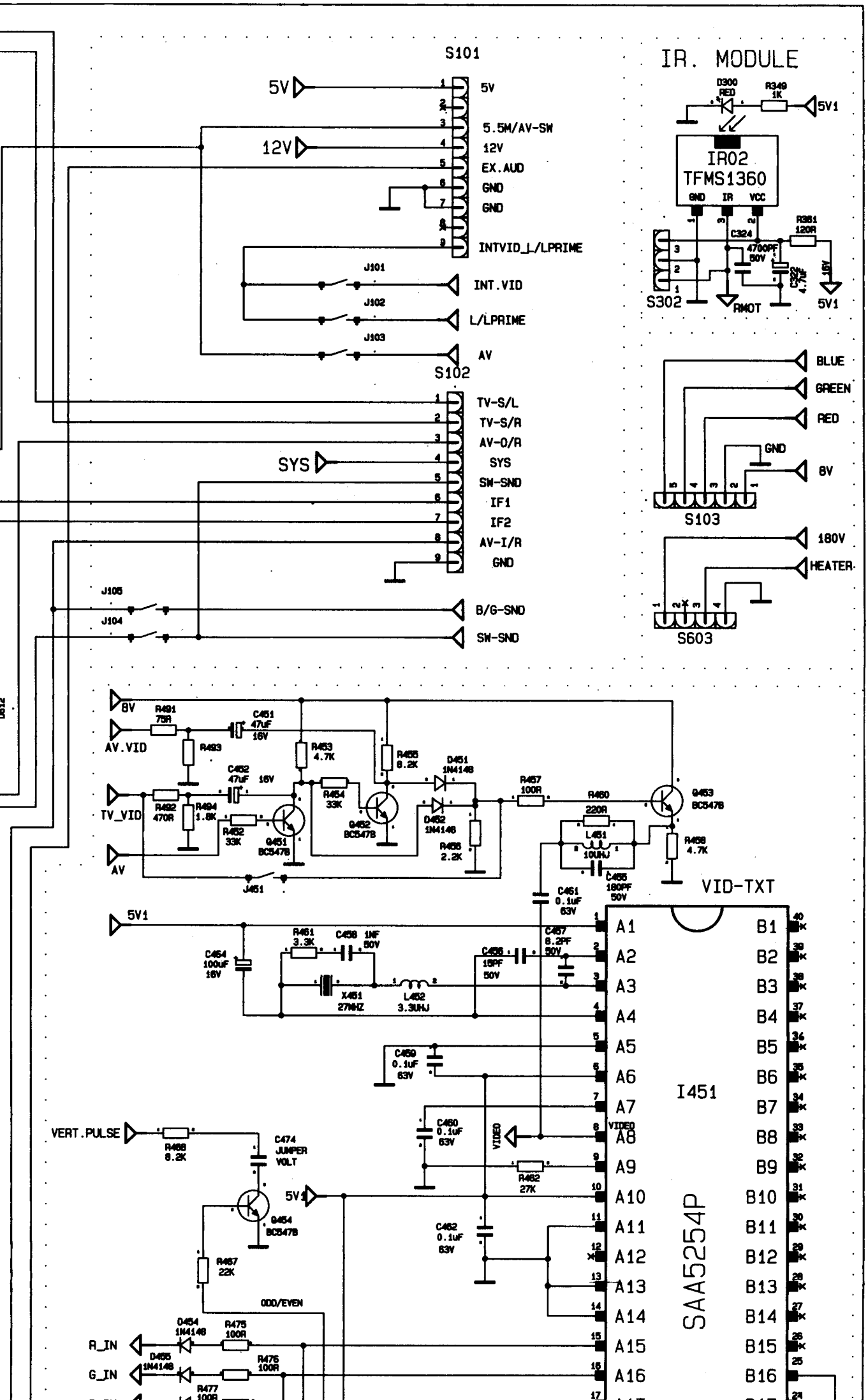


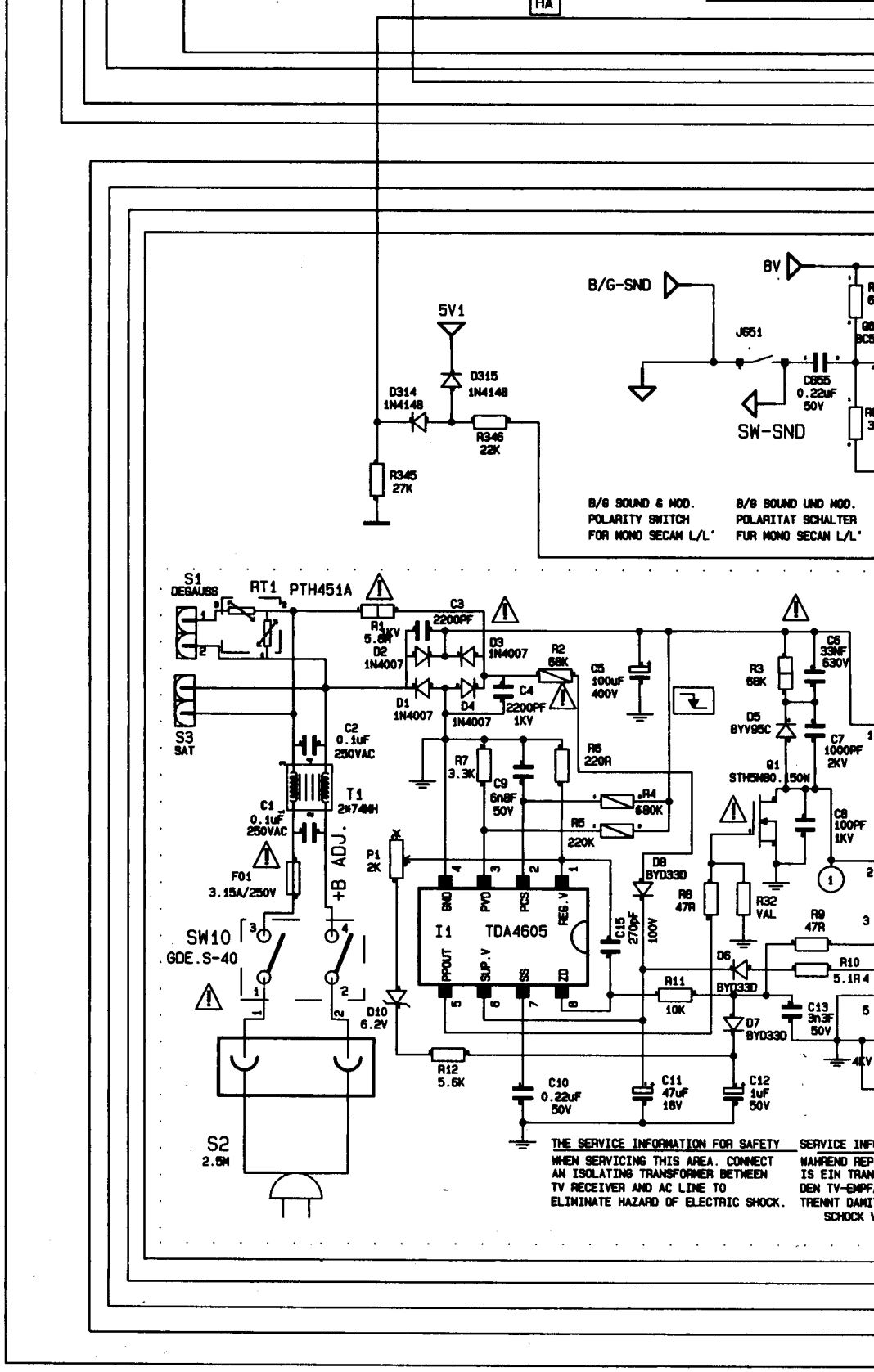
Block diagram (one amplifier shown)


FOR SECAM L/L'
FUR SECAM L/L'
VHF-I
L/LPRIME
SYSB
TU01
WSPTUNER
VTUNE
VOL
BRIG
SAT
CONT
HUE
BND0
BND1
AFC
ST.AV
FE
EXT1
KEY0
KEY1
KEY2
KEY3
KEY4
KEY5
KEY6
MDSTR
GND
P.UP
P.DWN
V.UP
V.DWN
S301
5V
33V
HA

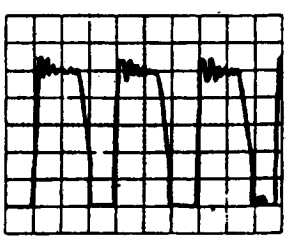

I402
TDA7057AQ
V.CN1
N.C.
VIN1
VSUP
VIN2
SGND
V.CN2
OUT2+
I302
PCF85E82
SDA
SCL
PTC
VDD
VSS
A2
A1
A0
I301
CTV322S (MONO)
CTV352S (STEREO)
VDD
STDBY
SDA
SCL
SYS-1
SYS-2
EXT2
RMOT
IDENT
REST
XTAL2
XTAL1
TEST
D.OSC1
D.OSC2
V.SYN
H.SYN
FB
B
G
R
I10
TDA83
(PAL/SE
TDA8361 (PAL)
A.DEMP
REF.C
REF.C.
IDEN
S.IFIN
EX.A.IN
VOUT
DEC.
GND1
SUP.
GND2
DEC
INCVBSIN
L.PEAK
EXCVBSIN
CHRIN/SS
BRB
B.OUT
G.OUT
R.OUT
INS.
R.IN
G.IN
B.IN
CONT.
SAT.
FBAS
INT.VID
EX.AUD
AGC
B/G-SND
SYS
STDBY
RMOT
AV
VERT.
FB
RED
GREEN
BLUE
8V
5V
5V1
F103
6.5MHz
38.9MHz
X301
10.00MHz
S303
J301
J302
J303
J304
J306
J307
J308
J309
J311
J312
J315
J401


STEREO
PGND2
OUT2-
OUT1-
PGND1
OUT1+
SPEAKERS
S403
S401
I401
TDA7056A (MONO)
N.C.
VSUP
VIN
GND1
VCNT
OUT+
GND2
OUT-
N.C.
12.5V
R403 1R
C401 100NF 25V
C402 470uF 25V
C404 10NF 25V
C633 47nF
C406 4n7F
R406 1R
VOLT
J402
I601
TDA3653
IN1
GND
SN.IN
GND
OUT
SUPP1
GUARD
FLYB.
SUPP2
VERT.SUP
(H.DRV)
C532 47nF
C823 1NF 100V
C827 100uF 63V
C828 470uF 50V
D610 BYD33D
R827 470R
R631 47K
D612
5V
C407 1NF 50V
R820 3.9K
R821 10K
C820 1000PF 50V
C821 4700PF 50V
C822 4700PF 50V
C824 100NF 63V
R825 220R
S602 (VERT.)
V.DEFL.YOKE
V. LINEARITY
VERT.
R451 JUMPER
VERT.PULSE (TXT)
R832 12K
P804 1.8K
R822 56K
C825 2.2uF
C826 1000uF 35V
V.SHIFT
R826 470R
R828
R829 2.2K
P801 10K
R833 15K
P802 500R
R824 1.5R
V.AMP.
D611
R830 8K2
C829
C410 VOLT
R401 1K
C139 220NF
C142 22NF 50V
C141 2.2uF 16V
C140 10uF 16V
D101 1N4148
D100 1N4148
R145 1K
R144 5.6K
8V
U AGC
P102 10K
C137 22NF 50V
C138 100NF 25V
C136 2.2uF 25V
F101
SAF38.9MS51P
R143 330K
C135 22NF 50V
AFC
B.DEC
S.DEC
S.OUT
TUN.T-O
AGC
TUN.AGC
IF.IN.
IF.IN
AFCOUT
VER.DRV
VER.R.G
VER.FB
01CON.
02CON.
FLYIN/S
H.DRV
S.SUP.
XTAL4.43
XTAL3.58
B.PH.DET
SUBOUT.S
B-YOUT
R-YOUT
R-YIN
B-YIN
H/S.CHR
C133 4700PF 50V
C134 0.1uF 63V
R139 12K
C131 4n7F 50V
C132 1uF 25V
HOR.DRV
D111 1N4148
C130 10NF 50V
R138 470K
P101 10K
H.SHIFT
R136 47K
X102
4.433619MHz
C127 18PF 50V
C128 10uF 16V
D112 1N4148
C129 10NF 50V
R137 4.7R
D103
R135 7.5K
Q106 BC547B
R134 6.8K
R133 22K
AV
R613 39K
V.SYNC
R G B SHIFT
C125 4n7F 63V
R132 100K
C126 100NF 25V
B-Y OUT
R-Y OUT
R-Y IN
B-Y IN
5V1
R154 2.2R
C121 1NF 50V
C122 1NF 50
C123 100NF 25V
C124 100NF 25V
-(B-Y) IN
NC
-(B-Y) IN
REF
-(B-Y) O
-(R-Y) O
A.GND
VP.AN
VD
SNDC.
NC
NC
NC
NC
-(B-Y)
-(R-Y)
B-Y IN
R-Y IN
I254


S101
5V
12V
SYS
J101
J102
J103
J104
J105
INT.VID
L/LPRIME
AV
B/G-SND
SW-SND
S102
TV-S/L
TV-S/R
AV-O/R
SYS
SW-SND
IF1
IF2
AV-I/R
GND
5.5M/AV-SW
12V
EX.AUD
GND
INTVID_L/LPRIME
IR. MODULE
D300 RED
R349 1K
5V1
IR02
TFMS1360
GND IR VCC
C324
4700PF 50V
R361 120R
S302
RMOT
BLUE
GREEN
RED
GND
8V
S103
180V
HEATER
S603
8V
AV.VID
TV_VID
AV
R491 75R
C451 47uF 16V
R493
R453 4.7K
R455 8.2K
D451 1N4148
C452 47uF 16V
R492 470R
R494 1.8K
R452 33K
Q451 BC547B
R454 33K
Q452 BC547B
D452 1N4148
R456 2.2K
R457 100R
R460 220R
Q453 BC547B
L451 10UHJ
R458 4.7K
C455 180PF 50V
J451
VID-TXT
5V1
C461 0.1uF 63V
R461 3.3K
C458 1NF 50V
C464 100uF 16V
X451 27MHZ
L452 3.3UHJ
C457 8.2PF 50V
C456 15PF 50V
C459 0.1uF 63V
C460 0.1uF 63V
VIDEO
R462 27K
C462 0.1uF 63V
I451
SAA5254P
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16
VERT.PULSE
R466 8.2K
C474 JUMPER VOLT
Q454 BC547B
R467 22K
ODD/EVEN
R_IN
G_IN
D454 1N4148
R475 100R
D455 1N4148
R476 100R
R477 100R

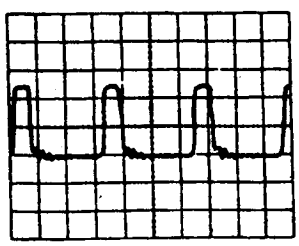


1) 5 usn/div 100 volt/div



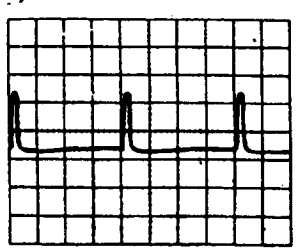
Drain of Q1

2) 20 usn/div 2volt/div

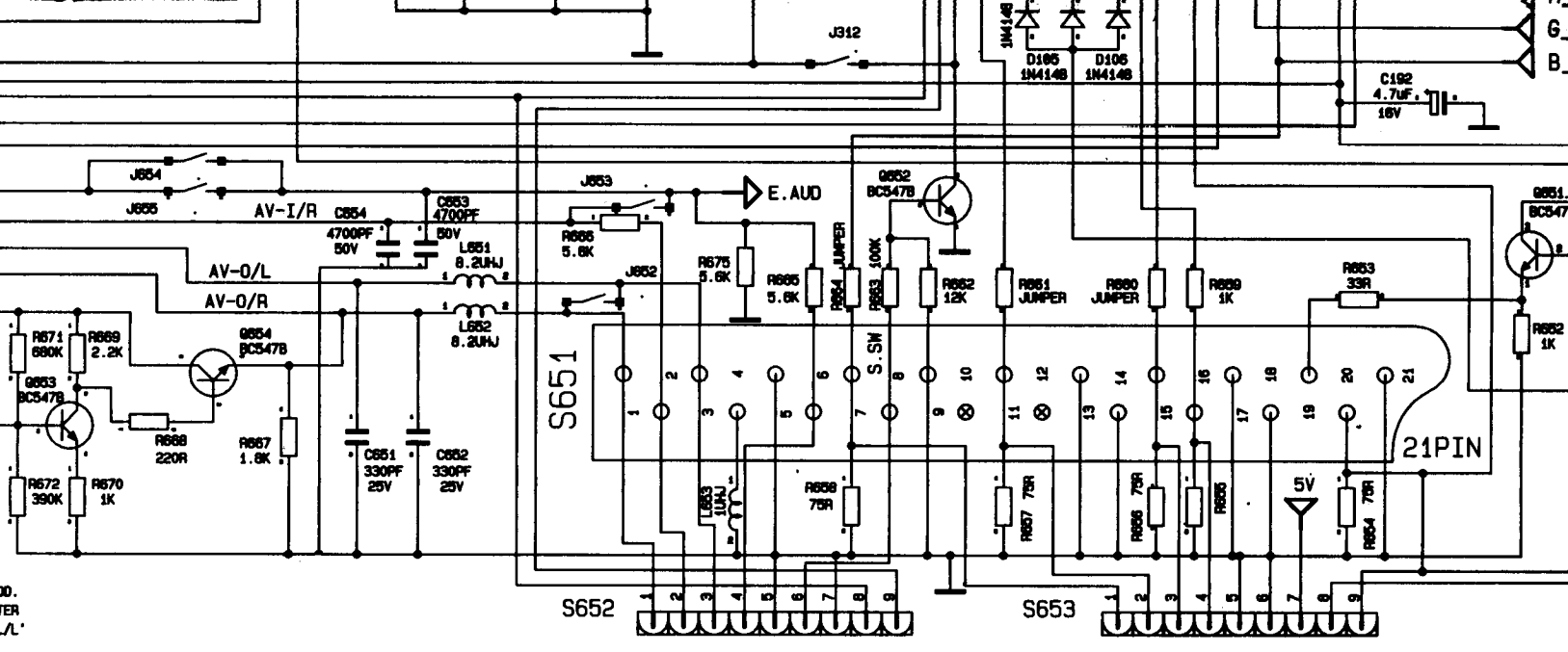


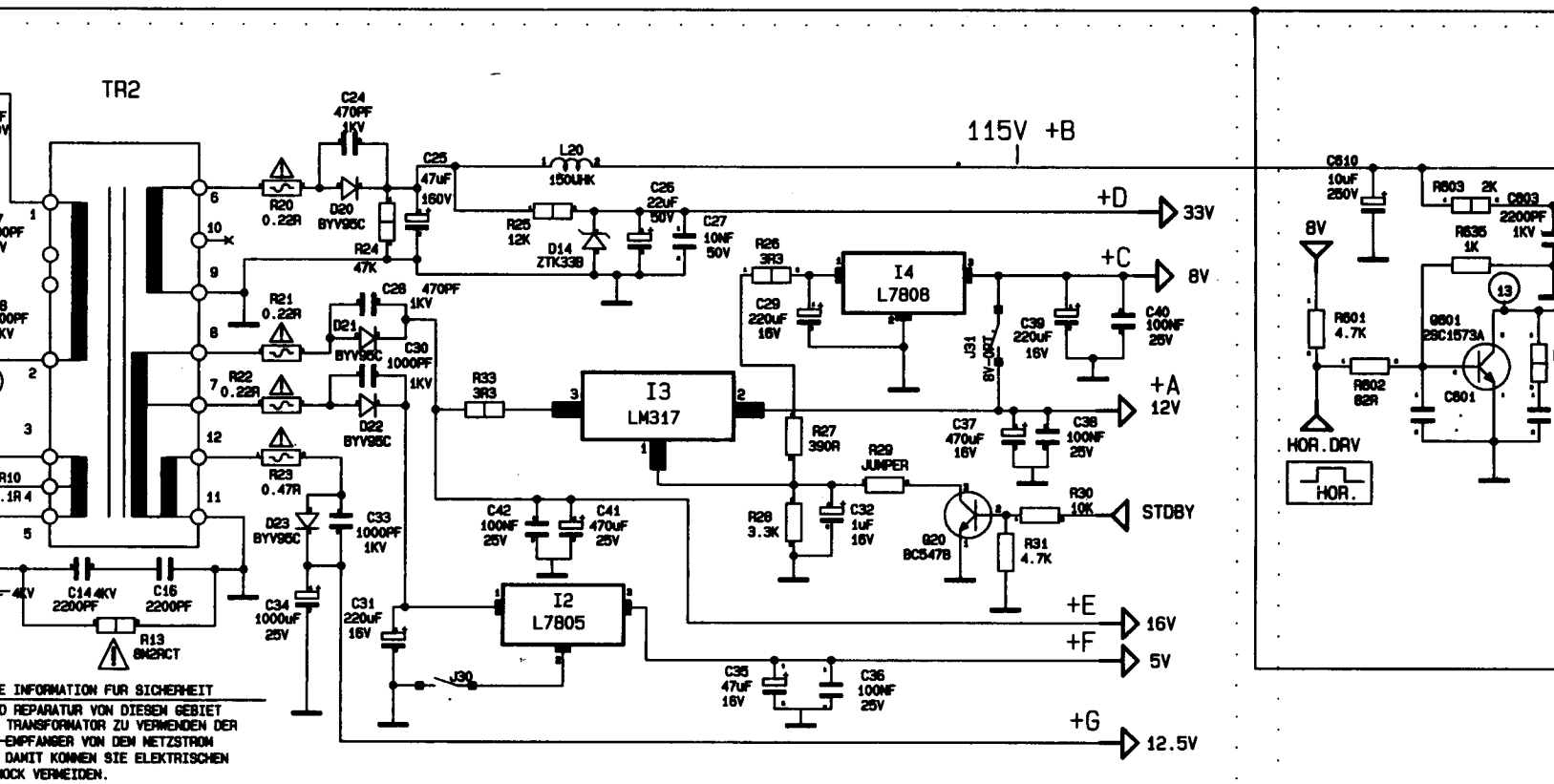
IC 301 pin 26

3) 5m sn/div 2volt/div



IC 301 pin 27



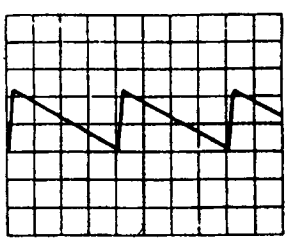


E INFORMATION FUR SICHERHEIT
D REPARATUR VON DIESEN GEBIET
TRANSFORMATOR ZU VERMENDEN DER
-EMPFANGER VON DEM NETZSTROM
DAMIT KONNEN SIE ELEKTRISCHEN
OCK VERMEIDEN.

AV-O/R
AV-O/L
AV-I/R
EX.AUD

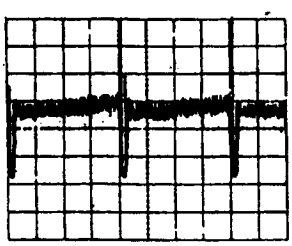
OSCILLOSCOPE S

4) 5 msn/div 0,5 volt/div



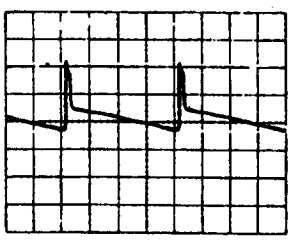
IC 101 pin 41

5) 5 msn/div 1 volt/div



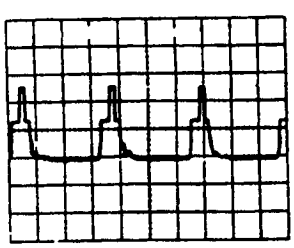
IC 601 pin 3

6) 5 msn/div 20 volt/div

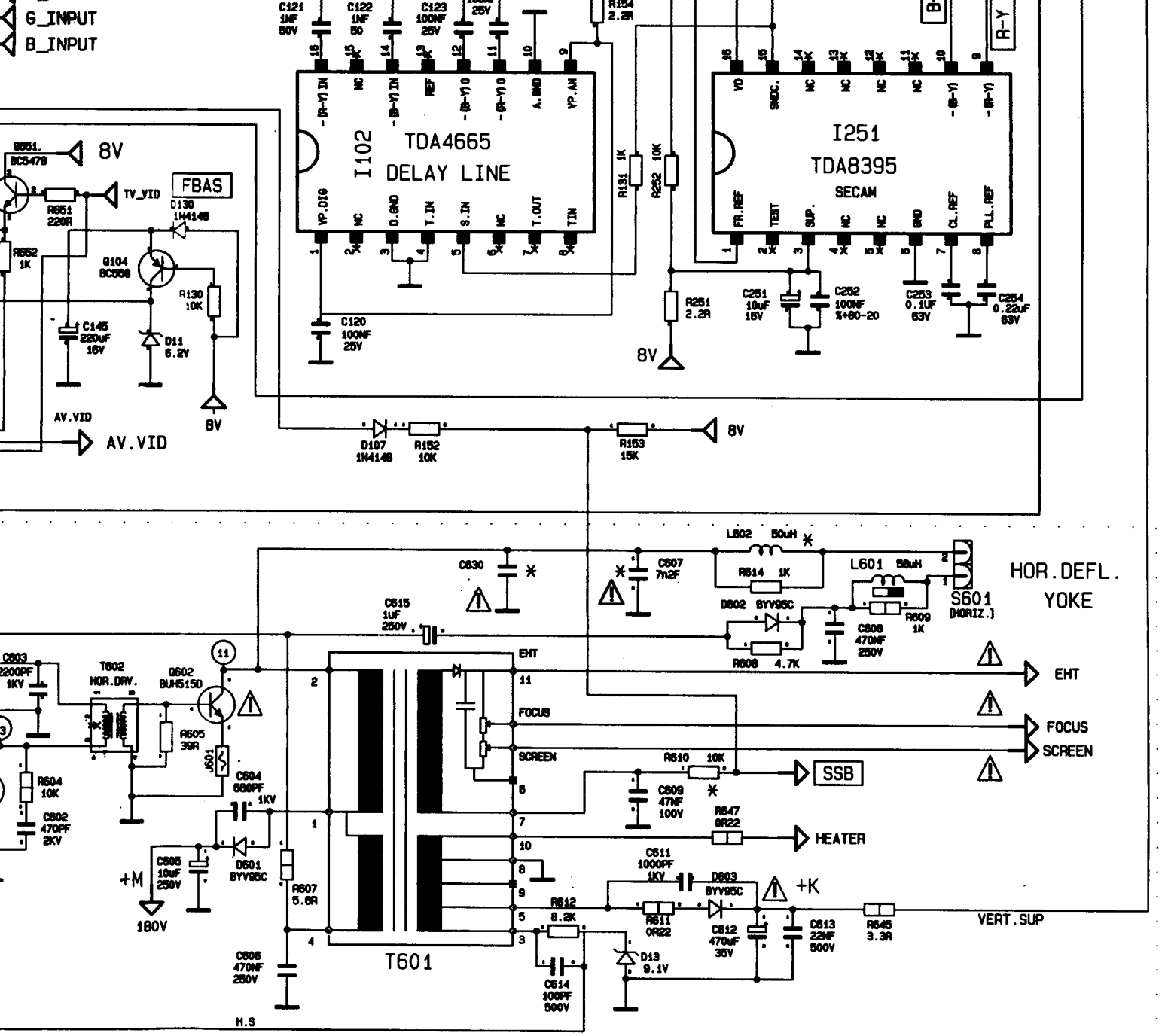


IC 601 pin 5

7) 20 usn/div 2 volt/div

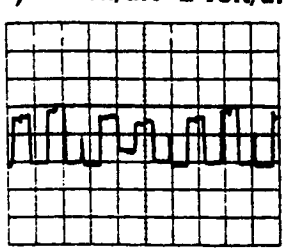


IC 101 pin 38



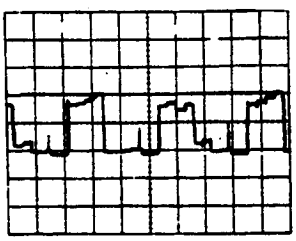
PE SHAPES / OSZILLOGRAMME

8) 20 usn/div 2 volt/div



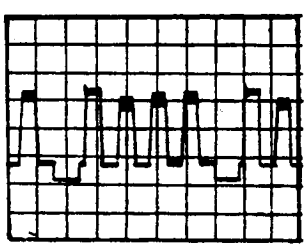
IC 101 pin 20

9) 20 usn/div 2 volt/div



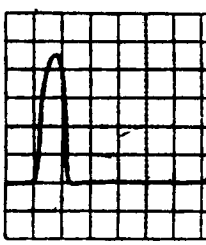
IC 101 pin 19

10) 10 usn/div 2 volt/div

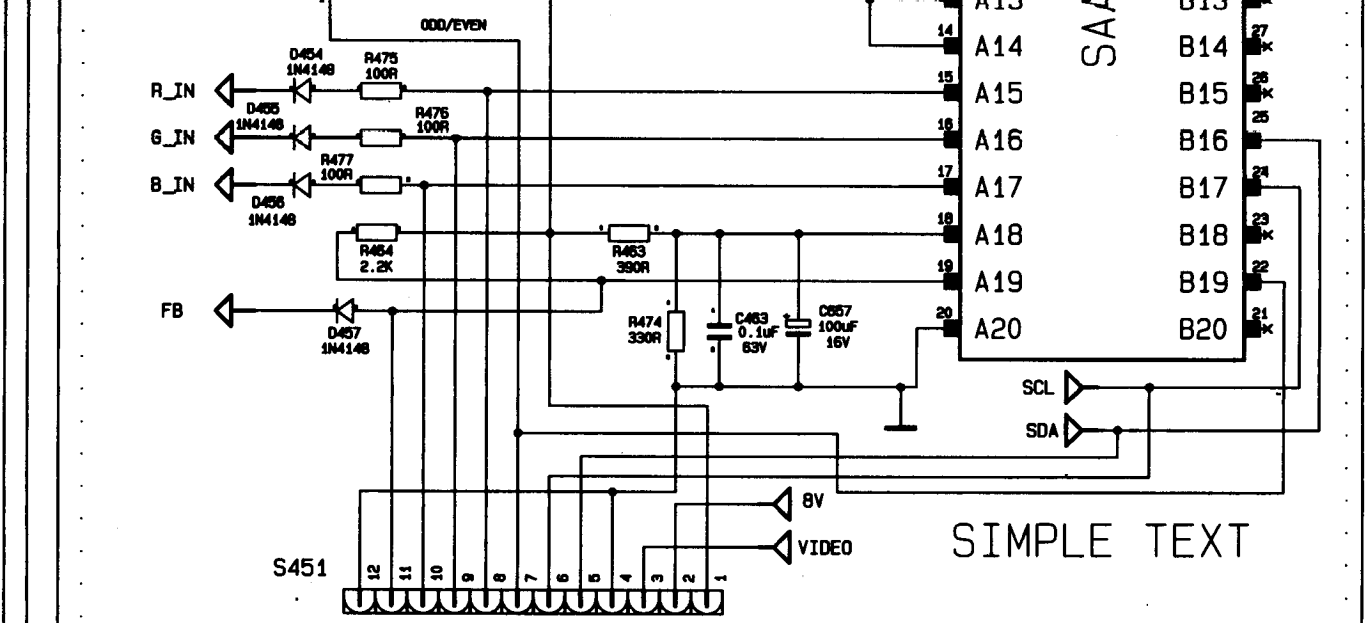


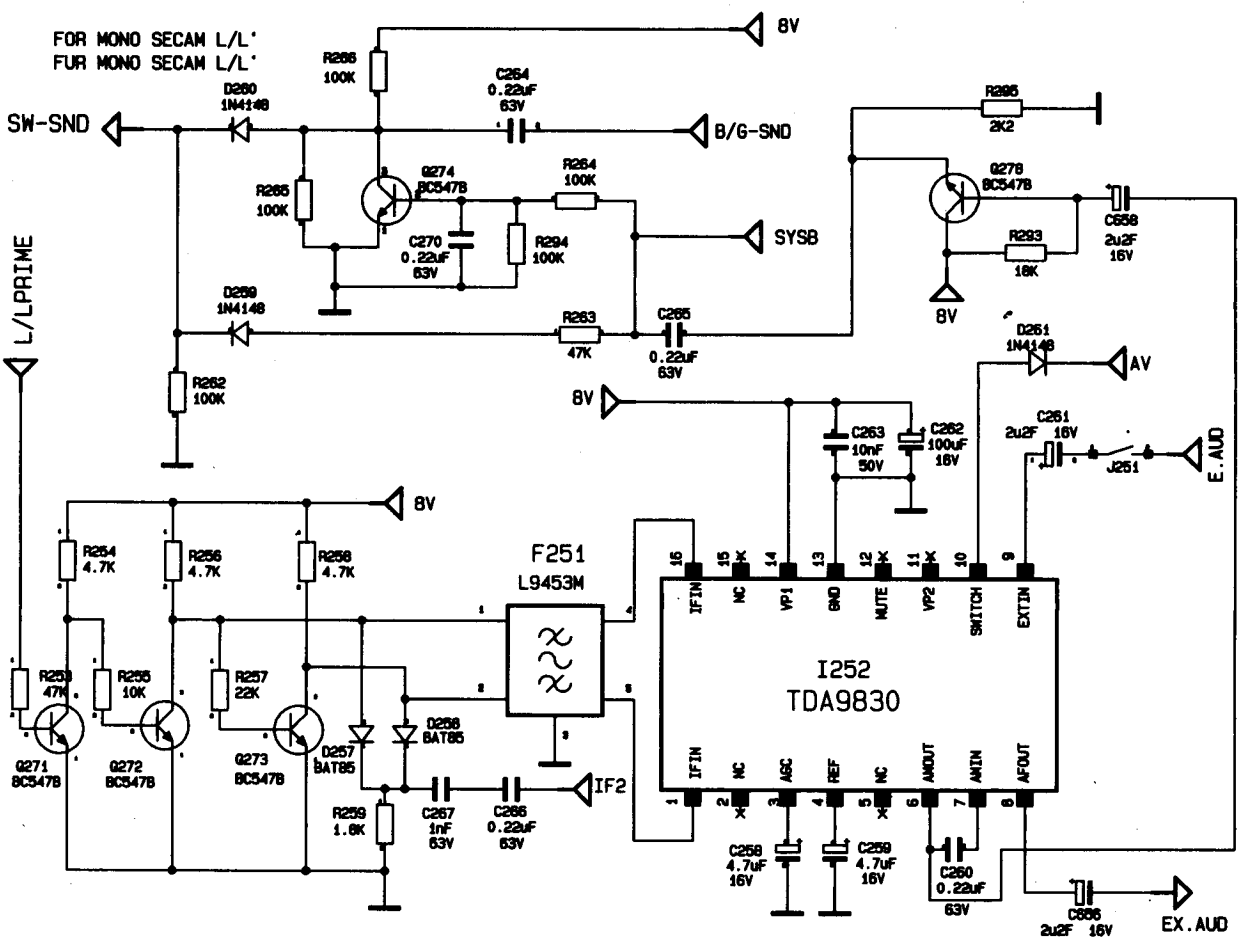
IC 101 pin 18

11) 10 usn/div 250

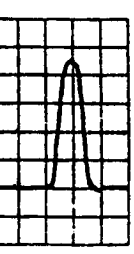


Collector of Q6



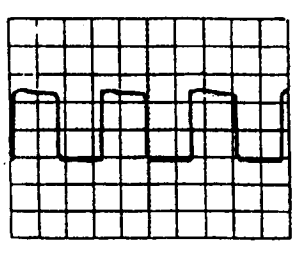


250 volt/div



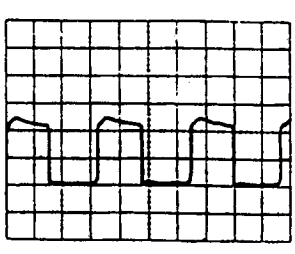
of Q602

12) 20 usn/div 0.2 volt/div



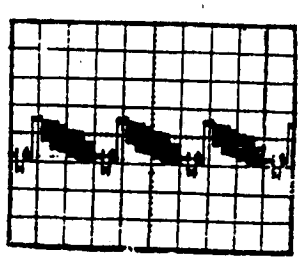
IC 101 pin 37

13) 20 usn/div 50 volt/div



Collector of Q601

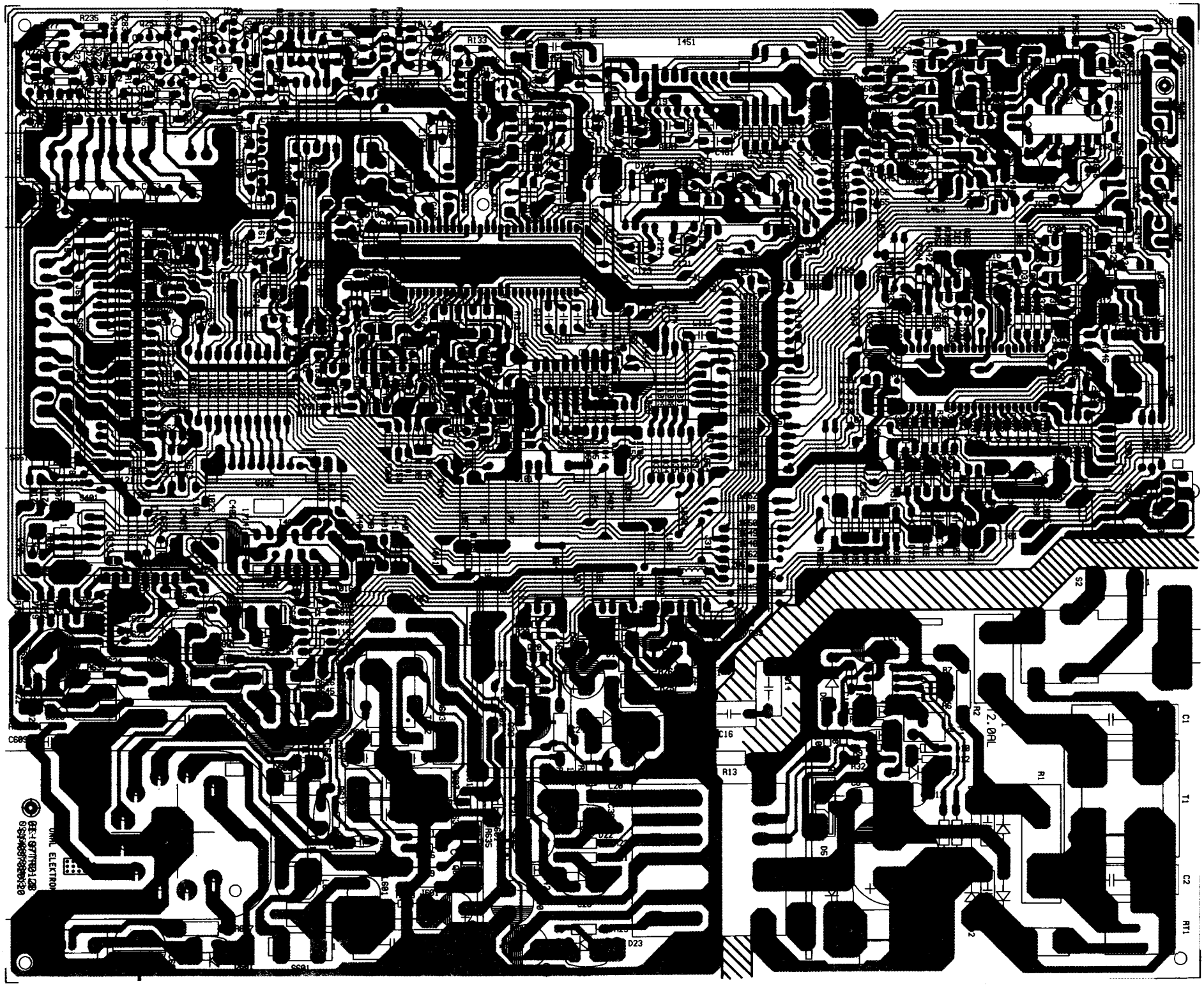
14) 20 usn/div 1 volt/div



IC 101 pin 13

A

06



MAIN CHASSIS BOARD / CHASSISPLATE

FOR SECAM L/L'
FUR SECAM L/L'

VHF-I

VTUNE

5V

8V

SYSB

L/LPRIME

SYS

AGC

TU01
WSPTUNER

I402
TDA7057AQ
STEREO

I301
CTV322S - (MONO)
CTV352S (STEREO)

I302
PCF8582

I101
TDA8362
(PAL/SECAM)
TDA8361 (PAL)

S301

P.UP
P.DWN
V.UP
V.DWN

MDSTR

AFC

VERT.

FBAS

EX.AUD

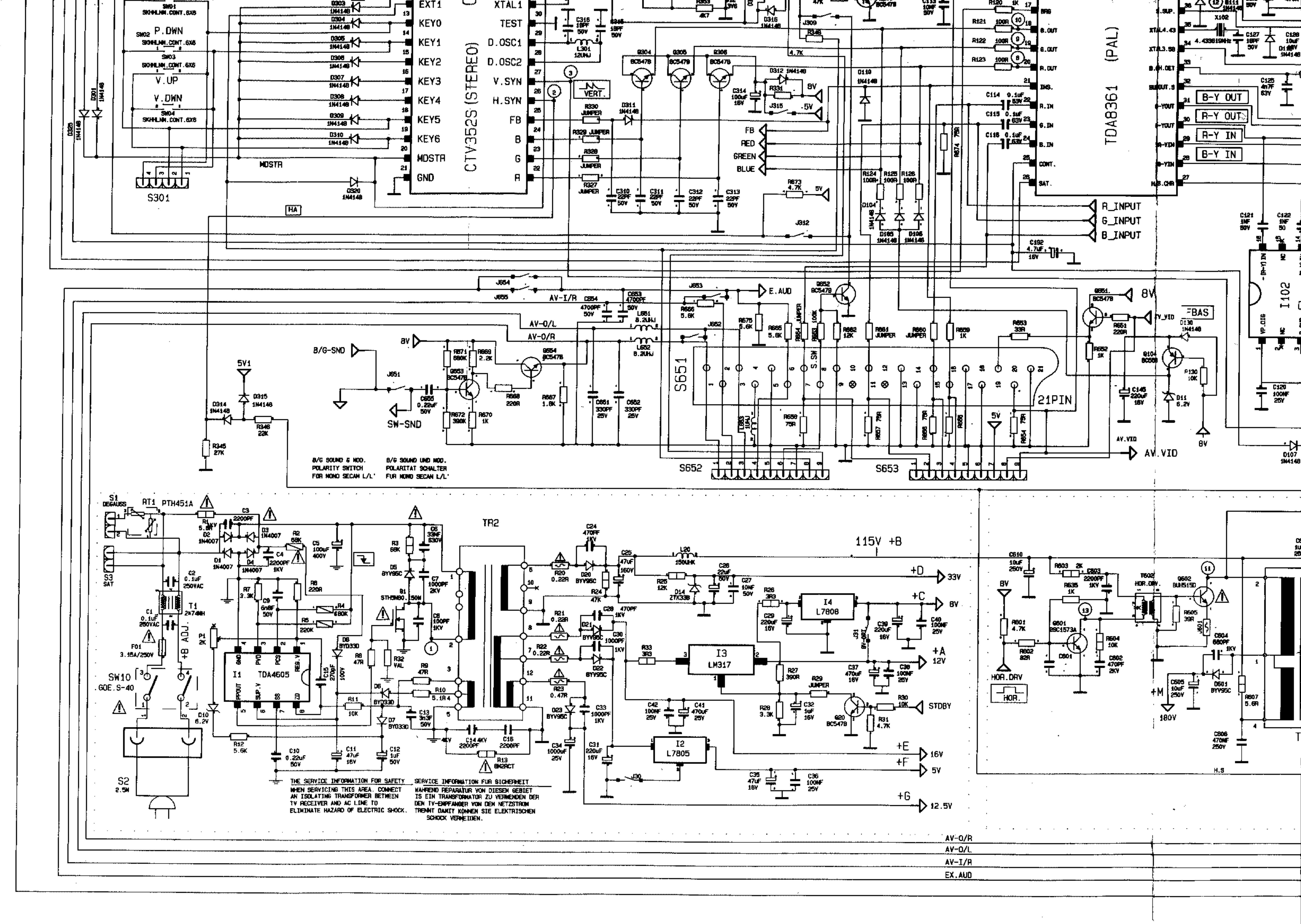
B/G-SND

R_INPUT
G_INPUT
B_INPUT

B-Y OUT
R-Y OUT
R-Y IN
B-Y IN

12.5V

I402
STEREO
VSUP VIN2 SGND V.CN2 OUT2+ PGND2 OUT2- OUT1- PGND1 OUT1+
I401
TDA7056A (MONO)
N.C. VSUP VIN GND1 VOUT OUT+ GND2 OUT- N.C.
SPEAKERS
S403
S401
12.5V
R403 1R
C401 100NF 25V
C402 470uF 25V
C404 10NF 25V
C833 47nF
VOLT
C405 4n7F
R406 1R
AGC
J402
I601
TDA3653
IN1 GND SW.IN GND OUT SUPP1 GUARD FLYB. SUPP2
C832 47nF
C823 1NF 100V
C827 100uF 63V
D610 BYD33D
C828 470uF 50V
R827 470R
R831 47K
R826 220R
C822 4700PF 50V
C824 100NF 63V
C820 1000PF 50V
C821 4700PF 50V
R620 3.9K
R621 10K
C807 1NF 50V
VERT.SUP (H.DRV)
5V
D612
8V
R143 330K
C136 22NF 50V
AFC
S602 (VERT.) V.DEFL.YOKE
V. LINEARITY
VERT.
R451 JUMPER
VERT.PULSE (TXT)
R632 12K
R804 1.8K
R622 56K
C625 2.2uF
R633 15K
R802 500R
V.AMP.
C826 1000uF 35V
R624 1.5R
V.SHIFT
P801 10K
R625 470R
R628
R629 2.2K
R613 39K
V.SYNC
D108
33V
R140 3.9K
H.SHIFT
P101 10K
R136 47K
HOR.DRV
D111 1N4148
X102 4.43361MHz
C127 18PF 50V
C128 10uF 16V
D112 1N4148
C129 10NF 50V
R137 4.7R
R135 7.5K
Q106 BC547B
R134 6.8K
R133 22K
AV
R G B SHIFT
C130 10NF 50V
R138 470K
C131 4n7F 50V
R139 12K
C132 1uF 25V
C133 4700PF 50V
C134 0.1uF 63V
C125 4n7F 63V
R132 100K
C126 100NF 25V
B-Y OUT
R-Y OUT
R-Y IN
B-Y IN
I101
TDA8362
(PAL/SECAM)
TDA8361 (PAL)
A.DEMP REF.C REF.C. IDEN S.IFIN EX.A.IN VOUT DEC. GND1 SUP. GND2 DEC INCVBSIN L.PEAK EXCVBSIN CHRIN/SS BRG B.OUT G.OUT R.OUT INS. R.IN G.IN B.IN CONT. SAT.
B.DEC S.DEC S.OUT TUN.T-O AGC TUN.AGC IF.IN. IF.IN AFCOUT VER.DRV VER.R.G VER.FB H.CON. S2CON. FBYIN/S H.DRV I.SUP. XTAL4.43 XTAL3.58 B.IN.DET SWOUT.S U-YOUT U-YOUT V-YIN B-YIN HUE.CHR
C142 22NF 50V
C141 2.2nF 16V
C140 10uF 16V
D100 1N4148
D104 1N4148
R144 5.6K
R145 1K
C139 220NF
U AGC
P102 10K
C137 22NF 50V
C136 2.2uF 25V
C138 100NF 25V
F101
SAF38.9MS51P
C135 2.2uF 25V
R_INPUT
G_INPUT
B_INPUT
C192 4.7uF 16V
C121 1NF 50V
C122 1NF 50V
C123 100NF 25V
C124 100NF 25V
R154 2.2R
5V1
I251
TDA4565
-(B-Y) IN NC -(B-Y) IN REF -(B-Y) O -(R-Y) O A.GND VP.AN
VD SNDC. NC NC NC NC -(B-Y) -(R-Y)
B-Y IN
R-Y IN
S101
5V
12V
SYS
5V 5.5M/AV-SW 12V EX.AUD GND GND INTVID_L/LPRIME
J101 J102 J103
INT.VID L/LPRIME AV
S102
TV-S/L TV-S/R AV-O/R SYS SW-SND IF1 IF2 AV-I/R GND
J105 J104
B/G-SND SW-SND
IR. MODULE
D300 RED
R349 1K
5V1
IR02
TFMS1360
GND IR VCC
C324 4700PF 50V
R361 120R
C322 4.7NF 16V
S302
AMOT
BLUE GREEN RED GND 8V
S103
180V HEATER
S603
8V
R491 75R
C451 47uF 16V
AV.VID
R493
R453 4.7K
R455 6.2K
D451 1N4148
C452 47uF 16V
TV_VID
R492 470R
R494 1.8K
R452 33K
Q451 BC547B
R454 33K
Q452 BC547B
D452 1N4148
R456 2.2K
R457 100R
R460 220R
Q453 BC547B
R458 4.7K
L451 10UHJ
C455 180PF 50V
AV
J451
VID-TXT
C461 0.1uF 63V
5V1
C464 100uF 16V
R451 3.3K
C458 1NF 50V
C456 15PF 50V
X451 27MHZ
L452 3.3UHJ
C459 0.1uF 63V
C460 0.1uF 63V
VIDEO
R462 27K
C462 0.1uF 63V
I451
SAA5254P
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16
VERT.PULSE
R466 8.2K
C474 JUMPER VOLT
5V1
Q454 BC547B
R467 22K
ODD/EVEN
R_IN
G_IN
D454 1N4148
D455 1N4148
R475 100R
R476 100R



CTV352S (STEREO)
EXT1
KEY0
KEY1
KEY2
KEY3
KEY4
KEY5
KEY6
MDSTR
GND
XTAL1
TEST
D.OSC1
D.OSC2
V.SYN
H.SYN
FB
B
G
R
S301
P.DWN
V.UP
V.DWN
VERT.
FB
RED
GREEN
BLUE
TDA8361 (PAL)
B-Y OUT
R-Y OUT
R-Y IN
B-Y IN
R_INPUT
G_INPUT
B_INPUT
I102
FBAS
AV.VID
S651
21PIN
S652
S653
E.AUD
B/G-SND
SW-SND
AV-I/R
AV-O/L
AV-O/R
B/G SOUND & MOD. POLARITY SWITCH FOR MONO SECAM L/L'
B/G SOUND UND MOD. POLARITAT SCHALTER FUR MONO SECAM L/L'
S1 DEGAUSS
RT1 PTH451A
S3 SAT
T1
SW10 GOE.S-40
S2 2.5W
I1 TDA4605
TR2
115V +B
+D 33V
+C 8V
+A 12V
+E 16V
+F 5V
+G 12.5V
I4 L7808
I3 LM317
I2 L7805
STDBY
HOR.DRV
HOR.
+M 180V
T602 HOR.DRV.
THE SERVICE INFORMATION FOR SAFETY
WHEN SERVICING THIS AREA. CONNECT AN ISOLATING TRANSFORMER BETWEEN TV RECEIVER AND AC LINE TO ELIMINATE HAZARD OF ELECTRIC SHOCK.
SERVICE INFORMATION FUR SICHERHEIT
WAHREND REPARATUR VON DIESEM GEBIET IS EIN TRANSFORMATOR ZU VERWENDEN DER DEN TV-EMPFANGER VON DEM NETZSTROM TRENNT DAMIT KONNEN SIE ELEKTRISCHEN SCHOCK VERMEIDEN.
AV-O/R
AV-O/L
AV-I/R
EX.AUD

TDA8361 (PAL)

B-Y OUT
R-Y OUT
R-Y IN
B-Y IN

R_INPUT
G_INPUT
B_INPUT

R G B SHIFT

I102
TDA4665
DELAY LINE

I251
TDA8395
SECAM

5V1
8V

FBAS
AV.VID
21PIN

V.SYNC

HOR.DEFL.
YOKE
S601
(HORIZ.)
L601 56uH
L502 50uH
T601
T602
HOR.DRIV.

EHT
FOCUS
SCREEN
SSB
HEATER
VERT.SUP
+M
+K
180V

I451
SAA5254P
SIMPLE TEXT

VERT.PULSE
ODD/EVEN
R_IN
G_IN
B_IN
FB
SCL
SDA
VIDEO
S451

SW-SND
L/LPRIME
B/G-SND
SYSB
EX.AUD
E.AUD

I252
TDA9830
F251
L9453M
IF2